Turn-by-turn Trigger Card Operating Manual

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The purpose of the turn-by-turn trigger card is to generate a pattern of triggers that are synchronous with the beam in a circular accelerator. The trigger pattern is arbitrary, and can be fixed or set remotely through an Ethernet connection.

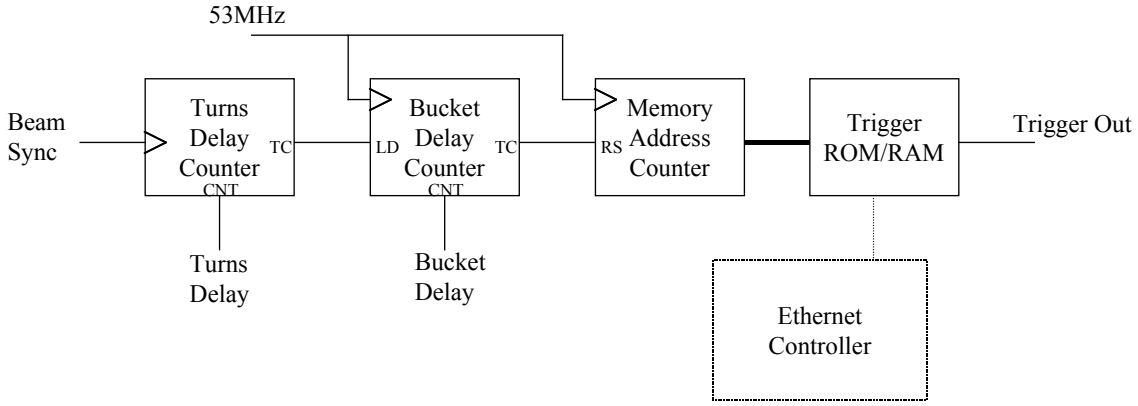

Figure 1: Block diagram of trigger card operation.

A cascade of counters controls the timing of the trigger output. These counters are clocked by the RF input and reset with the beam sync input. The first counter in the chain actually counts beam sync pulses for the purpose of inserting multi-turn delays. Setting the multiturn delay to zero bypasses this counter. Either the terminal count from this counter or the beam sync trigger enables the delay counter. This counter counts the number of buckets set by the front panel thumbwheel switches. Once this counter reaches terminal count, the final counter that addresses the bit wide memory is activated. The memory contains the actual trigger pattern, and it will be a ROM for the "dumb" trigger cards and a RAM for the "smart" trigger cards. The output of the memory drives the trigger output of the card.

There are two possible hardware configurations for this card. The "dumb" configuration uses a ROM as its lookup table and must be reprogrammed for any changes to the trigger pattern. The "smart" configuration contains an Ethernet processor and a RAM as its lookup table. The processor can change the trigger pattern by accessing the RAM during operation. The processor can also be programmed to listen to multi-caste states devices that are broadcast to the Ethernet input. Another difference between the two configurations is the extra trigger input for the smart card or 5C trigger. This trigger acts as an interrupt to the processor to better synchronize changes to the trigger pattern.

I/O Description:

BSYNC – Input – A TTL trigger signal that periodically resets the counters. It is typically synchronized to the beam revolution frequency.

53MHz – Input – This signal triggers the counter clocks. There is a comparator at the front end of this input, so the input signal must have zero crossings to affect a trigger. Either an RF waveform, or an AC coupled square wave will work.

Trigger Out (0-3) – Output – Trigger pattern output. All outputs are copies of the same trigger pattern.

5C Trigger (Smart card only) – Input – TTL trigger signal that interrupts the processor to change the trigger pattern.

LSB----MSB – Front Panel Switch – Bucket delay setting. The least significant digit is on top, and the most significant digit is on the bottom. It should not be set to a value higher than the harmonic number of the machine.

Turns Delay – Front Panel Switch – Sets the number of revolutions between trigger patterns. If it is set to zero, the trigger pattern outputs every revolution. If it is set to one, the trigger pattern plays every other revolution.

Absolute Maximum Ratings:

BSYNC	-1V to 6V
53 MHz	±5V
5C	?

Electrical Characteristics:

Reset

Input Level	TTL
Input Resistance	High Z
Pulse Width min	50ns

53 MHz

Input Voltage Range	-2.5V to 5V
Input Resistance	50_
Operating Point	700mV p-p
Max Frequency[1]	53 MHz

[1] This frequency is really too fast for the address counter, and if triggers are spaced less than 100ns apart, there will be ghost triggers and missing pulses due to bad address sampling. However, the counter still maintains accurate count.

Trigger Out

High level	4V min
Low level	1.5V max
Impedance Drive	50_ min