FAST DIGITIZATION AND DIGITAL RECEIVER TECHNOLOGY

INTRODUCTION

A/D CONVERTER ARCHITECTURES
SAMPLE AND HOLD

m-bit ADC

DOUT

AOUT

Σ

DAC

AIN

AOUT

Σ

2*(m-bits)

DOUT

(m-bits)

DIN

AOUT

Pipelined A/D Architecture
SUCCESSION APPROXIMATION A/D ARCHITECTURE
SIGMA-DELTA A/D ARCHITECTURE
A/D SPECIFICATIONS

Signal-To-Noise Ratio (SNR or S/N)
  rms Signal to rms Noise
  Quantization Error = \( V \times \text{LSB} / \sqrt{12} \)
  \( \text{rms Signal} = 0.5 \ V / \sqrt{2} \)
  \( \text{SNR} = 2^n \sqrt{3} / \sqrt{2} = 1.225 \times 2^n \)
  \( \text{SNR}_{\text{db}} = 20 \ \log (2^n \sqrt{3} / \sqrt{2}) \)
  \( \text{SNR}_{\text{db}} = 20 \ \log (2) \times n + 20 \ \log (\sqrt{3} / \sqrt{2}) \)
  \( \text{SNR}_{\text{db}} = 6.021 \times n + 1.763 \) (dB)
Dynamic Range (DR)

Signal-to-Noise And Distortion (SINAD)

Effective Number of Bits (ENOB)

$$ENOB \text{ (bits)} = \frac{(SINAD - 1.763)}{6.021}$$
Aperture Uncertainty (Jitter)

Seconds rms

\[ \text{SNR} = -20 \log (2\pi F_{\text{in}} \times T_{\text{au}}) \]

For \( T_{\text{au}} = 0.25 \) ps rms

\( F_{\text{in}} = 10 \) MHz, \( \text{SNR} = 96 \) dB

\( F_{\text{in}} = 100 \) MHz, \( \text{SNR} = 76 \) dB

\( F_{\text{in}} = 500 \) MHz, \( \text{SNR} = 62 \) dB
Spurious-Free Dynamic Range (SFDR)

Amplifier SFDR = \(\frac{2}{3}(P_1 - P_0 - 10 \log(BW) - NF)\)

- \(P_1 = \text{IP}_3 - \text{GAIN}\)
- \(P_0 = \text{Input Noise Power (-114 dBm, 50 Ohms)}\)
- \(BW = \text{Bandwidth in MHz}\)
- \(NF = \text{Noise Figure}\)

*Example:*

\[\text{SFDR} = \frac{2}{3}(+38 - 16 - 0 - 114 + 4) = -88 \text{ dB}\]

A/D SFDR = rms signal to peak spurious component

A/D SFDR can be > ideal SNR

Dither Noise for Better SFDR
Processing Gain

Frequency Domain
Gain = 10 Log (number of points) Complex
Gain = 10 Log (number of points/2) Real

Time Domain
A/D Integrated Noise Is Constant
Increasing Sample Rate Lowers Noise Per Sample
Gain = 10 Log (Decimation)
Filter Design Can Give Slight Increase
There Is A Limit To The Passband Noise Floor
Correlated Digital Sample Noise Floor
Digital Low-Pass Filter (Optional)

RF Input

AMP

LO 1

Local Oscillator

LO 2

Local Oscillator

Power Splitter 2-Way 90 Deg.

1st IF

I & Q Demodulator

I & Q Demodulator

Power Splitter 2-Way 90 Deg.

LO

RF

90Deg

0Deg

I

Q

Square Law Detector

Square Law Detector

A/D Converter

A/D Converter

Digital Low-Pass Filter (Optional)

Baseband

I

Q

ANALOG RECEIVER
DIGITAL RECEIVER

RF Input

AMP

Local Oscillator

LO 1

1st IF

A/D Converter

NCO

(LO 2)

Sine

Cosine

Tuning Frequency

Phase Offset

Digital Low-Pass Filter

Digital Low-Pass Filter

I

Q

Baseband
Digitization Requirements

Band-Limited

Headroom
Digital Mixing

Fs/4 Up/Downconversion

\[ I(t) = A(t) \cos(2\pi F(t)) \]
\[ Q(t) = A(t) \sin(2\pi F(t)) \]

0° - 90° - 180° -270°

Consine Sequence
1 0 -1 0

Sine Sequence
0 -1 0 1

Fs/2 Spectral Inversion (1, -1)

Numerically Controlled Oscillator (NCO)
\[ I(t) = A(t) \cos(\text{PV}(t)) \]

\[ Q(t) = A(t) \sin(\text{PV}(t)) \]

**NCO BLOCK DIAGRAM**
CORDIC Precision

Clock Rate (LO Frequency)

Multipliers (18 x 18)

Interleaved NCO’s

I(t) and Q(t) Filtering
Digital Filtering

CIC (High Decimations)

FIR (Sharp Response)

Commercial Digital Receiver Chips

Analog Devices

Graychip (TI)

Harris (Intersil)
Decimate by \( R \) (N Stages) (N Stages) 

Integrator 

Comb 

\( M=1 \) 

Decimating CIC Filter
CIC Response (Decimating)

Magnitude Squared \( P(f) = \left(\frac{1}{(M \times R)^N}\right)^2 \sin (\pi M f R / f_s) / \sin (\pi f / f_s))^2 \)

\( f_s = \) input sample rate
\( R = \) decimation
\( f = \) input frequency

Often Plotted Normalized to \( f_{\text{out}} = f_s / R \)

\( P(f) = (\sin (\pi M f) / \sin (\pi f / R))^2 \)

\( P(f)_{\text{dB}} = 10 \log (P(f)) \)
CIC RESPONSE

Decimate by 4, Varying Order

Varying Decimation, Order = 4
CIC ALIAS REJECTION

Order = 4, Decimation = 4

Order = 4, Decimation = 64
FIR Filters

Transversal Filter Equivalent
Sharp Response
Number of Taps
Numerical Precision
Polyphase
Fully Parallel
Symmetrical Coefficient FIR is Phase Linear
Window Functions (Blackman, Hamming, etc.)
Remez (Parks-McClellan)
5 Tap Symmetric FIR Filter
FIR BLACKMAN

Decimate by 4
FIR BLACKMAN

Decimate by 16
CIC ALIAS REJECTION

Order = 4, Decimation = 64
CIC (Order 4, Decimate by 64) with 127-Tap FIR, Decimate by 2
(18-Bit Coefficients, Decimate by 4 Design)
CIC (Order 4, Decimate by 64) with 127-Tap FIR, Decimate by 2
(18-Bit Coefficients, Decimate by 4 Design)
ECDR-GC314-PMC Raw A/D Data

Source: 21.03 MHz. 5.5 dBm @ HP8664A with 20 MHz HPF and 32.4 MHz LPF at Channel 1 Input. Clock: 64.8 MHz. Crystal Oscillator with 60 MHz HPF and 65 MHz LPF. 2048 Point FFT
ECDR-GC314-PMC Receiver Data

Source: 21.03 MHz. 5.5 dBm @ HP8644A with 20 MHz HPF and 32.4 MHz LPF at Channel 1 Input. Center Frequency at 21.02355 MHz.
Clock: 64.8 MHz. Crystal Oscillator with 60 MHz HPF.
Receiver Processing Gain = 10Log(256) = 24 dB, 4096 Point CFFT.
A/D S/N (Jitter) = -20Log (2π21.03x10^6(0.1x10^{-12})) = 97.6 dB
Digital Receiver Advantages

Improved Performance
- Reduced Components and Cost
- No Component Tolerance, Frequency or Temperature, etc. Dependence
- Reduced Obsolescence
- Improved SFDR
- Near Perfect I&Q Balance
- Near Perfect Filtering

Application Commonality
- Easily Reconfigured
- Reduced System I/O
- Distributed Processing
Product Design Considerations

Today’s Technology Requirements
- Schematic Capture
  - Component Libraries
  - Parts Footprints
  - BOM
  - Netlist
- Notes and Documentation
Board Layout

CAD
Auto-routers
Multi-layer
Vias
Controlled Impedance
Mechanical Considerations
Special Requirements (Mixed-Signal)
Product Manufacture

PC Board Manufacture
   Capabilities Required
   Min. Quantities Hole Size, Line Width, Controlled Impedance, Testing, etc.

PC Board Stuffing
   Min. Quantities, Component Size, Inspection, Testing, etc.
Example Beam Instrumentation Product Design

Bunch-by-Bunch Current Monitor
   Include Co-adding

Support Beam Steering

Example Parameters
   $F_{RF} = 360 \text{ MHz} = F_{CLK}$
   Number of Bunches = 300
   $F_{REV} = 1.2 \text{ MHz}$
   Trigger = Bunch 1
   Four BPMs
   Band-limited Analog Inputs
Design Elements

A/D: AD9430 (12-bits, >210 MSPS, 700 MHz BW)
Time-Interleaved Pairs

PECL Clock Logic

Programmable Logic
Altera Stratix FPGA (One Per Channel)
In-Circuit Reprogrammable Configuration

Standard Bus Interface (VME, PCI, etc.)

Additional Altera Stratix FPGA
Beam Steering Algorithms
A/D #1 Data
LVDS 180MSPS

LVDS-TO-LVTTL

∑ Logic

Dual Port RAM

FIFO Memory

Output Logic

Local Data Bus

Beam-Steering FPGA

A/D #2 Data
LVDS 180MSPS

LVDS-TO-LVTTL

∑ Logic

Dual Port RAM

FIFO Memory

FIFO Memory

FIFO Memory

FIFO Memory

Logic

Logic

Logic

Logic

90MSPS Control

Clock

Trigger

Timing & Control Logic
Other Bunch Data Processing Options

Individual Bunch Filtering
Individual Bunch Digital Receiver (1.2 MHz)
Multi-Bunch Digital Receiver (360 MHz)

Beam Steering Algorithms

Difference-Over-Sum
AM/PM Conversion
Log-Ratio
Stable Beam Suppression

IP Cores

Log, Rectangular-to-Polar, FIR, DFFT, etc.

In-Circuit Programming
# The Stratix Device Family

<table>
<thead>
<tr>
<th>Device</th>
<th>Logic Elements</th>
<th>32x18 M512 Blocks</th>
<th>128x36 M4K Blocks</th>
<th>4,096x144 MegaRAM Blocks</th>
<th>Total RAM Bits</th>
<th>DSP Blocks</th>
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<td>10,570</td>
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# Package Offerings & User I/O

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<tr>
<th>Device</th>
<th>672-Pin BGA Wire-Bond 1.27 mm 35 x 35</th>
<th>956-Pin BGA Flip-Chip 1.27 mm 40 x 40</th>
<th>672-Pin FBGA Wire-Bond 1.0 mm 27 x 27</th>
<th>780-Pin FBGA Flip-Chip 1.0 mm 29 x 29</th>
<th>1020-Pin FBGA Flip-Chip 33 x 33</th>
<th>1508-Pin FBGA Flip-Chip 40 x 40</th>
<th>1923-Pin FBGA Flip-Chip 45 x 45</th>
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↑ Vertical Migration Supported