

OPERATIONS BULLETIN #888

FERMILAB ENERGY DOUBLER BEAM POSITION MONITOR SYSTEM

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July 28 1982

1.0 INTRODUCTION

Although many documents have been written on the proposed beam position monitor system for the energy doubler there seems to be an omission of an overview which describes the system in general, and in addition acts as a bibliography for the rest of the documents. This document is intended to fill that gap. The first section of this document will describe the goals and design criteria of the BPM system. Data acquisition schemes are discussed next along with a brief description of the formatting and presentation of this data to the host computer. The final section will deal with the hardware as a block diagram description. A listing of documents grouped as BPM Design Notes is included at the end.

The emphasis throughout this document is on aspects of the system which will be reflected in the response of the system as viewed by a Main Control Room user.

2.0 GOALS AND DESIGN CRITERIA

The goals considered in designing the BPM system can be summarized as follows:

1. Protection of the superconducting magnets by aborting the beam if the closed orbit measured at any detector exceeds a unique preset limit. These measurements can be repeated at a rate up to once per millisecond. There are two sets of abort limits chosen as a function of energy. Larger excursions of the beam are allowed at lower energies. The energy at which the processor switches from 'low field limits' to 'high field limits' is settable by the host.
2. A second category of preset limits is set inside (ie. closer to the center of the beam chamber) the abort limits. These limits are used during the

- measurement cycle to provide alarming. As in the case of the abort limits there are two sets of the alarm limits for low/high field use.
3. A circular buffer of data taken during this measurement cycle is maintained so that an analysis of beam position leading to an abort can be done after the abort has occurred.
 4. The data from selected measurement periods can be written to a separate memory for purposes of feedback control of correction elements.
 5. The data from selected measurement periods is available to the host for realtime plotting of closed orbits.
 6. Position information from two detectors per service building will be available as analog signals for MADC inputs.
 7. In addition to measuring the position of Booster size batches of beam the system must also be able to provide position measurements on one 53 MHz bunch of beam. (In the remainder of this paper "Batch Mode" refers to 20 or more contiguous bunches of beam. "Bunch Mode" applies to a single isolated bunch of beam.)
 8. The system must be able to measure the position of counter rotating antiproton bunches.
 9. The system must be able to measure beam position over a range of +/- 1.0 inch (25.4 MM), with a resolution of 0.5 MM. Present system parameters indicate that beam position can be measured with a resolution at beam chamber center of 0.15 MM.
 10. The system must be able to measure position information over an intensity range of $1.0 * 10^8$ to $3.0 * 10^{10}$ in the batch mode, and down to an intensity of $1.0 * 10^{10}$ in the bunch mode.
 11. The system is self synchronizing. This implies that the beam must have a gap of missing bunches at least 200 nanoseconds in duration.
 12. The system will provide a means of measuring single turn beam position, triggerable within a window of 20 microseconds. This mode of operation will also provide intensity information from each detector.

13. The system will contain self testing hardware and software.

Two documents provide further information on specifications and design criteria:

- o Beam Position Processor Specifications, 6/16/80 and revised 7/7/80. This is a unclassified, unnumbered document without an author's name, but presumably written by Bob Shafer.
- o Properties of Beam in Doubler. This memo is unclassified, unnumbered, undated and handwritten. It was written by Bob Shafer.

3.0 DATA ACQUISITION SCHEMES

3.1 Snapshots

A primary task of the BPM system is that of protecting the super conducting magnets from quenches resulting from beam being missteered into them. In order to accomplish this task the BPM system includes a basic cycle which is pressed into action whenever beam is in the doubler. This repetitive process has become known as taking snapshots. In theory the process is simple. The closed orbit is measured for each detector; the beam position is compared against two sets of limits, one for aborting and a second less stringent limit for alarming purposes; appropriate action is taken if limits are exceeded; and the data is stored away in a circular buffer.

In practice the process is quite involved and will be discussed in greater detail at a later time. However the basic points as well as the data structures controlling the process are discussed here.

3.1.1 Closed Orbit Measurement - The analog circuits of the BPM system are capable of measuring position in a fraction of a revolution. This information in and of itself does not provide closed orbit information because a closed orbit is defined as the path a particle with no betatron oscillations will take around the machine. In order to determine what this path is, the effect of the betatron oscillations must be eliminated. To accomplish this, an average of single turn measurements is made. Since the fractional tune of the doubler is .4, a minimum of 2 to 3 samples on adjacent turns must be used to derive this average. In the BPM system the number of turns used for averaging is selectable at 8.

16, 32, or 64 assuring good closed orbit information. A precaution has to be taken at this point for the following reason. The entire single turn measurement process takes just under 5 microseconds at which time a second measurement could be made. As mentioned earlier the actual trigger for measurement is the intensity signal. (The sample and hold is 'edge' triggered by the intensity signal going from zero to a level indicating a required amount of beam.) If the doubler contained two booster batches on opposite sides of the ring a measurement would be taken on each batch unless some means is provided to 'hold off' the arming of the next measurement. For this purpose a control parameter is provided called MEASUREMENT HOLDOFF which is settable by the operator from 5 - 16 usec in units of 1 usec. It specifies the fastest rate at which single turn measurements used in the closed orbit averaging can be taken.

An additional variable requires definition in regard to this averaging process. In the BPM it is called FRAME CYCLE LENGTH (one measurement averaging period has become known as a 'frame') and it refers to how often the averaging cycle is repeated. It is settable from 1 - 15 milliseconds in units of 1 msec. Note that the shortest frame cycle length (1 ms) and the maximum number of measurements for average (64) are not compatible: $(64 * 2\mu s = 1.34ms)$. The choice of this combination of parameters would invalidate data, and therefore will not be allowed by software.

At the end of the frame cycle the averaging is done (by hardware) and a Direct Memory Access (DMA) transfer is done from the hardware into processor memory.

3.1.2 Snapshot Frame Processing - The processor acts on the data as outlined below. Note that throughout the process the position information transferred from hardware is merged with status bits and other information to form the SNAPSHOT DATA FRAME, 20 bytes containing all pertinent information about the snapshot frame. The data frame is outlined in the next section.

1. The processor first must determine if each channel contains valid position information. Several considerations are used, one of which is the DETECTOR PRESENT MASK, a 12 bit mask downloaded from the host. In addition to indicating to the processor which of its twelve channels actually has a detector connected to it, this mask can be used to remove a channel from the scan if it isn't working. Other considerations determining the validity of position information will be discussed later.
2. A scan is done of all channels containing valid information to determine if any have exceeded their abort limit. Each of the twelve channels has its

own limit, and as mentioned earlier there are two sets of limits for low and high field. The criteria used to determine which set to use will be discussed later. The limits are symmetrical around the center of the beam chamber. Any channel exceeding its limit is flagged by setting a bit in the data frame, and a mask downloaded from the host (ABORT MASK) is used to determine if this channel is inhibited from causing an abort. If it is not inhibited, an abort counter is incremented. At the end of the scan the abort counter is compared against another downloaded parameter called ABORT MULTIPLICITY. This parameter indicates to the processor how many uninhibited channels with valid data must exceed their abort limits before the processor can pull the abort line.

3. The processor inserts the cycle time into the snapshot data frame.
4. All channels with valid data that exceed their alarm limit are flagged by setting a bit in the data frame. If this is true of any channel the host is notified via an unsolicited message. The processor then stores the contents of the SNAPSHOT DATA FRAME into a special Alarm frame Buffer which the host can access.
5. The SNAPSHOT DATA FRAME is then written into the Snapshot Circular Buffer, a buffer of the most recent 512 SNAPSHOT DATA FRAMES. Note that if an abort occurs for any reason in the energy doubler this buffer is immediately frozen.
6. Data from channels which have been selected for fast time plotting are written to two D/A's.

3.2 Flashes

The second data gathering technique employed by the BPM system is referred to as a flash. It is primarily intended to be a tune up tool when first attempting to get beam to circulate in the doubler. Each BPM system will respond to an event encoded on the energy doubler clock by taking single turn measurements of both beam position and intensity from all channels. No checking for limits is done; the data is simply packed into a FLASH DATA FRAME (discussed in a later section) to be read out by the host. The procedure is simpler than in the snapshot case; the details are a matter of hardware. However several important observations are provided.

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1. Although intended for first turn tune-up, flashes may be taken anytime there is beam in the machine.
2. Once the BPM receives the command to take a flash, data acquisition in the snapshot mode is terminated until flash data is taken and placed into its data frame buffer. This implies that the doubler is not protected by the BPM during a flash. Therefore flashes should not be initiated indiscriminately.
3. The flash mode points out the motivation for designing the BPM with intensity edge triggering. Doubler tune-up will be done with one quarter of a booster batch (20 contiguous bunches) at low intensity. The data will be measured at each detector as the electronics for that detector sense the intensity crossing a predefined limit.

3.3 Profiles

This is not a different data acquisition scheme as far as the BPMs are concerned, but it does provide a different means for the host to acquire the data. Upon receipt of a command (a doubler clock event) the BPM copies the most recent SNAPSHOT DATA FRAME from the Snapshot Circular Buffer into a second buffer called the Profile Buffer. This buffer can hold 256 SNAPSHOT DATA FRAMES, providing space for data from up to 256 profile commands which could be issued during the acceleration process. The Profile Buffer is not a circular buffer, data will not 'wrap around'. This buffer is not intended as a reconstruction buffer as is the Snapshot Buffer. It is intended to be used as a representation of the closed orbit throughout the acceleration cycle, primarily for programming correction elements.

3.4 Displays

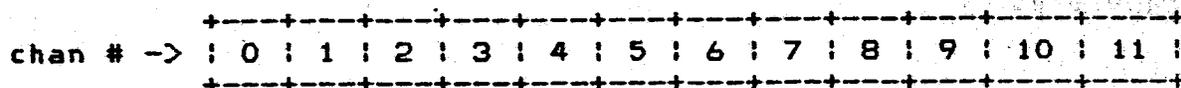
This acquisition scheme provides the capabilities of data displays most similar to the main ring system. A difference is that the orbit can be displayed multiple times during the acceleration cycle. As far as the BPM is concerned the process is similar to the profile technique mentioned above. Upon receiving a command (a doubler clock event) the most recent SNAPSHOT DATA FRAME is written into a single frame Display Buffer. This frame is available to the host and it is expected that the host will read its contents before the next command for a display frame is issued.

4.0 BPM DATA FORMATS

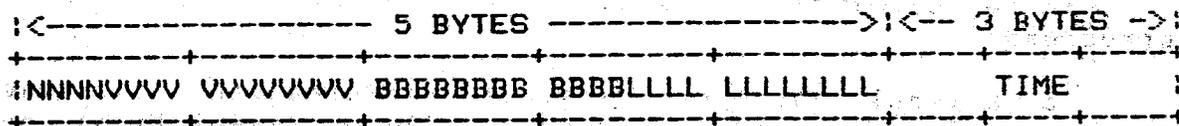
The two primary BPM data structures are outlined in this section. The information included here is only for the readers reference as to what is included in these structures. This is not intended to be a programmers guide.

4.1 Snapshot Data Frame

The SNAPSHOT DATA FRAME contains 20 bytes of data and status. The first twelve bytes contain position information for the twelve channels.



The final eight bytes include:



and are explained as follows.

N: These four bits indicate how many of the 12 channels reported the passage of beam at least once during the averaging cycle.

V: Bits labeled with an 'V' are Valid Data Bits. These bits are an 'ANDing' of the detector present mask with 12 Averaging Complete Bits returned from the hardware. The averaging complete bits indicate if the associated channel reported the passage of beam enough times during the frame cycle to complete the specified averaging. A '1' indicates valid data.

B: Bits labeled with a 'B' are Abort Status Bits. A '1' means that the position exceeded the abort limit for that channel.

L: Bits labeled with a 'L' are Alarm Status Bits. A '1' indicates that the position exceeded the alarm limit for that channel.

Time: The final three bytes contain the time stamp for the frame. A least count is one millisecond providing times up to 280 minutes.

4.2 Flash Data Frame

The FLASH DATA FRAME contains 30 bytes of data and status. The first 12 bytes contain position data; the second 12 bytes contain intensity data. Bytes 25 and 26 are:

```
+-----+-----+  
!XXXXVVVV VVVVVVVV!  
+-----+-----+
```

where the 'X's are don't care bits and the 'V's indicate if the associated channel reported passage of beam on the beam revolution in question. A '1' indicates valid data. The final four bytes contain the time stamp for the data frame in units of 10 microseconds.

4.3 Further Information On Data Formats

Three documents provide further information on these data structures.

- o Several documents provide information on the conversion of the eight bit representations of position and intensity into millimeters and protons per bunch. The primary source is:
BPM Design Note #1: EXPECTED CALIBRATION AND CALIBRATION TOLERANCES OF THE BEAM POSITION SYSTEM, Bob Shafer, 11/3/81

These numbers are refined in:

BPM Design Note #4: MEASUREMENT OF R.F. MODULE CALIBRATION CONSTANTS AND TOLERANCES, Don Martin, 4/17/82

- o Several nebulous references are made to 'detectors sensing the passage of beam'. This is explained BPM Design Note #5 on the Analog Box
- o A forthcoming BPM Design Note on BPM Data Structures

5.0 BPM BLOCK DIAGRAM DESCRIPTION

Please refer to Fig. 1 for reference.

5.1 Beam Position Detectors

There are on the average of nine detectors per BPM unit. As in Main Ring there is one at each quadrupole, measuring beam position in the quadrupoles focusing plane. Unlike Main Ring the detector is located upstream of the quadrupole. A discussion on the detector and its properties is found in:

FERMILAB ENERGY DOUBLER BEAM POSITION DETECTOR, Bob Shafer, et al., IEEE Transactions on Nuclear Science, Vol. NS-28, No. 3, June 1981, P 2290

5.2 RF Position Measurement Modules

The units labeled 'RF Modules' on the block diagram are the devices which convert the RF signals into analog position and intensity signals. Each detector has its own RF module associated with it. A discussion on these devices is found in:

AN RF BEAM POSITION MEASUREMENT MODULE FOR THE FERMILAB ENERGY DOUBLER, Bob Webber, et al., IEEE Transactions on Nuclear Science, Vol. NS-28, No. 3, June 1981, P 2323

Further information is contained in the BPM Design Note #1 and #4 mentioned earlier.

5.3 Analog Box

In order to function properly the BPM system must take the analog information generated by the RF modules and convert it into digital information which can be used by the BPM processor. It must also be able to perform this task in the two different modes discussed earlier; Snapshot mode and Flash mode. The Analog Box is the device which converts the analog information to digital words as well as providing control of the process.

Functionally the Analog box consists of two different components; the Daughter Card, of which there is one for each detector, and the Motherboard which provides a backplane for the daughter cards in addition to control circuitry.

5.3.1 Analog Box Daughter Card - The analog position and intensity signals from each RF module are brought onto the associated daughter card. The intensity signal is used in two ways; the most important is for triggering the sample and hold. For this purpose the intensity signal is applied to one input of a comparator. The other input is a DC voltage which can be set from

the host on a house by house basis. When the intensity signal passes from a 'non beam state' through the threshold, a gate is generated which applies the position and intensity signals to the storage capacitors of independent sample and hold amplifiers. The length of the gate is dependent on whether the accelerator is circulating batches or single bunches.

In Snapshot Mode the position signal is coupled directly through to a TRW 10 sec A/D where it can be read by the BPM processor.

In Flash Mode the position information is digitized and stored in a separate latch. The S/H intensity signal is sent through a logarithmic amplifier and coupled via a FET switch to the same D/A, where its value is latched. Thus both position and intensity data are available to the BPM processor.

5.3.2 Analog Box Motherboard - The motherboard acts as an interface between the daughter cards and multibus hardware, as well as providing general services to the daughter cards. In particular it:

- o Provides address decoding so that the BPM processor can access position and intensity data.
- o Contains a storage register and a D/A so that the INTENSITY THRESHOLD 8 bit word can be stored, converted and routed to all daughter cards.
- o Controls the timing of the Flash data taking process.
- o Provides control signals for the timing of the Snapshot data taking process. (Snapshot timing is controlled by Multibus hardware)

5.3.3 Further Information On Analog Box - BPM Design Note #5 contains a detailed description of the Analog Box. A procedure for the alignment of the Daughter Cards can be found in BPM Design Note #6. A future BPM Design Note will describe the test procedure used to measure the calibration constants and tolerances of the Analog Box, and the results of the measurements.

5.4 Multibus Crate

The BPM Multibus crate contains six cards. Two of these are standard cards found in other doubler systems; the MOBO which is the Multibus end of the Camac to Multibus interface, and the MSC 8004, a processor card made by Monolithic Systems Corporation which contains the standard Accelerator Division software for communication with the host computer.

The four additional cards have been designed specifically for the BPM system. They include; a second processor board, an Analog Box controller board, a timing controller and 'external device bus' driver board, and a clock decoder board. A brief description of the four boards follows.

5.4.1 BPM Processor Board (PRO) - The BPM system is unique in the doubler controls system in that it contains two processors. The decision was made to use two processors based on the importance of the snapshot oriented protection scheme, and the speed at which the data needs to be manipulated. The majority of tasks performed by the BPM Processor have been outlined in sections 3.1.2, 3.2, 3.3 and 3.4.

For the BPM Processor there are two distinct divisions of time; the time when beam is in the doubler, and the time when beam is not. The boundaries on these divisions of time are defined by doubler clock events. When the BPM detects a 'Prepare for Beam' clock event the response of the BPM processor is to begin the snapshot data frame, whether there is really any beam in the doubler or not. At this time all communication with the outside world is terminated until a 'Beam Off' clock event is detected, or an abort occurs. (Actually there are several exceptions to this rule, the most notable is that BPM clock events generate interrupts.)

5.4.1.1 BPM Processor Board Hardware - The PRO is a rather straightforward processor board since it was designed for a specific purpose. It contains a Z80A CPU chip, one socket for ROM and one socket for RAM. Most of the memory it uses is on the 8004 processor board. It also contains a Direct Memory Access Chip (Zilog ZB410 DMA) which is used only for accessing snapshot frame data from the analog controller board, and a Counter/Timer Circuit chip (Zilog ZB430 CTC) used for keeping track of time, and generating interrupts. The PRO also contains bus priority logic since it must be able to assert itself as bus master in the presence of the 8004 processor.

5.4.1.2 BPM Processor Board Software - The software in the BPM processor will be discussed in a future BPM Design Note. Its key features are discussed here, but before doing so a few words should be said about the code in the B004 processor.

The B004 is used by the BPM system as an I/O processor. All communication between the host and BPM is handled by the B004. The B004 maintains tables defining all the data structures which can be used for communication. When the host sends down data for the BPM the B004 places it in memory, and notifies PRO that the tables contain new data. When the host requests data the B004 returns the data from its memory. If the PRO has reason to alert the host of some condition, i.e. an abort or alarm condition has been detected, it will generate an interrupt to the B004, and the B004 will proceed with the communication to the host.

Having discussed what the PRO software doesn't do we will summarize what it does do. Other than initialization routines the PRO is interrupt driven. For the purposes of this discussion we will break down the interrupts into two categories: interrupts generated by doubler clock events and the interrupt generated by the DMA chip.

Interrupts generated by doubler clock events:

- o MASTER RESET - This event resets the time used in the time stamps of the data frames.
- o PREPARE FOR BEAM - This event precedes the injection of beam by several hundred milliseconds. The PRO responds by checking to see if any new data has been downloaded from the host. If it has, PRO transfers it from the B004 memory to internal memory or to hardware registers, whichever is applicable. Then the Snapshot Data Frame is enabled, and the Flash permit is set.
- o BEAM OFF - Snapshots are turned off and the Flash permit is removed.
- o HIGH FIELD - The PRO sets its pointers to the high field limits.
- o LOW FIELD - the PRO sets its pointers to the low field limits.
- o WRITE PROFILE MEMORY - See Section 3.3.
- o CLEAR PROFILE MEMORY - This event sets the profile pointer back to the first address.

- o FLASH TRIGGER - See Section 3.2.
- o WRITE DISPLAY FRAME - See Section 3.4.

Interrupt from DMA chip:

- o DMA SERVICE REQUEST - This interrupt originates with the hardware and occurs at the end of every Snapshot Frame Cycle. The response of the processor is outlined in Section 3.1.2

5.4.2 Timing And External Device Board (TEX) - The TEX board has two main functions. The first of these is that it provides access to a system bus which connects the processor to two of the blocks on the block diagram which haven't been mentioned yet; the Test Interface Module (TIM), and the Beam Loss Monitor system (BLM). These are discussed in Sections 5.5 and 5.6.

The second function of TEX is the timing for the Snapshot Frame. TEX instructs the Analog Box to arm itself for a measurement, and when the measurements are latched on the Daughter Cards, TEX controls the reading of the data onto the ACT (see next Section). Furthermore TEX keeps track of the length of the Snapshot Frame Cycle, and at the end of the frame cycle initiates the DMA transfer.

5.4.3 Analog Controller Board (ACT) - The Analog Controller Board handles the data manipulations during the Snapshot Frame. The data from each measurement is transferred to ACT where it is added to data from the previous measurements. During this process the card keeps a record of all channels which have reported valid data enough times to complete the requested averaging. At the end of the Snapshot Frame Cycle TEX initiates the DMA transfer and at that time the averaging is done by ACT.

5.4.4 Clock Decoder Board (CLK) - In addition to providing some support services this board receives the energy doubler clock, determines if the encoded event is meant for the BPM system, and if so interrupts PRO.

Information on the Multibus boards designed for the BPM system is being prepared and will become BPM Design Notes.

5.5 Test Interface Module (TIM)

The Test Interface Module is not a part of the Beam Measurement System per se, but is available to the processor via the external device bus for system tests whenever the system is not taking snapshots (that is when beam is not in the doubler). Three categories of tests can be done:

- o Power Supply Tests - All the voltages in all RF modules as well as those in the Analog Box are shipped to TIM which acts as an MADC to digitize them and make them available to the processor. Only the Multibus and BLM voltages are not monitored via TIM.
- o Cable Tests - TIM can test the continuity of the cables that run from the detector in the tunnel up to the RF modules in the service building. This test checks for shorts as well as opens.
- o RF Tests - The RF modules as well as the analog circuits are verified by this test. TIM generates a 53 MHz signal with the appropriate notch and applies this signal to the inputs of the RF modules. Furthermore there are 6dB attenuators which can selectively be switched into either input. Thus a measurement of the response of the system at three different points (0dB and +/- 6dB) can be made.

A BPM Design Note is also being prepared on the Test Interface Module.

5.6 Beam Loss Monitor (BLM)

The Beam Loss Monitor system for the energy doubler is controlled and monitored through the BPM processor. The communication link is the External Device Bus, shared with the Test Interface Module. Several features of the system will be noted at this time:

- o Each BLM system will support up to 12 tunnel loss detectors which are argon filled ionization chambers. The layout of the BLM system is similar to the Analog Box with daughter cards and a motherboard.
- o Each daughter card contains a logarithmic integrator with a time constant of 63 milliseconds. This is similar to the time constant with which the superconducting magnets respond to beam losses. Therefore each daughter card produces a voltage which represents the likelihood that magnets in the

area will quench.

- o The range of the system is .01 Rad/sec to 100 Rad/sec for continuous losses, and .001 Rad to 10 Rad for instantaneous losses.
- o Once data structures are properly downloaded each BLM system is capable of directly (without the BPM processor) generating an abort signal if any one of the detectors senses loss greater than a house-wide abort limit. The limit is high field/low field dependent as in the BPM system.
- o A second set of limits can be used for alarm purposes. Again in this case the limits apply to all 12 detectors and there is one for high field and one for low field.
- o Detectors can be individually masked off so that they don't generate alarms or aborts. In addition a BLM can be entirely masked off.
- o Digital readout of all 12 detectors, BLM power supply voltages, and BLM high voltage for the ion chambers is available via memory mapping in the BPM system.
- o The high voltage supply is settable from the host.
- o The analog output from any detector can be routed to a standard MADC channel for plotting. (One at a time from a given BLM)

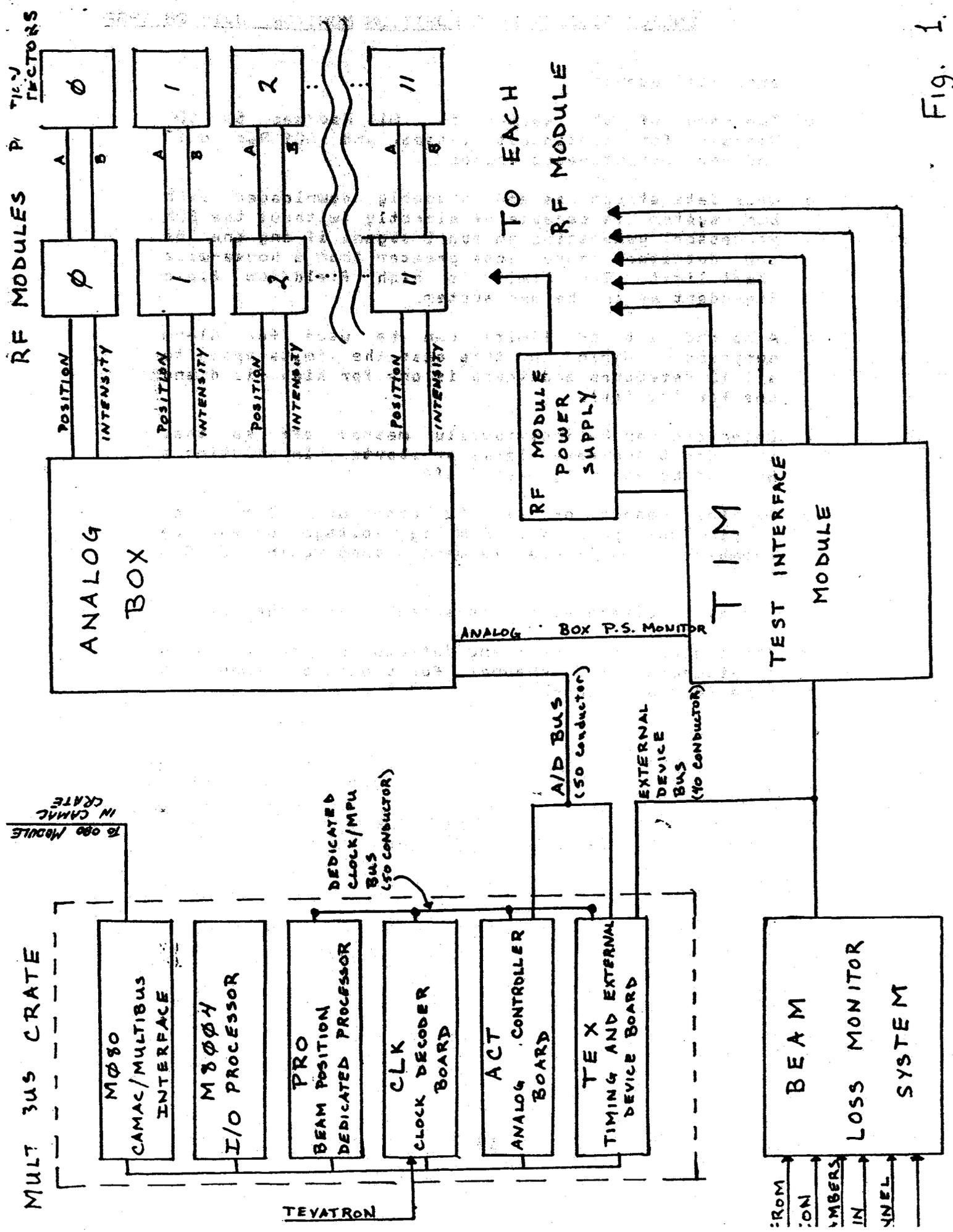


Fig. 1.

July 27 1982

TO: DISTRIBUTION
FROM: Rod Gerig
SUBJECT: BPM Design Notes

This note brings up to date the note of Nov. 5, 1981 which introduced the series of documents known as Beam Position Monitor Design Notes. The file of master copies remains in the care of Marion Richardson.

Design notes which are complete or nearly so:

1. Expected Calibration and Calibration Tolerances of BPM (R. Shafer)
2. Wire Measurement and Detector Performance (Shafer, R. Webber)
3. Interpretation of E.D. Beam Position Detector Performance (Shafer)
4. Measurement of rf Module Calibration Constants and Tolerances (D. Martin)
5. Description of Analog Box (S. Bristol, R. Gerig)
6. Alignment Procedure for Analog Box (Bristol)
7. BPM Diagnostic Software Modules (A. Baumbaugh)
8. BPM Scope, Loop Builder with Examples (Baumbaugh)

Design Notes which are not yet written, but are anticipated:

- a. Measurement of Analog Box Calibration Constants and Tolerances (Bristol, Gerig)
- b. Alignment and Calibration Procedure for rf Modules (Martin)
- c. General Description of rf Modules (Webber)
- d. Cabling used in BPM system (Webber)
- e. BPM Test Interface Module (Webber)

