Minutes, 3/04/04 Tevatron BPM Upgrade Meeting
Stephen Wolbers

This set of minutes, and all future minutes, are or will be deposited in the Beams Document Database as document number 792.

The agenda as announced consisted of:

1. Timing/diagnostics system and crate layout.

The transparencies shown are found in Accelerator Division document database #1061.

Mark Bowden went through the transparencies. I did not take detailed notes but will hit the highlights here.

- There was a question about the UCD cards that plug into the MVME processor boards. Are they ordered? Are 31 ordered? Should 31 be ordered?

- The overall design for the crate is to use the back of the crate for some of the cables. This leads to some changes in the crate backplane compared to the original design. This is still a proposal and there are many questions about cable runs, crate design, cooling, etc.

- The timing (clock generator) is an issue. The stability of the Echotek card needs to be understood. If an alternate system can produce a better stability then it will be acceptable.

- The diagnostic design shows signals being generated (53 MHz) and injected through one end of a BPM plate and read in at the other end. Relays are used to control this. How reliable are the relays? What is the strategy for signal injection and readout? Is there any requirement for signal injection directly to the front-end of the EchoTek board? We must ensure that reflections at cable transitions (RG8->jumper cables) etc. are small.

- Bob suggests that a crate be mocked up.

- We did not come up with a list of action items but it is likely that the major issues are obvious. We are not yet able to release the purchase requisition for the VME crates until we have a final understanding of the crate layout.

- We should get together reasonably soon to review and update status of this work.

3. AOB.