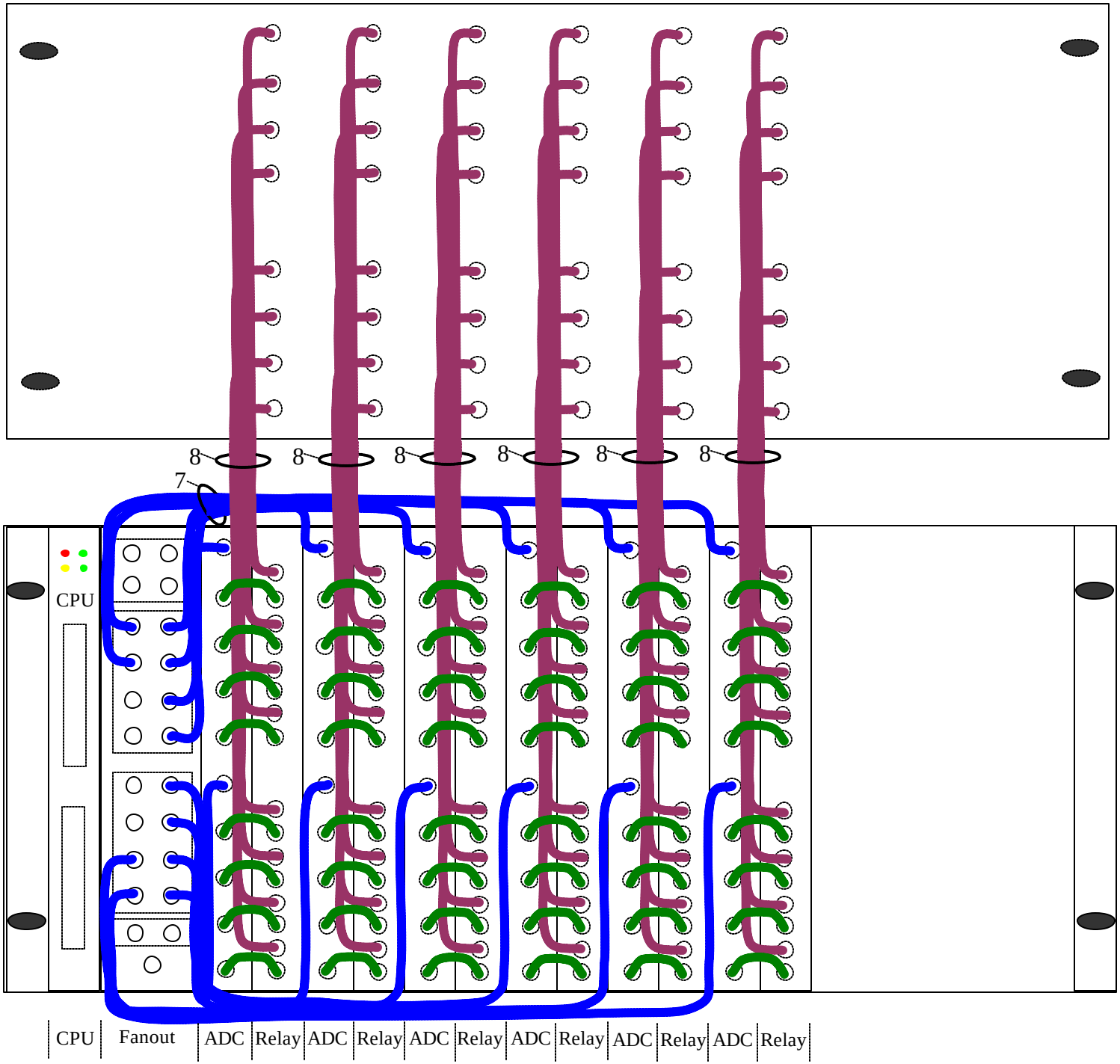
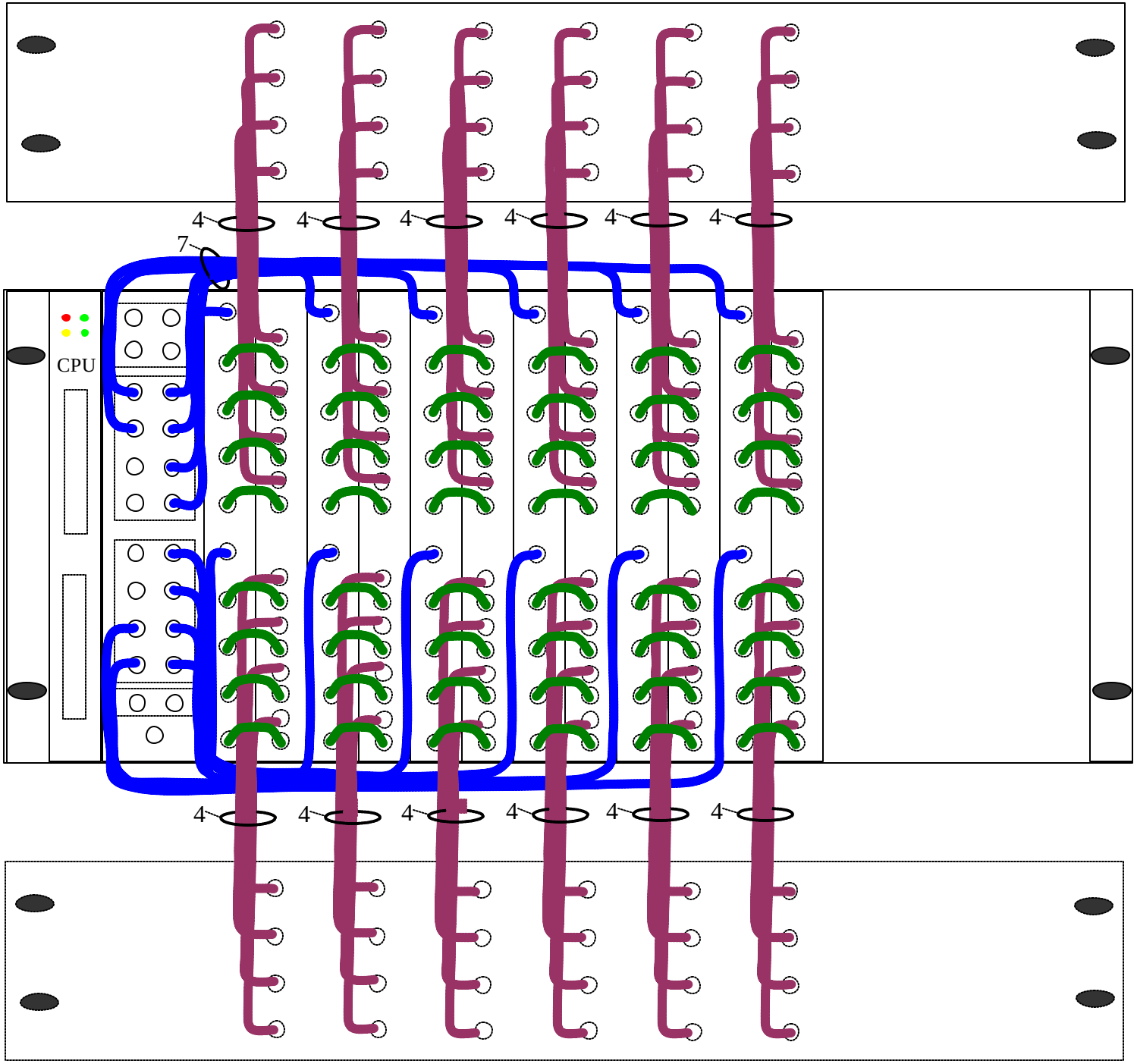
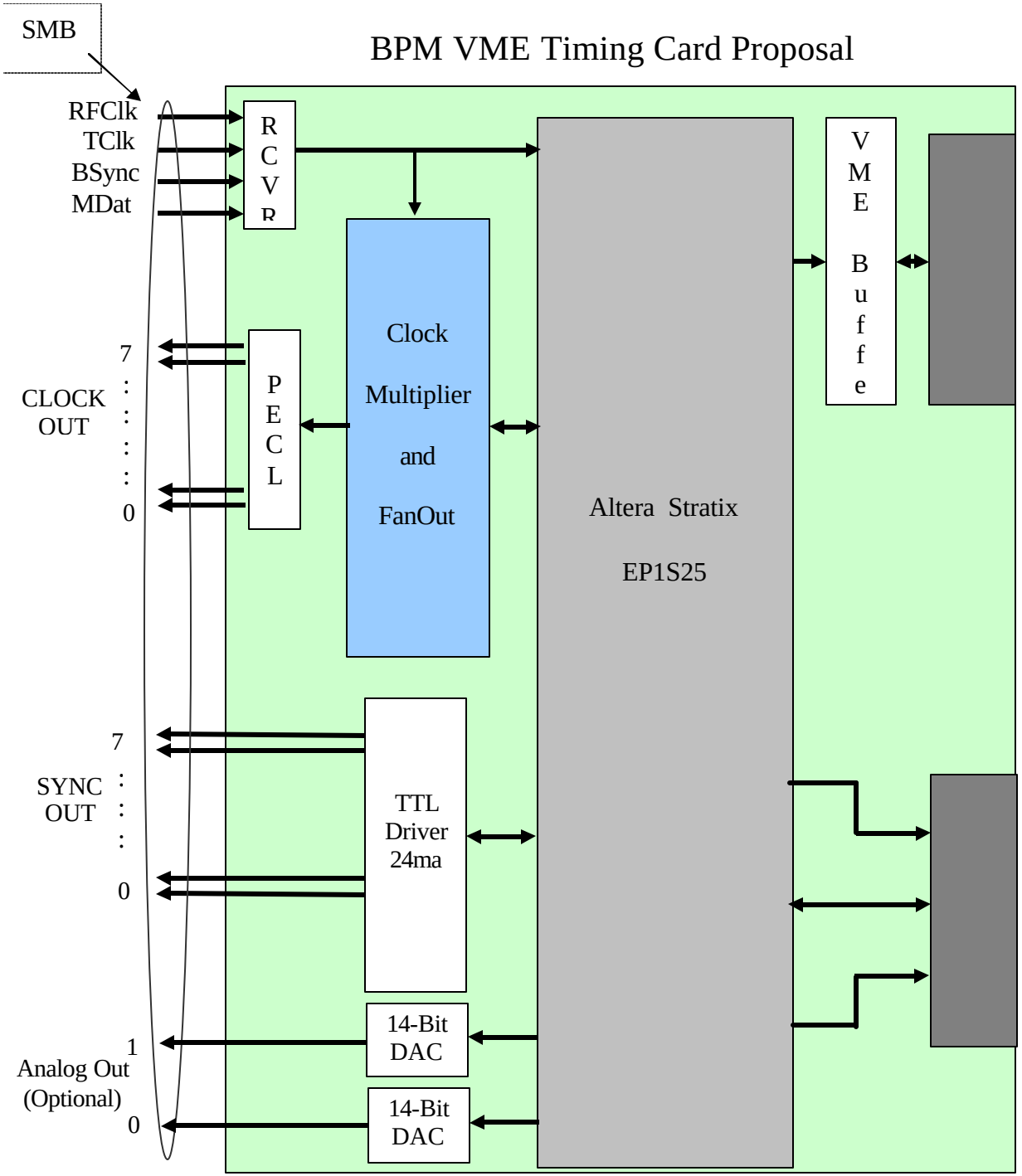
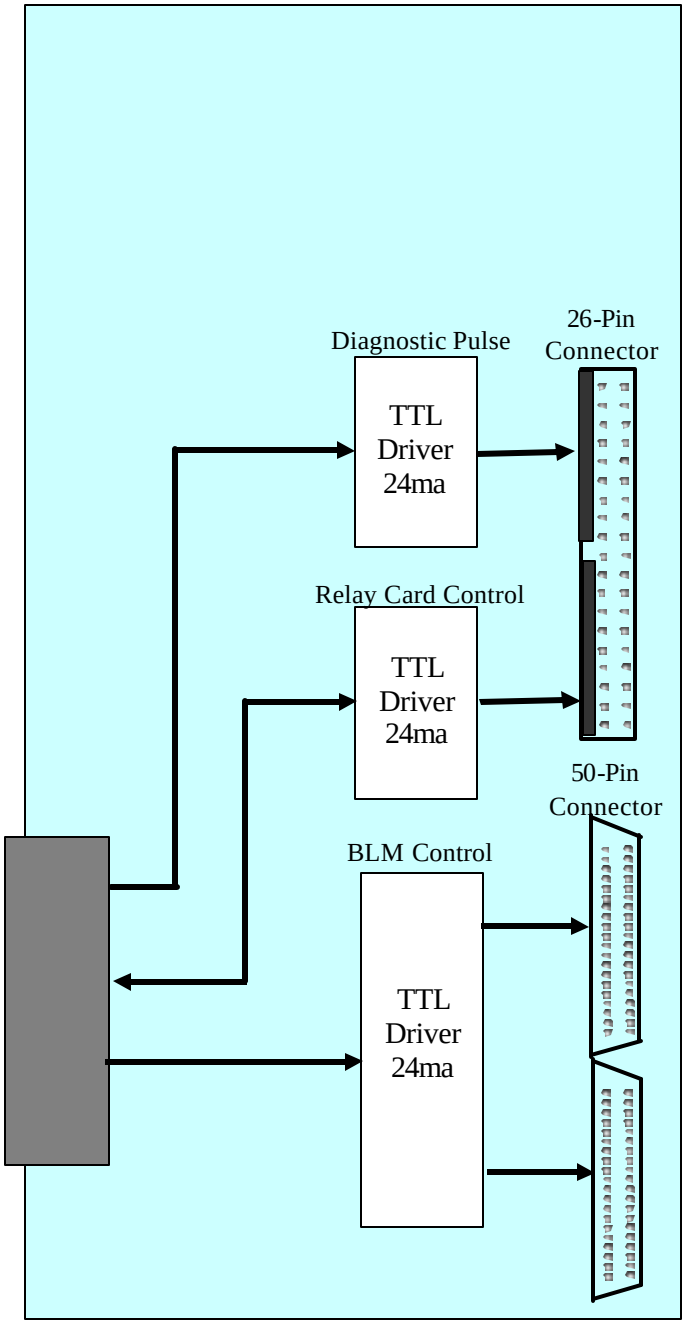
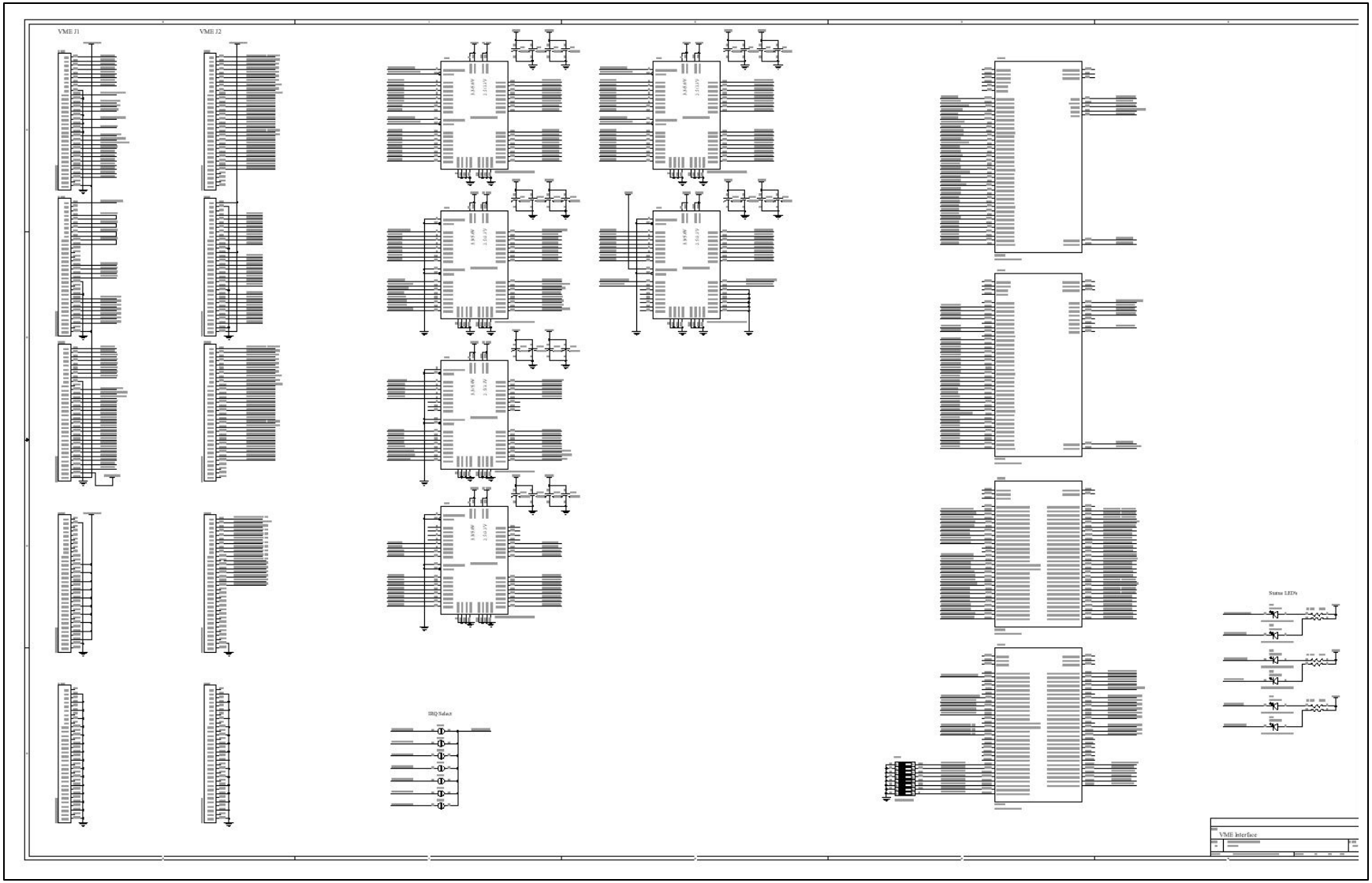

8
8
8
8
8
8
7
CPU
CPU
Fanout
ADC
Relay
ADC
Relay
ADC
Relay
ADC
Relay
ADC
Relay
ADC
Relay


4
4
4
4
4
4
7
CPU
4
4
4
4
4
4


BPM VME Timing Card Proposal
SMB
RFClk
TClk
BSync
MDat
RCVR
Clock Multiplier and FanOut
PECL
CLOCK OUT
7
0
Altera Stratix EP1S25
VME Buffe
SYNC OUT
7
0
TTL Driver 24ma
14-Bit DAC
14-Bit DAC
Analog Out (Optional)
1
0


VME Transition Card
Diagnostic Pulse
TTL Driver 24ma
26-Pin Connector
Relay Card Control
TTL Driver 24ma
50-Pin Connector
BLM Control
TTL Driver 24ma

Timing Fanout Card Status
(Preparing For Internal Design Review)



Timing Fanout Card Firmware Status

1) Altera IP interface code is being converted to VHDL
    a. Debugging & Simulating (Aldec & Altera)
    b. Expected to be completed next week

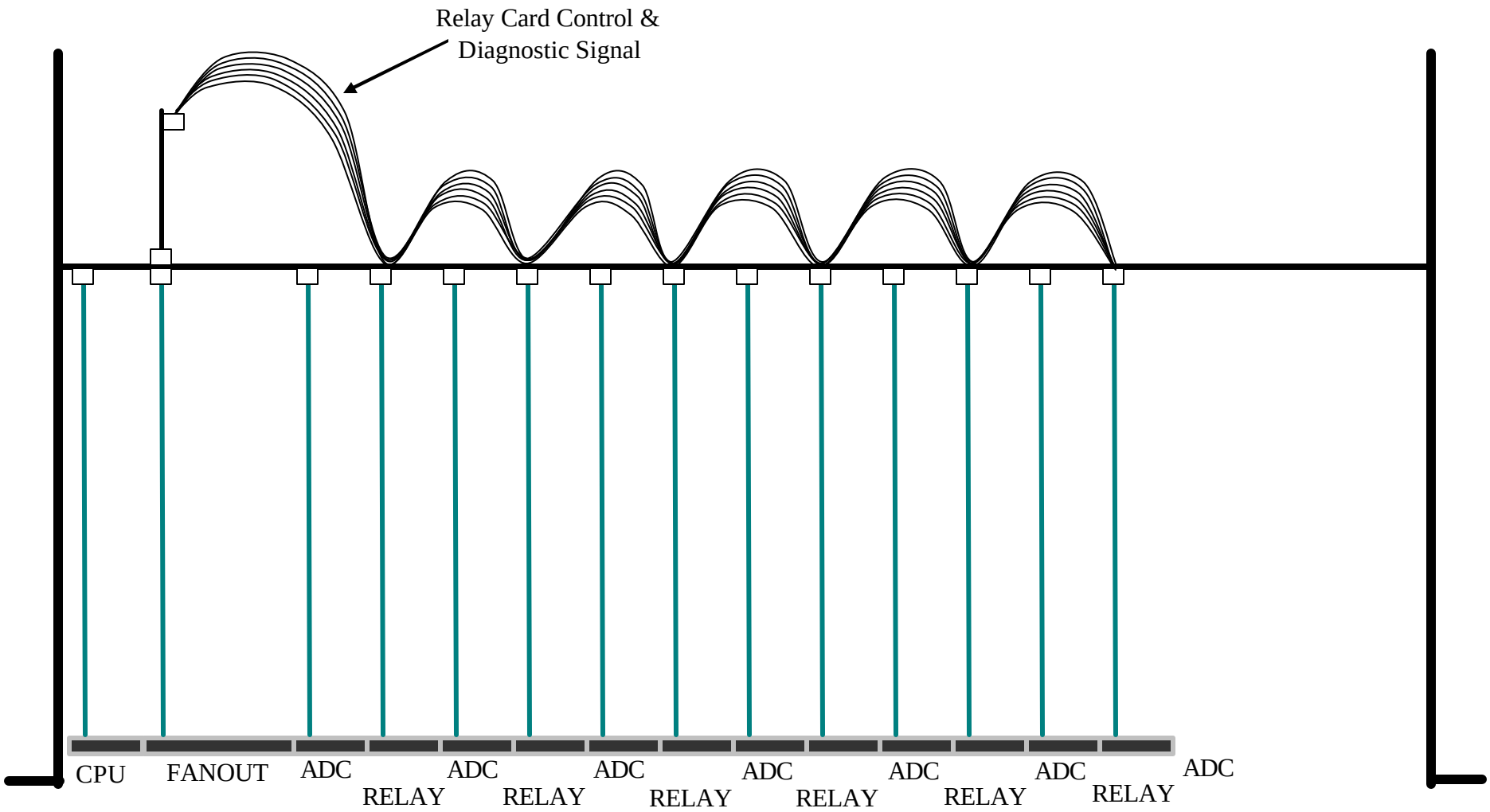
2) Altera Clock decoding firmware conversion
    a. Starts next week
    b. Completion anticipated by May 28

3) VME Interface Firmware
    a. Completion anticipated by June 8

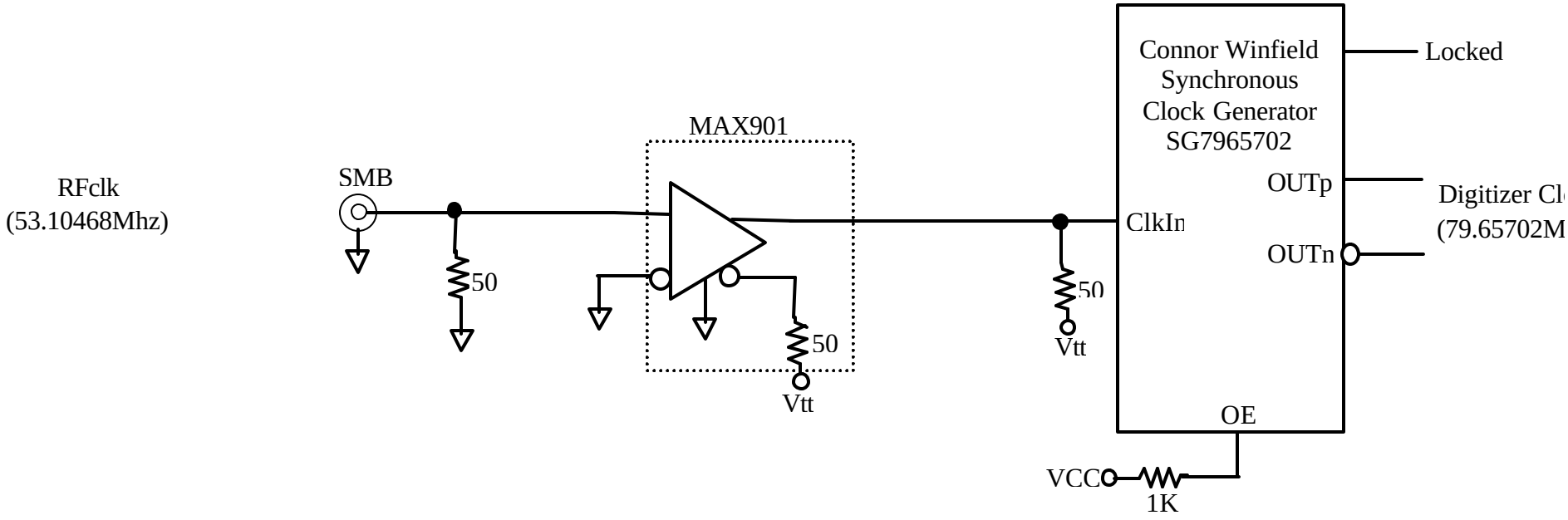
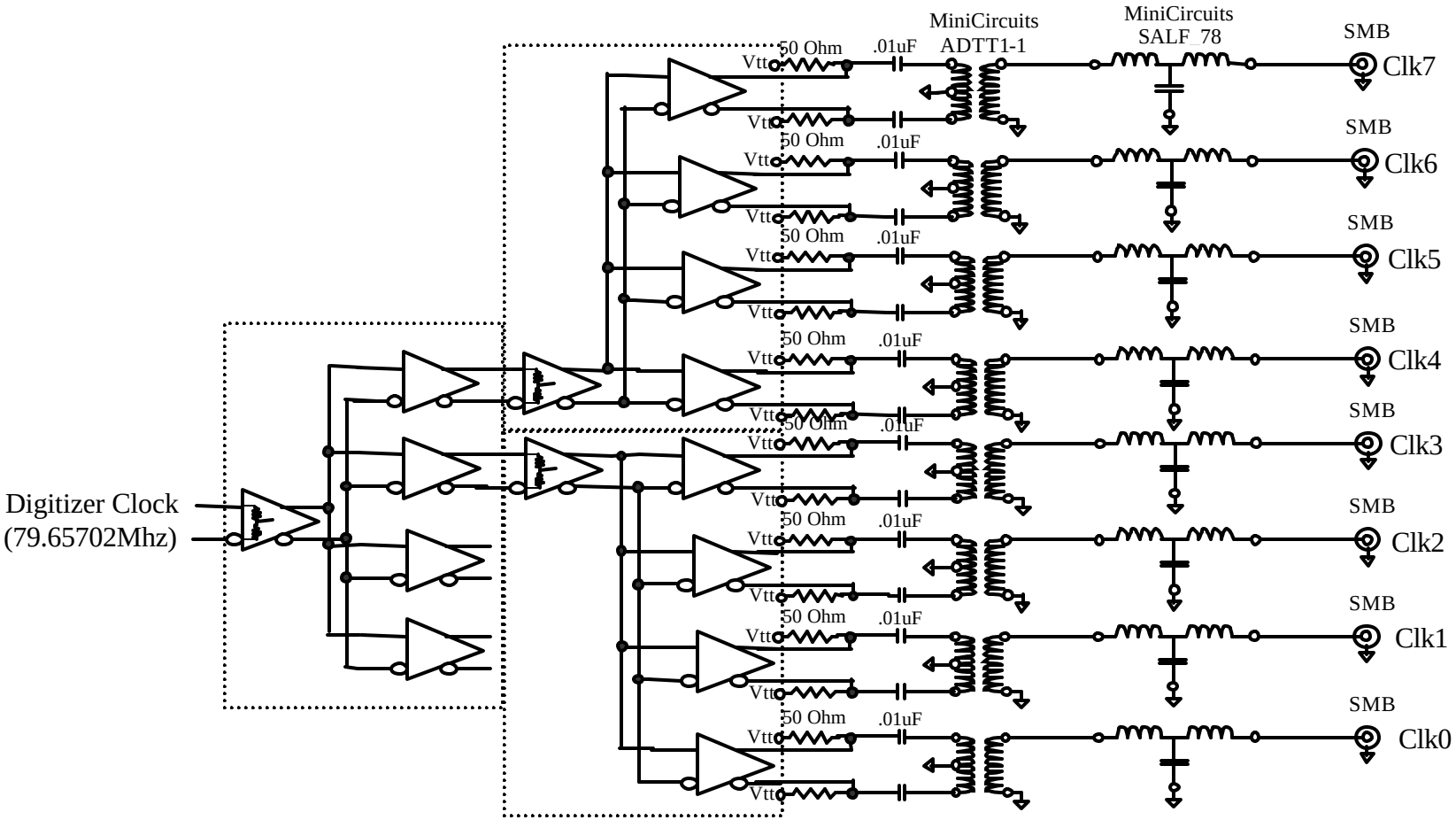
4) BLM Control Firmware
    a. Completion anticipated by June 22

5) Relay Control Firmware
    a. Completion anticipated by June 30

Top View of VME Crate
Showing Timing Fanout Card
Control Cable Connections to Relay Card



Clock Generation
(79Mhz)



Clock Fanout Section