

Tevatron IPM Project

# QIE for IPM Front End (QIFE) Board

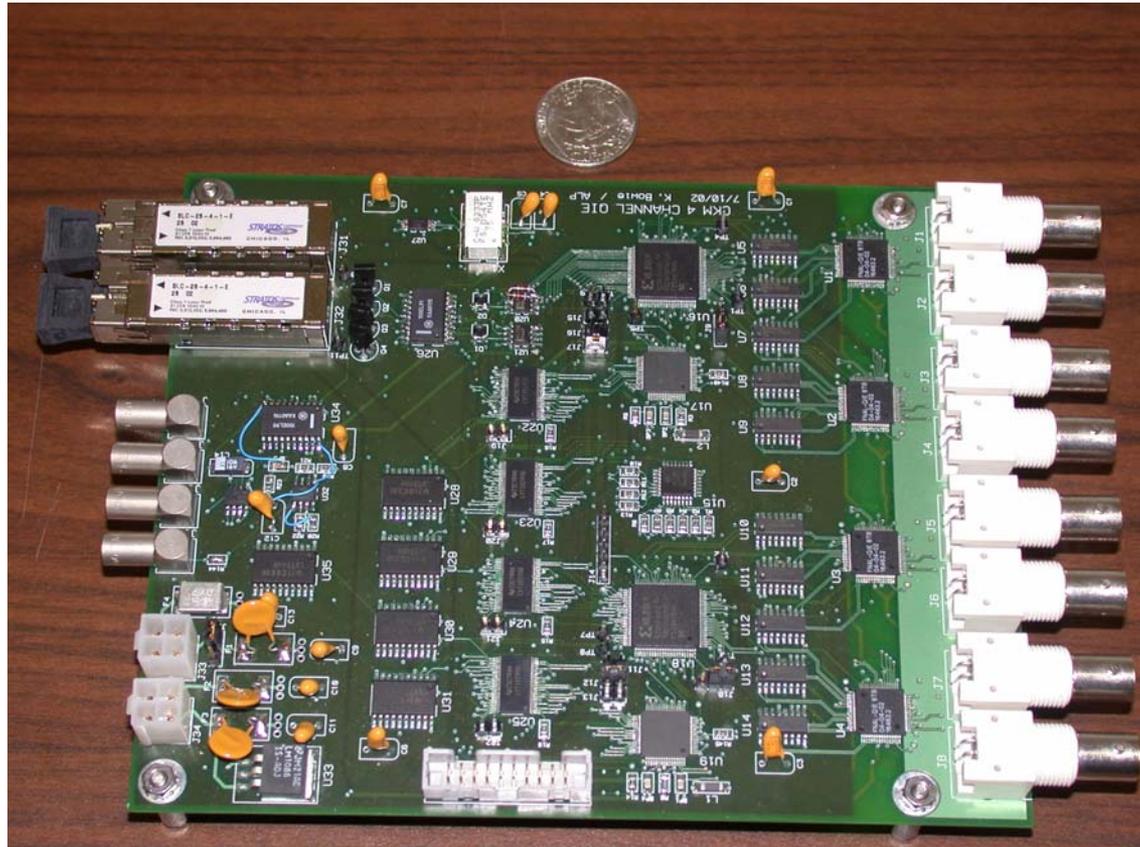
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# QIFE Functional Description

- Multiplexes and serializes integrated charge data
- Uses proven architecture to shorten development process (derived from QIE testing board)
- Provides at least 8 channels per board at 2RF/7 data throughput
- Demonstrates a nominal level of radiation tolerance for front end electronics
- Provides a mechanism for correlating proton and antiproton bunch information with the integrated charge data.

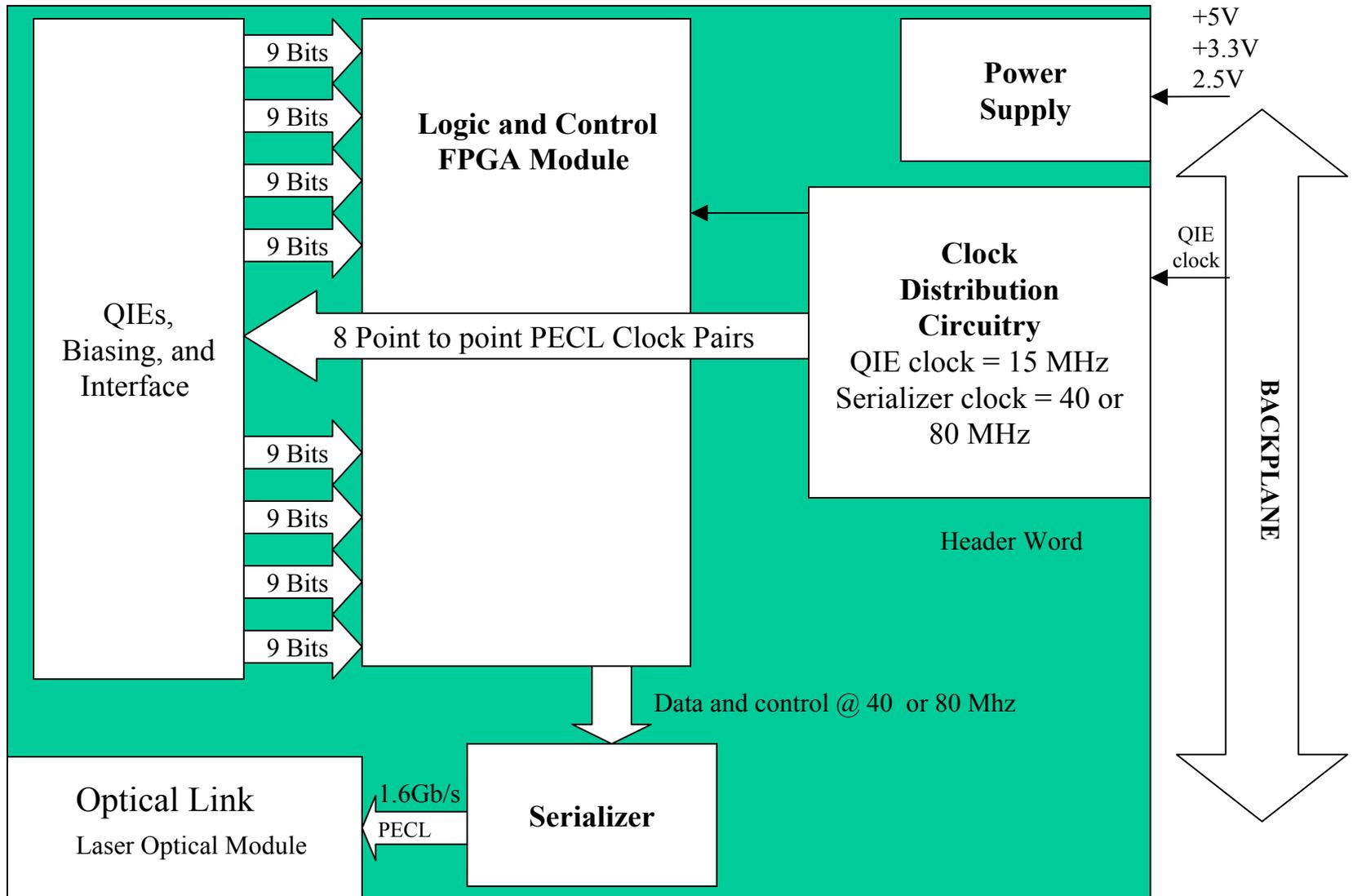
# QIE Testing Board



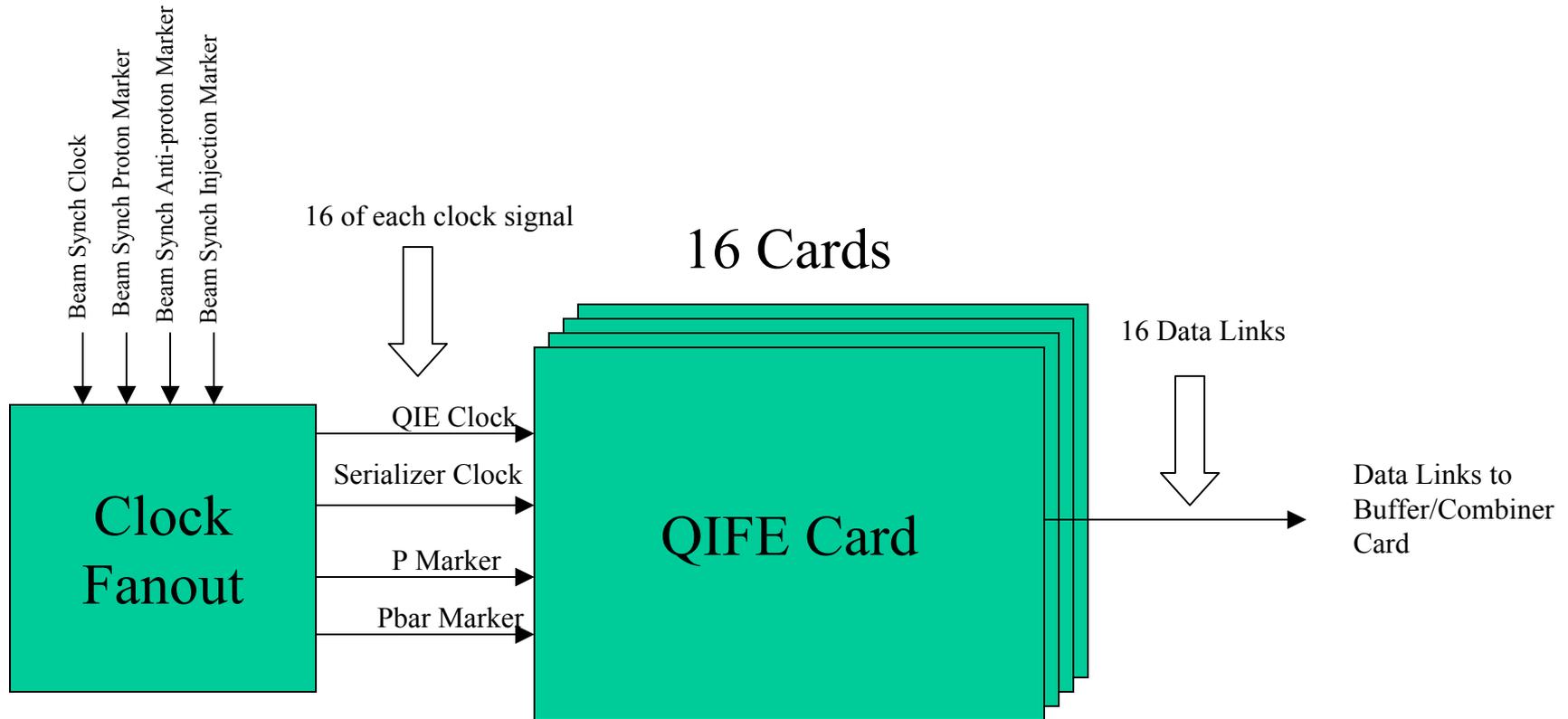
# Changes from Testbench Board

- More channels (8 or 10 compared to 4)
- Higher data rate (1.6Gbps compared to 700Mbps)
- Uses separate clocks for QIE sampling and serialization
- Must be rad tolerant to 20 Krad

# QIE for IPM Front End Board Block Diagram



# Front End Subsystem Block Diagram



# Performance Requirements

- Signal resolution (charge):  $\sim 1\text{fC}$
- Sampling frequency: 15 MHz
- Noise level (RMS):  $\sim 1/2$  LSB
- Distance to detector: 5 feet
- Data link transmission distance: 300+ feet
- Radiation tolerance level: SEL immunity and board failure  $\geq 20$  krad

# Minimum Data Rate

- Minimal functionality:
  - At least 8 QIEs per board
  - 5 header bits:
    - Proton marker
    - Antiproton marker
    - QIE mode (3 modes  $\rightarrow$  2 bits)
    - Data/ no data tag
  - Integration done at  $2RF/7$  frequency (15 MHz)
  - Amount of data from single integration cycle: 63 bits
    - 8 QIEs \* 7 bits of integration data  $\rightarrow$  56 bits
    - 2 Cap ID bits shared between all 8 QIEs  $\rightarrow$  2bits
    - 5 additional header bits
  - Minimum data payload bit rate:  $63 \text{ bits} * 15 \text{ MHz} = 945 \text{ Mbps}$
  - Transmission protocol overhead: 25%
  - $\rightarrow$  1.2 Gbps to fiber for minimum functionality

# Serial Link Implementations

- CERN Gigabit Optical Link (GOL) ASIC based design
  - Advantages:
    - Initially preferred for radiation tolerance
  - Disadvantages:
    - Device availability concerns
    - Limited to 8 QIE channels per board (1.6Gbps max)
- COTS Serializer (TLK2501) based design
  - Advantages:
    - Readily available
    - Very mature chip (all design issues should be documented)
    - Possibility to move to 10 or more channels per board (2.5 Gbps max)
  - Disadvantages:
    - Testbeam tests showed more susceptibility to single event-type errors (bit errors, losses of lock) than GOL
    - May require additional testbeam reliability studies be done for IPM project

# Spare Bandwidth Available

- GOL ASIC: 1.6 Gbps capable transmitter
  - 1.6 Gbps → 1.28 Gbps data payload
  - 945 Mbps used on QIE data and essential header markers
  - Available bits per integration cycle within GOL bandwidth capabilities:
    - Bits = (Max data payload – Used QIE payload) / integration frequency  
→ 22 additional bits of information available for each integration period (after QIEs and 5 marker bits)
- TLK2501: 2.5 Gbps capable transmitter
  - 2.5 Gbps → 2.0 Gbps data payload
  - 945 Mbps used on QIE data and essential header markers
  - adding additional QIEs to data stream adds 105 Mbps each
  - Using 10 QIEs per board: available bits = 56 additional bits per integration cycle

# How to use spare data bandwidth?

- Proton and pbar bunch counters
- Turn counters
- Integration cycle counters
- Serializer clock cycle counters

Any of these counters might be useful for debugging

# Radiation Tolerance

- Already tested for CERN CMS:
  - QIE8 chips
  - LVDS receivers
  - Antifuse FPGAs
  - GOL serializer
  - PECL drivers
  - PECL to TTL converters
- Rad tolerant designs guaranteed by manufacturer:
  - Linear regulators
  - Crystal oscillators
- Promising devices requiring further tests (possibly testbeam)
  - COTS serializer (TLK2501)
  - Reconfigurable FPGAs (Xilinx and Altera testing done elsewhere looks promising)

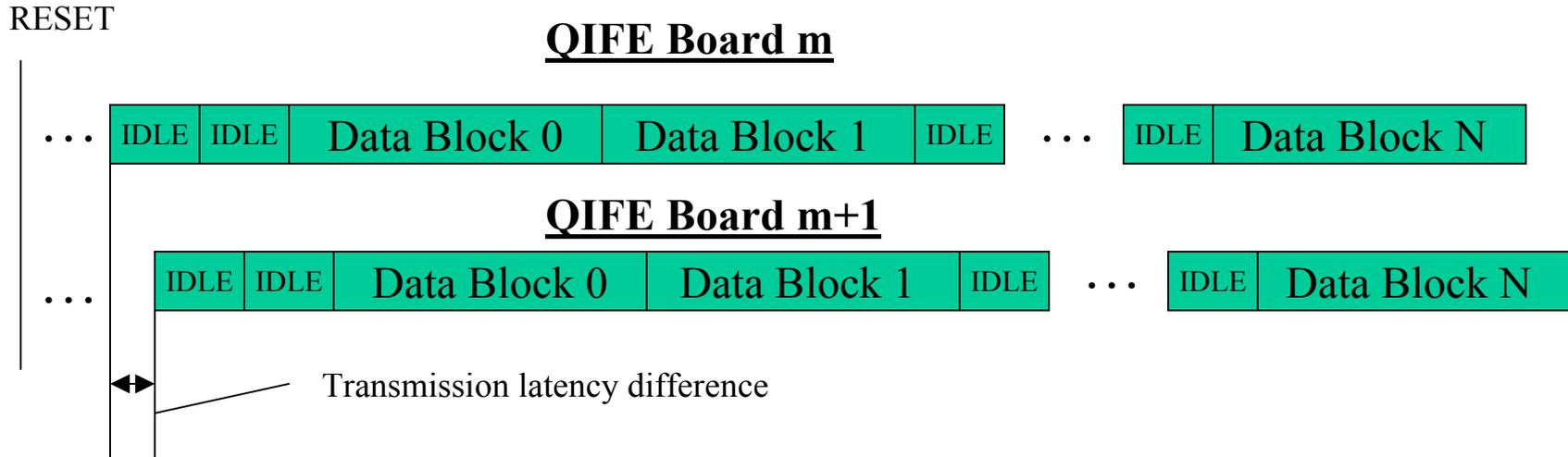
# Extra Slides

# Data Stream

## Implementation Concerns

- Need fixed block length (unambiguous decoding requirement)
- IDLE characters between blocks may be arbitrarily long
- Latency differences between high speed serial data links on different QIFE boards must not exceed four  $2RF/7$  clock cycles (Data synchronization requirement)

# Data Link Frames



- There will be transmission and receive latency differences between QIFE boards
- If the sum of these latency differences were to exceed four integration cycles, then QIE Cap ID is not sufficient to identify charges integrated during the same interval
- Data sheet parameters suggest this should not be an issue, but might require validation.

# TLK2501 COTS SERDES

## Sample Data Block Format (Minimal Header)

