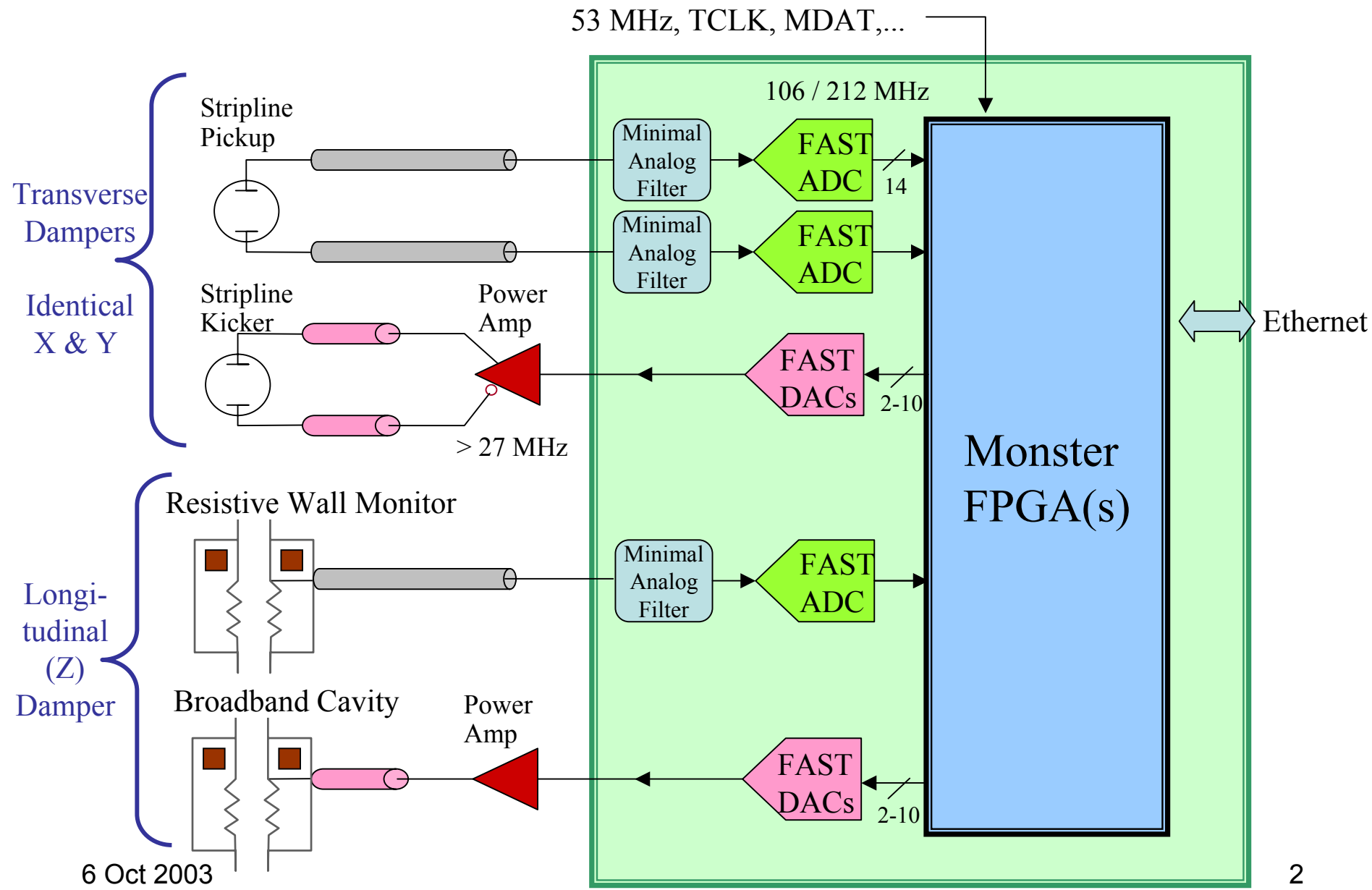
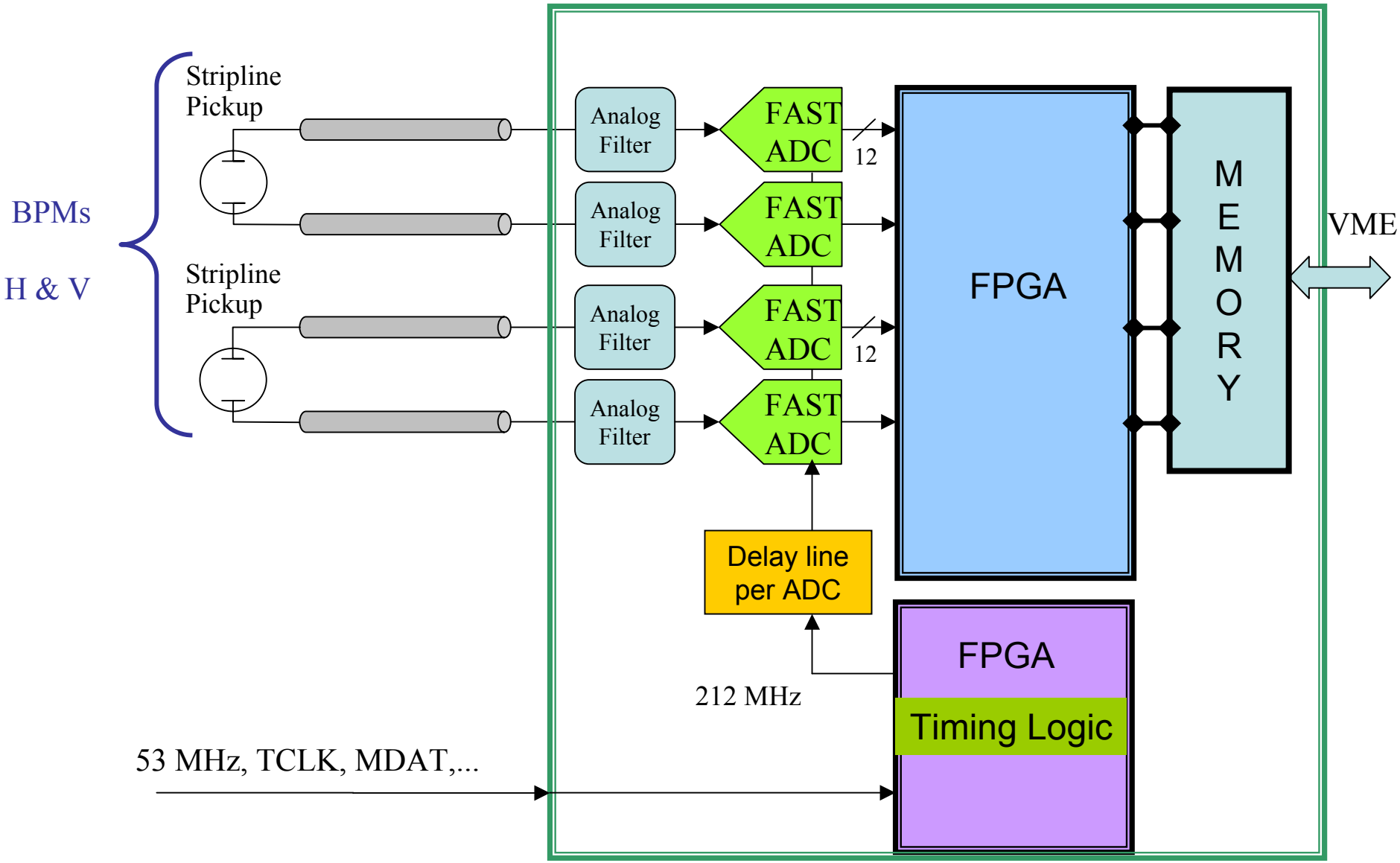
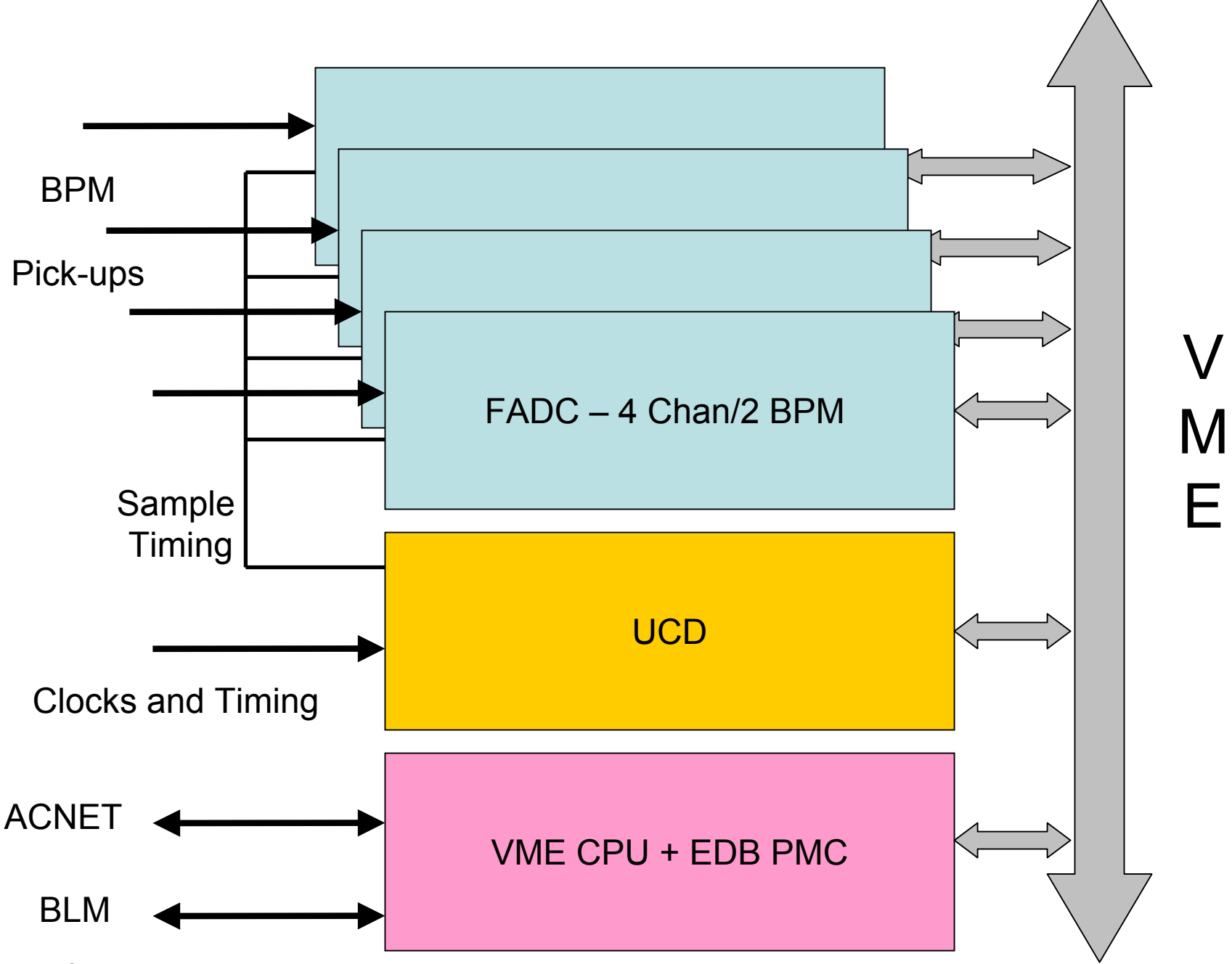
Make a BPM out of a Damper?

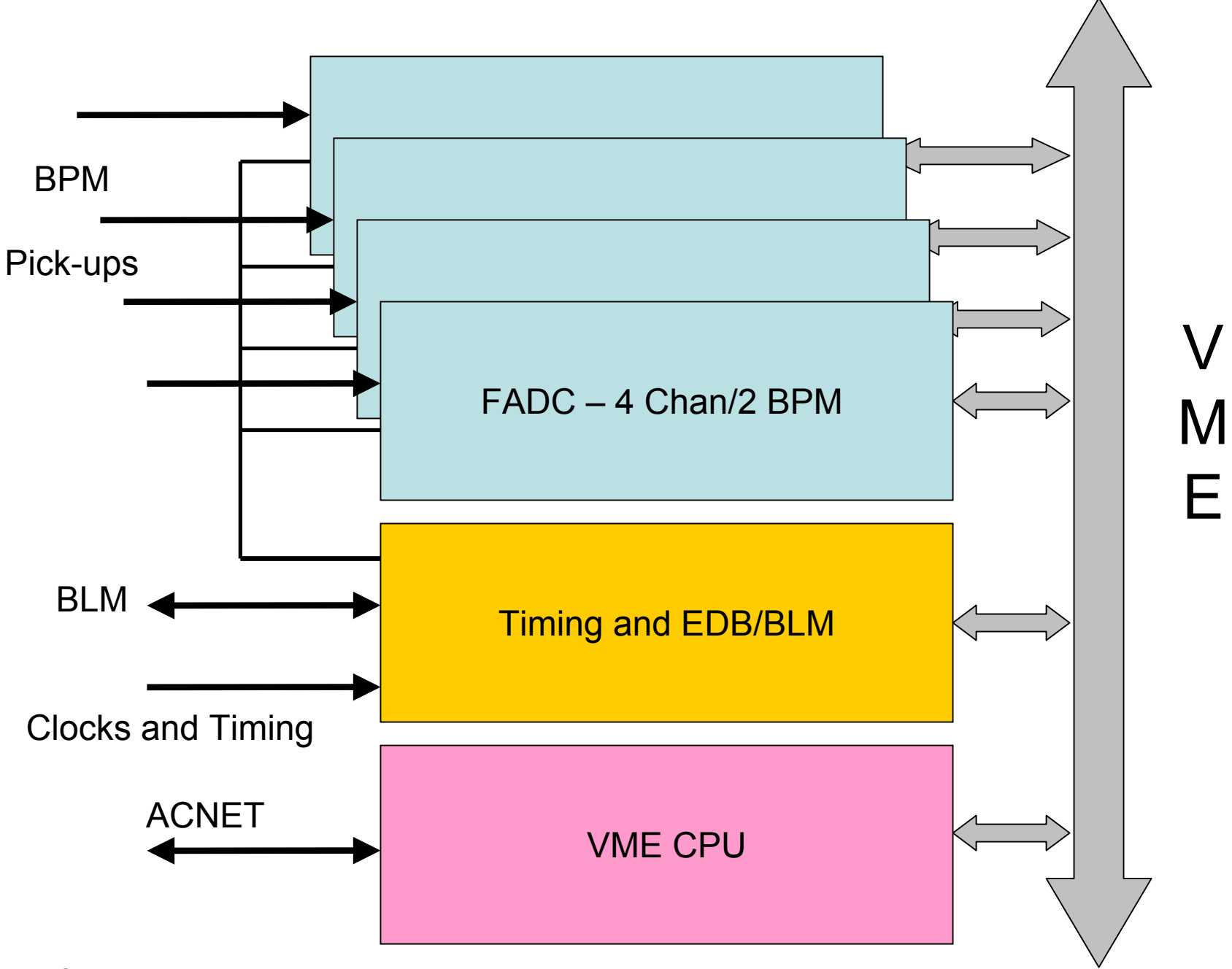
Digital Damper



Damper -> BPM


BPMs
H & V
Stripline Pickup
Stripline Pickup
Analog Filter
Analog Filter
Analog Filter
Analog Filter
FAST ADC
FAST ADC
FAST ADC
FAST ADC
12
12
FPGA
MEMORY
VME
Delay line per ADC
212 MHz
FPGA
Timing Logic
53 MHz, TCLK, MDAT,...

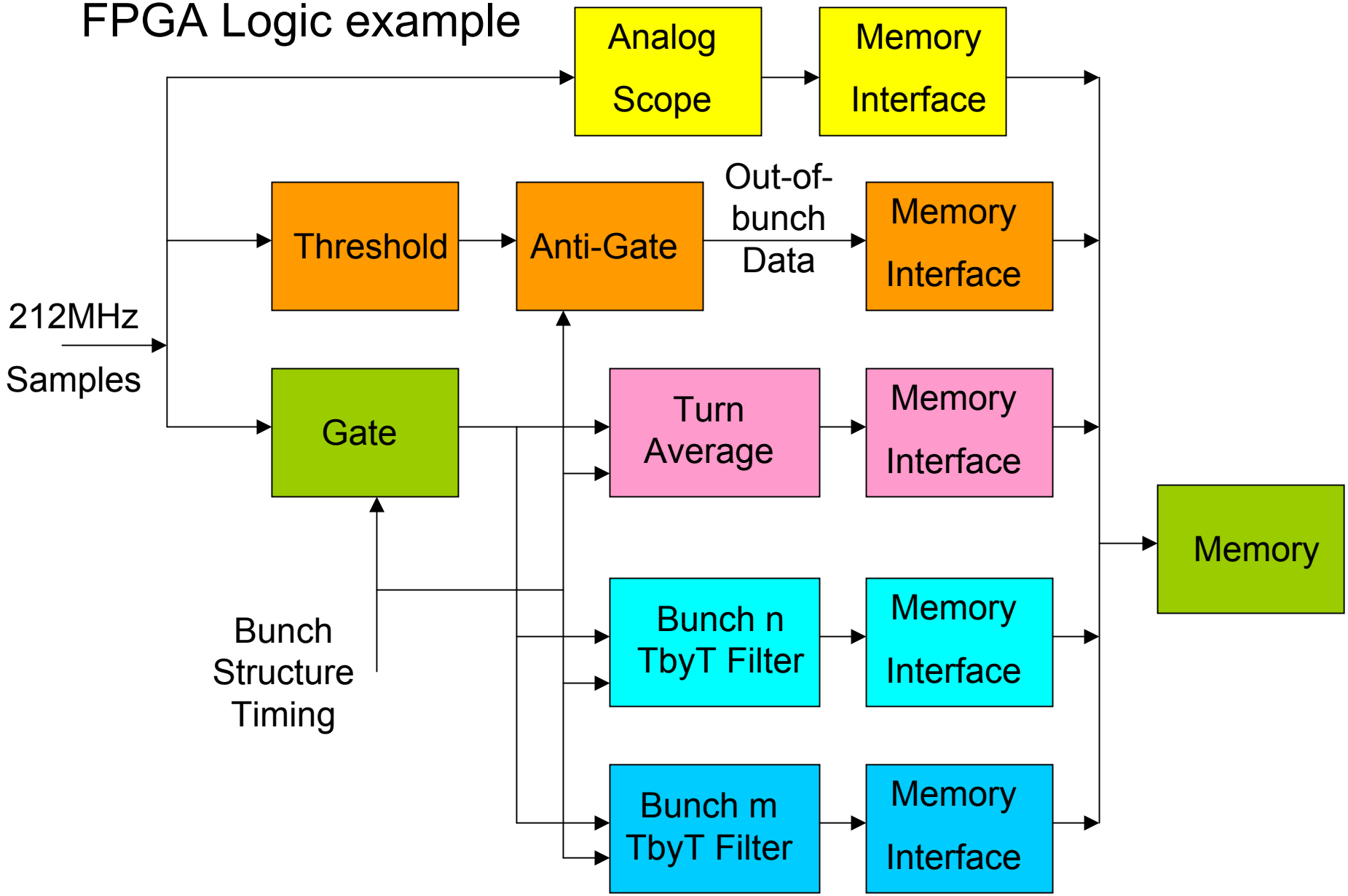

BPM
Pick-ups
Sample
Timing
Clocks and Timing
ACNET
BLM
FADC – 4 Chan/2 BPM
UCD
VME CPU + EDB PMC
V
M
E


BPM
Pick-ups
FADC – 4 Chan/2 BPM
BLM
Timing and EDB/BLM
Clocks and Timing
ACNET
VME CPU
V
M
E

So What Do We Get?

- Minimum: A Sample every bucket, allowing filtering and averaging everything with everything. Multiple data streams.
- Synchronous sampling and phasing can be beam triggered.
- Sampling based on the beam structure, i.e the FPGA data rate is proportional to the beam structure.
- We can time-separate the proton signal from the antiProton signal.

FPGA Logic example



What is the bad news?

- It isn't a perfect fit to our problem but the core design is close enough that we should be able to use it.
- It isn't a production board just a good core design we can build upon.
- It is complete over-kill but it costs $400-$500 per channel today, quantity one.

What needs to be done?

- Determine the Analog Filter to use:
  - Nothing??
  - Low Pass Filter only?
  - Switchable Bandpass Filter to spread the pulse width on uncoalesed bunches?
- Determine functionality of current board and stuff another one for our testing.
- Soon, channel # decision. Then layout new board and simulation of VHDL logic.

Webber Questions

- are there parallel, simultaneous position processing issues in the new requirements that the FDB architecture can/cannot satisfy?
  - Nope
- what are the requirements for switching between modes in a short time?
  - Run several modes in parallel
- is the FDB pipeline/FIFO processing architecture limiting in any significant way relative to TeV requirements?
  - No FIFO, FPGA pipeline runs faster than data rate.
- are implied VME backplane data rates acceptable?
  - VME rates are ACNET request dependent. Boards can buffer data.
- what might be possibility of excessive loading on VME CPU?
  - Programmer dependent.
- what are the triggering implications and requirements on external timing/triggering system?
  - Noticeable, timing must sync to accelerator clock.