TevBPM Upgrade Hardware Meeting, February 6, 2004

Mark Bowden made a presentation of possible options for VME card design and organization. The overheads are located on the Beams document database as Beams-doc-1006.

There was a discussion about the advantages of having a Tevatron Beam Synch clock event that for injection. This makes the sampling of the first turn of beam deterministic around the ring for all injections, and it eliminates the necessity of hunting through the memory buffer for the first turn.

Under the current specifications, we could not find a reason that the Recycler timing module couldn't work in the Tevatron. However, the Recycler timing module firmware has little headroom for upgrades. Since the fanout module requires a redesign anyway, it would require little effort to include an upgraded FPGA on this module with VME communication capability. The FPGA fanout module could be programmed to act as a pass through for signals from a Recycler timing module until the new firmware can be designed and debugged. This eliminates fanout module firmware development from the critical path of testing and commissioning a full system.

There was also discussion about the diagnostics signals (referred to as calibration in the talk). The plan is to generate the signal with the FPGA and a DAC and have a series of relays to send signal down on one cable and monitor the signal on the rest of the cables.

There was a consensus that design of the fanout board with the FPGA upgrade should continue.

We discussed the options for generating the sampling clock for the EchoTek modules. The recycler uses a PMC phase locked loop card that is rather expensive ($2200 ea.). This module has capabilities that are not necessary for the Tevatron system. It is capable of remote control of the digitizer frequency, but we will not want to change the digitizer frequency in the Tevatron. We decided to look into options that will be less expensive and may be included on the fanout board.

There are some questions that need to be answered before we have a final design:

Do we need to measure the diagnostic reference signal with some channel directly without going through the tunnel hardware and cables?

Do we need to have direct, external access to raw signals from BPM for diagnostics purposes?

How many Recycler style trigger cards should we construct to insure commissioning is not stalled by firmware development?

Jim Steimel