

From stephen@fnal.gov Wed Feb 18 10:58:04 2004
Date: Thu, 12 Feb 2004 07:25:01 -0600
From: Stephen Pordes <stephen@fnal.gov>
To: baumbaugh@fnal.gov, bhanna@fnal.gov, hendricks@fnal.gov, molson@fnal.gov,
steimel@fnal.gov, demaat <demaat@fnal.gov>, Bill_Haynes <haynes@fnal.gov>,
nickerbocker@fnal.gov
Cc: Jonathan Lewis <jdl@fnal.gov>, Paul Czarapata <pcceed@fnal.gov>,
Mike_Syphers <syphers@fnal.gov>, yarema <yarema@fnal.gov>
Subject: blm meeting issue summary..

BLM proposal presentation 02/10/04

present: Hanna, Steimel, Votava, Haynes, Hendricks, Demaat, Pordes, Baumbaugh,
Knickerbocker, Olson

Al presented his picture of the requirements and architecture of a system that can be tested in july. His transparencies are in the BLM topic in Instrumentation (Doc 992-v2): discussion is based on these.

General issues to be addressed are:

are there features that are not needed;
are there features that are missing;
are there architecture decisions that need to be changed;

Key aspects:

DIGITIZING AND ABORTS

Digitize at some rate - up to 1 MHz - with 14 bit ADC -> all quantities are then constructed from digitized data:

4 types of constructs for aborts:

single sample threshold, 2 running sum thresholds with different lengths, 1 time over threshold.

Multiplicity thresholds for each type of abort.

Individual channel masking for each type of abort.

Abort type available to concentrator.

MECHANICALS

Similar size crate as present.

Daughter cards carry two channels each.

Design will avoid requirements for massive uncabling to replace a card.

HV will be as present.

CONTROL AND COMMUNICATION

Assume ACNET interface initially at least by BPM controller.

Communication initially via External Device Bus to be able to interface with current system (hardware and software).

Same set of data buffers as present plus deep turn-by-turn buffers.

PC104 buss, EZ80 CPU

Ethernet spigot for future.

Issues re DIGITIZING AND ABORTS

Do we need 4 abort types? Do we need 64 states?

Can the concentrator use the abort types? Should it be able to?

Issues re CONTROL AND COMMUNICATION

BPM controller to be ACNET interface

is ethernet appropriate?
(suggested that bill haynes and al agree on a high speed data link
hosted by the BPM controller)
how much memory needs to be reserved on the BPM controller?
will look to see if Power PC available on PC104
assembly language or C?

Issues re MECHANICAL
request for power switch at front
request for voltage test points
request for led indicators
insistence on robustness

Stephen