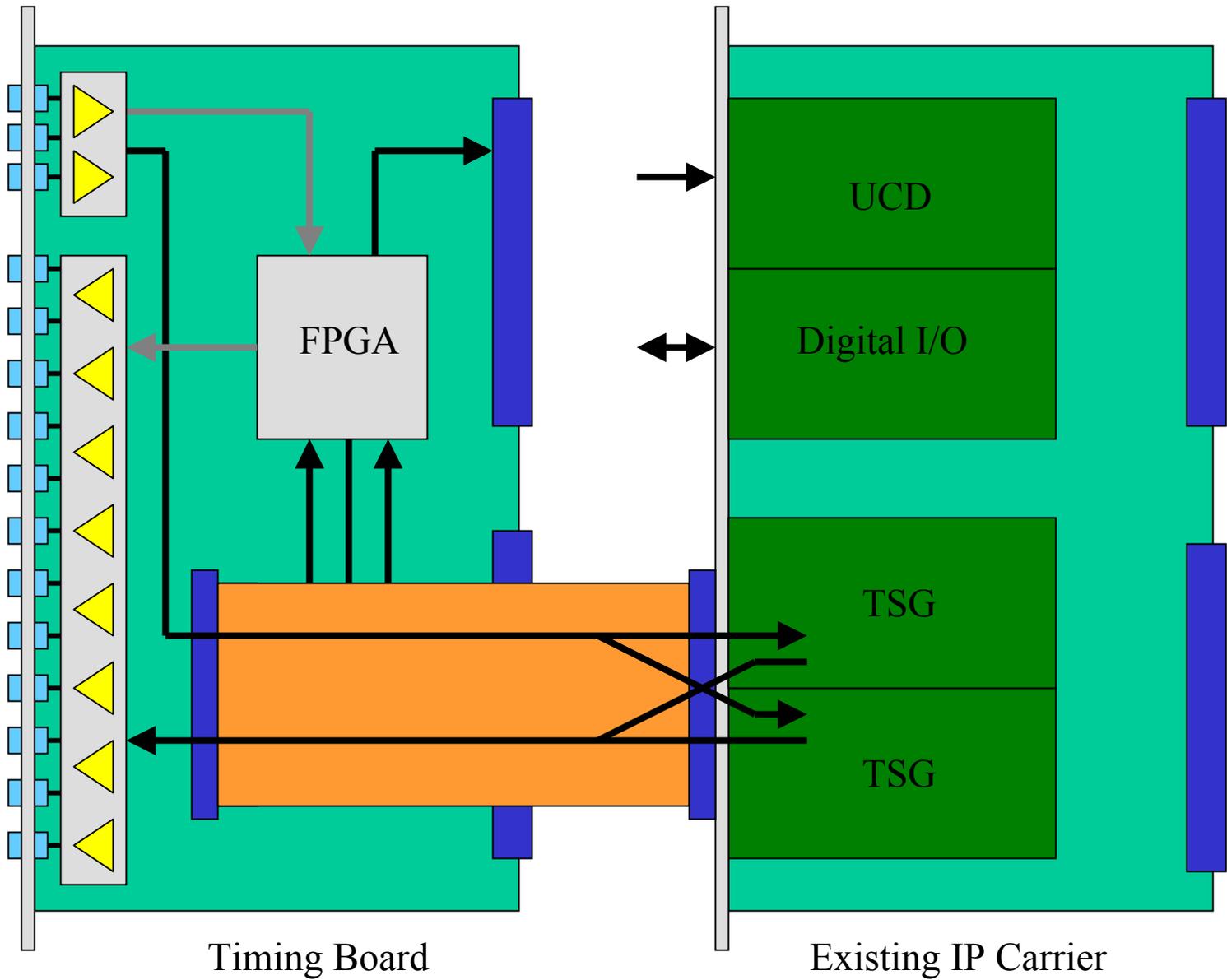
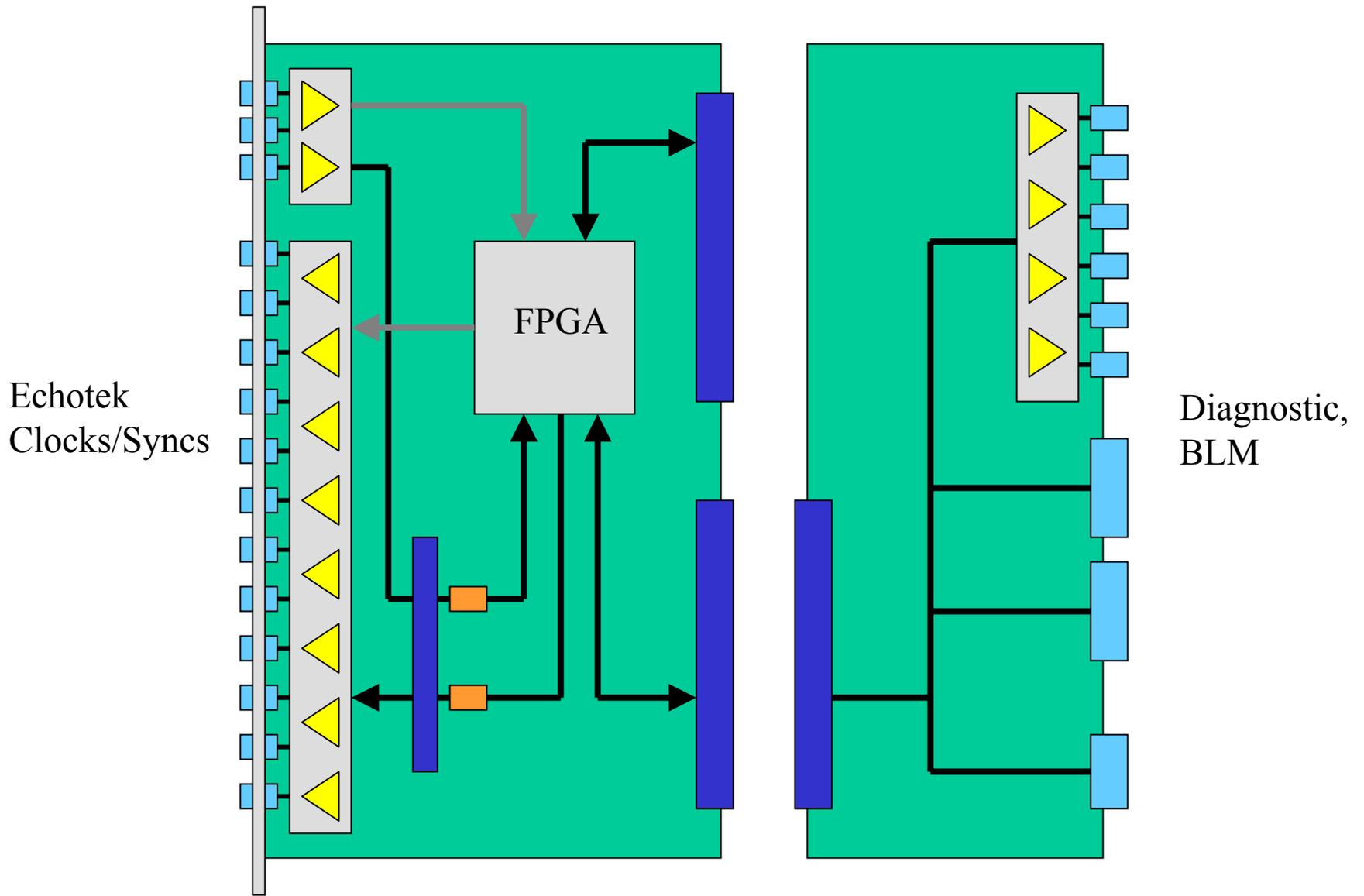


Timing Board



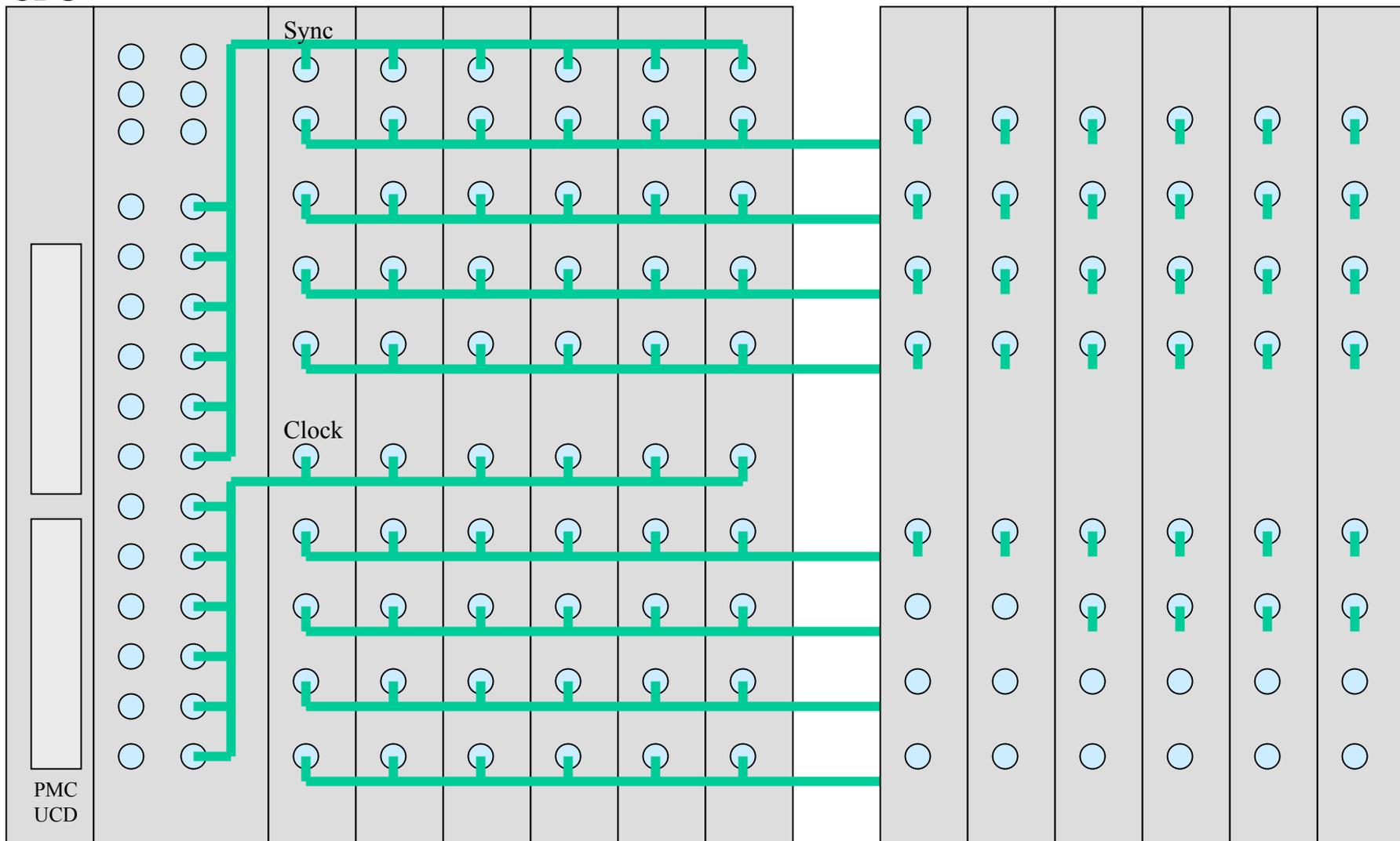
Use existing IP version until firmware is ported to new FPGA



Back to 2 boards (reduce front panel crowding)

# Digital Receivers

CPU

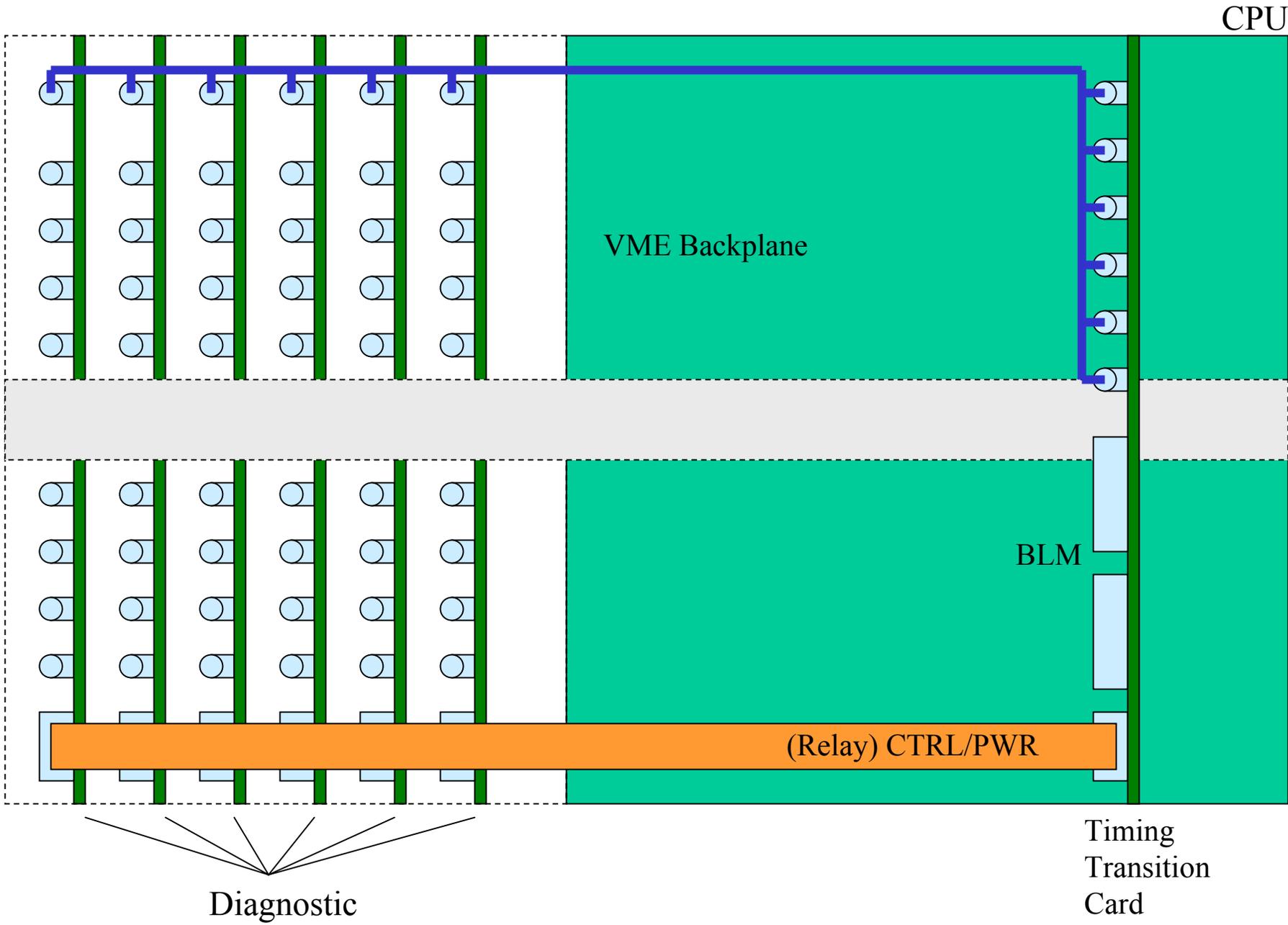


PMC  
UCD

Timing

(Clock generator incorporated in Timing board)

Diagnostic

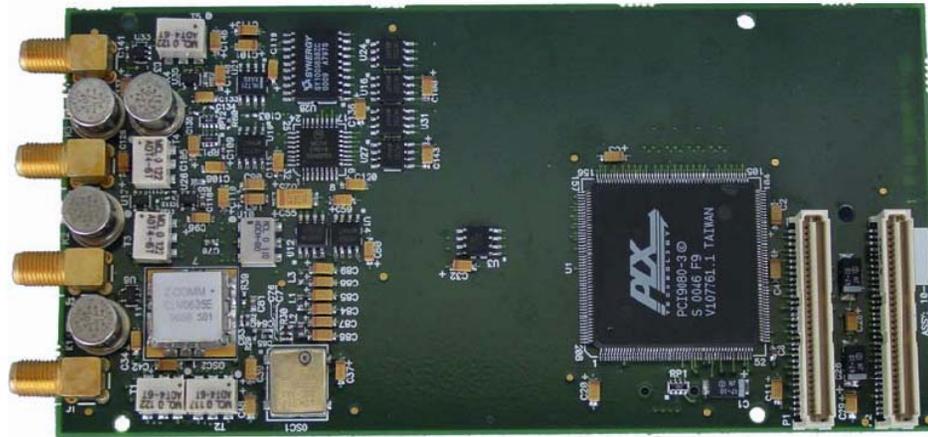


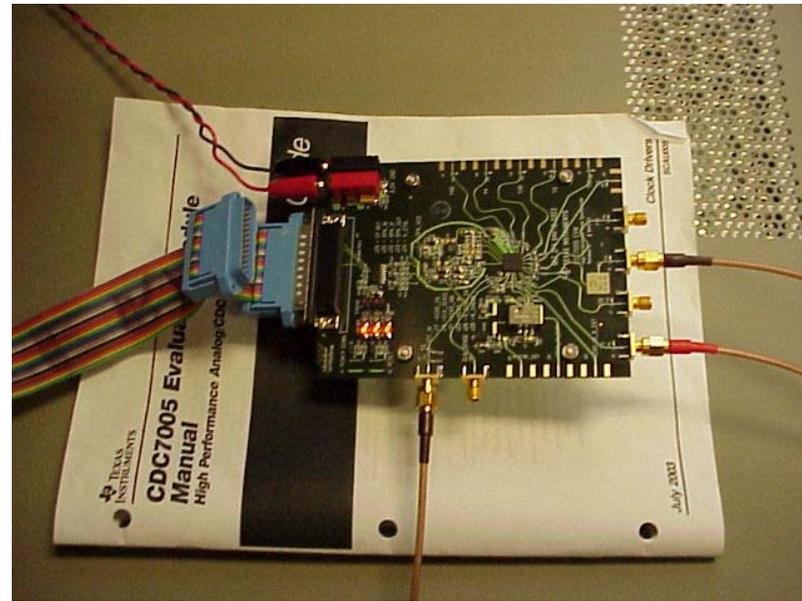
## Clock Requirements?

- sync to Tev RF
- tradeoff between jitter and tracking range  
(VCXO vs. VCO)
- 14 bit ADC, 53 MHz signal  
1 LSB =  $< 0.5$  psec
- we would like to measure Echotek and  
Tev RF jitter (250 psec?)

# Echotek Clock Generator

- VCO
- tracking range 47.9 - 56.3 MHz





CDC7005 SPI

File Operate Help

Reference Divider M: 3

Reference Delay M: 0ps

PFD Pulse Width Delay: 0ps

Charge Pump Current: 2.0mA

CP Enable:

CP direction:

OPA Enable:

VCXO Divider N: 1

VCXO Delay N: 0ps

Lock detect window: ±1.2ns

MUXSEL: Y0

MUX0 Div by 1:  Y0 Enable

MUX1 Div by 8:  Y1 Enable

MUX2 Div by 4:  Y2 Enable

MUX3 Div by 8:  Y3 Enable

MUX4 Div by 8:  Y4 Enable

Port address: 378

Send

Reset all Dividers

PD current Sources

Enable External Reference Resistor

Enable Bandgap

Enable Hold Functionality

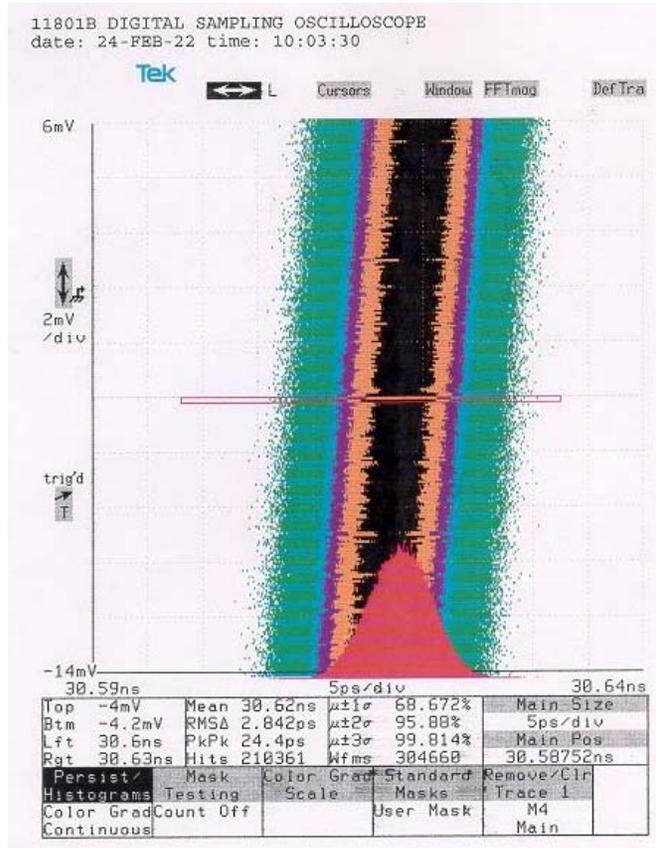
**CDC7005**  
Serial Peripheral Interface  
Version 2.1

TEXAS INSTRUMENTS  
High Performance Analog / CDC  
© by Josef Marsmann

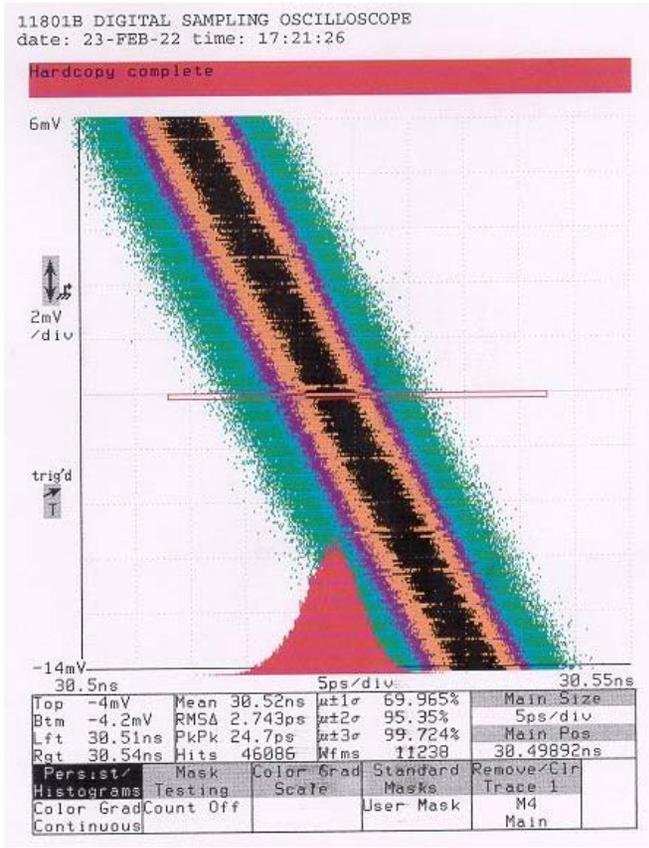
## Test with TI CDC7005

- similar to Echotek Clock Generator (\$99 evaluation module, not PMC)

- used VCXO (better frequency stability, but narrow tracking range)



input



output

# SCG102A Synchronous Clock Generators

PLL



## Applications

- SONET / SDH / ATM
- DWDM / FDM
- DSL-PON Interconnects
- FEC (Forward Error Correction)

## Features

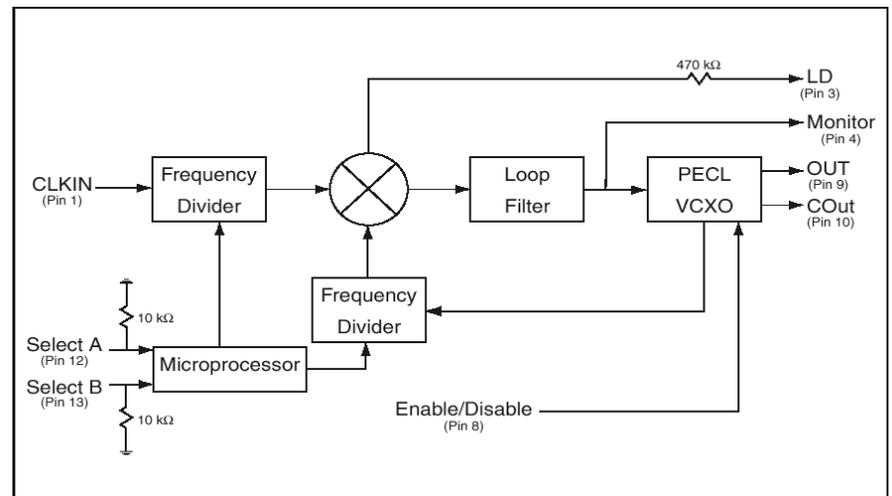
- 3.3V High Precision PLL
- Accepts 1 of 4 Selectable, Pre-determined Input Frequencies
- 77.76 MHz to 170 MHz Output Frequencies Available.
- Jitter Generation OC-192 Compliant
- 1.0" x 0.80" x 0.285", Surface Mount

Input

53.104 MHz (+/- 2.5 KHz)

Output (3/2)

79.656 MHz (0.5 psec)



# Timing Board

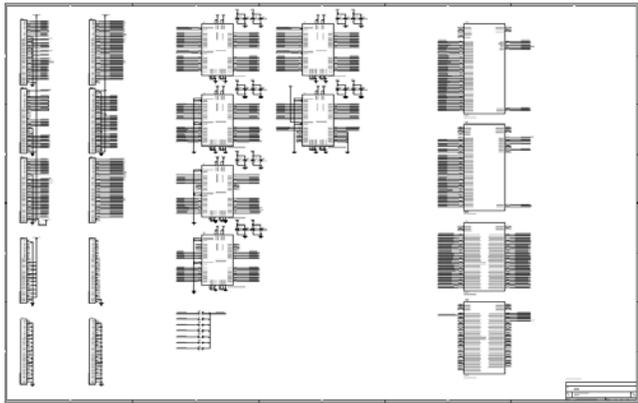
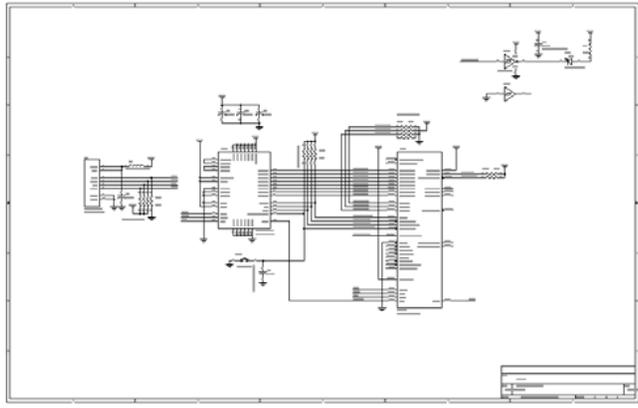
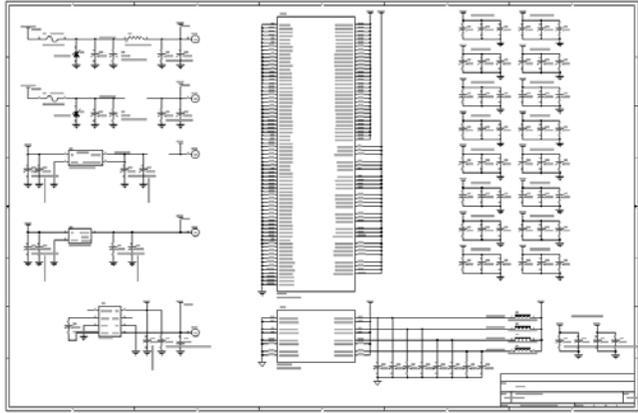
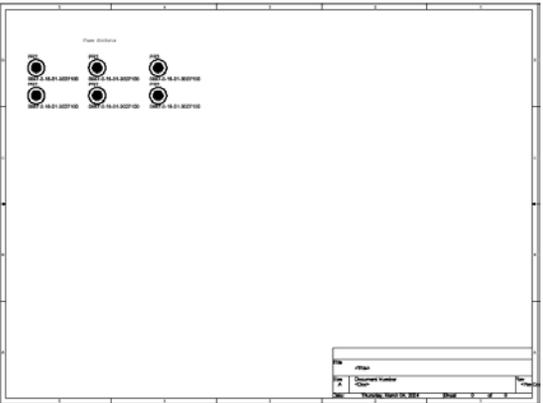
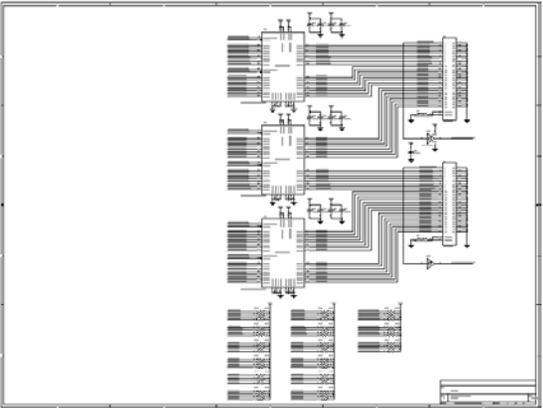
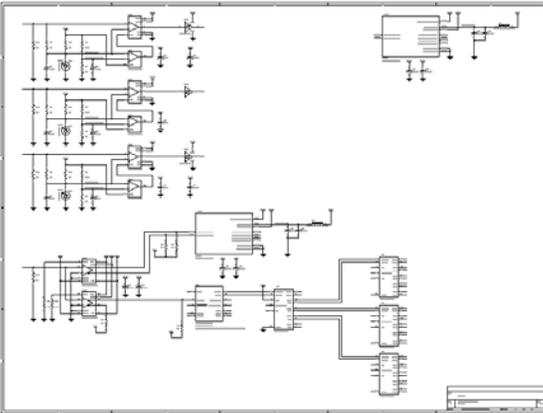
- FPGA comparison

**Table 1-1. Stratix Device Features — EP1S10, EP1S20, EP1S25, EP1S30**

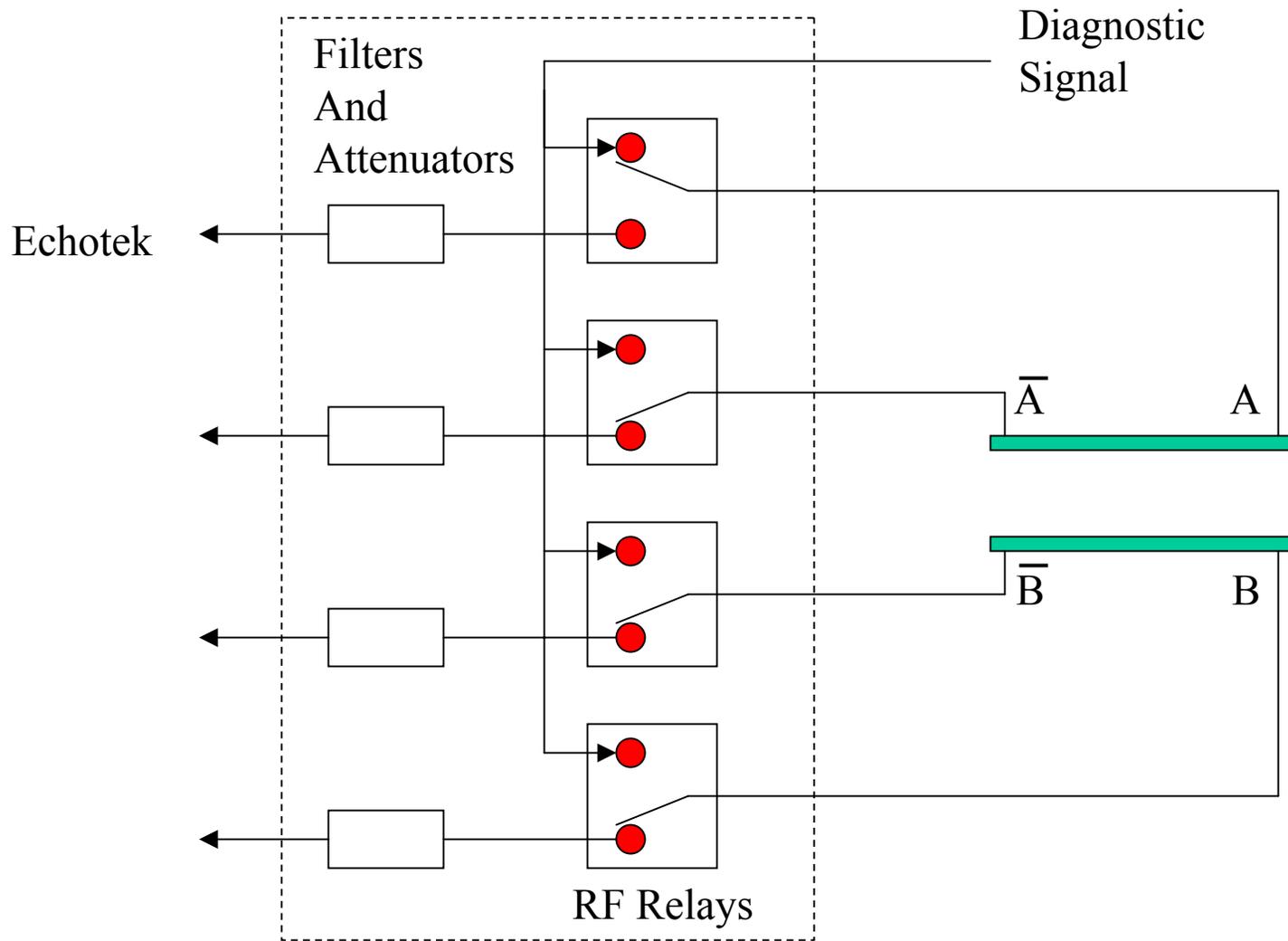
| Feature                           | EP1S10  | EP1S20    | EP1S25    | EP1S30    |
|-----------------------------------|---------|-----------|-----------|-----------|
| LEs                               | 10,570  | 18,460    | 25,660    | 32,470    |
| M512 RAM blocks<br>(32 × 18 bits) | 94      | 194       | 224       | 295       |
| M4K RAM blocks<br>(128 × 36 bits) | 60      | 82        | 138       | 171       |
| M-RAM blocks<br>(4K × 144 bits)   | 1       | 2         | 2         | 4         |
| Total RAM bits                    | 920,448 | 1,669,248 | 1,944,576 | 3,317,184 |
| DSP blocks                        | 6       | 10        | 10        | 12        |
| Embedded multipliers (1)          | 48      | 80        | 80        | 96        |
| PLLs                              | 6       | 6         | 6         | 10        |
| Maximum user I/O pins             | 426     | 586       | 706       | 726       |

TSG 10K40  
2300 LEs

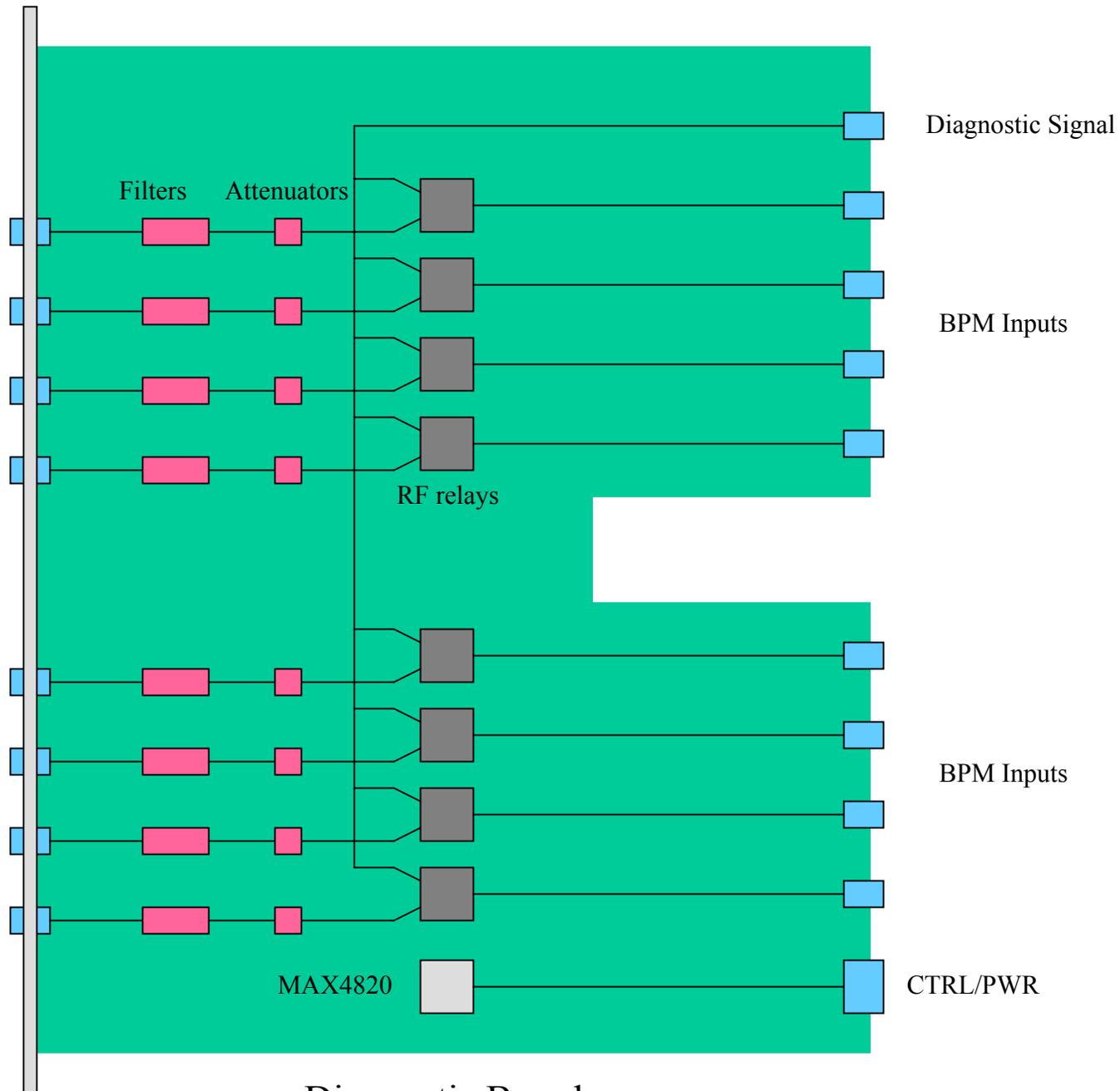
- existing VME interface and TSG code ported, not compiled
- partial schematics



Timing Board



Diagnostic signal applied to any one of four BPM ports can be monitored on other three ports.



Diagnostic Board