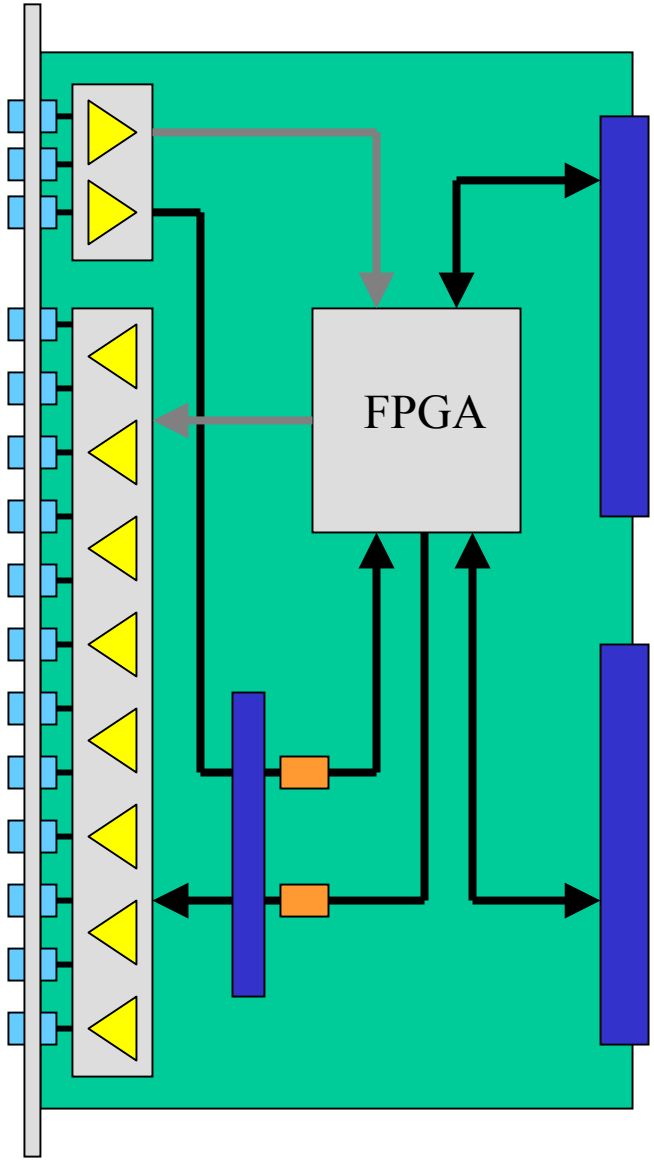
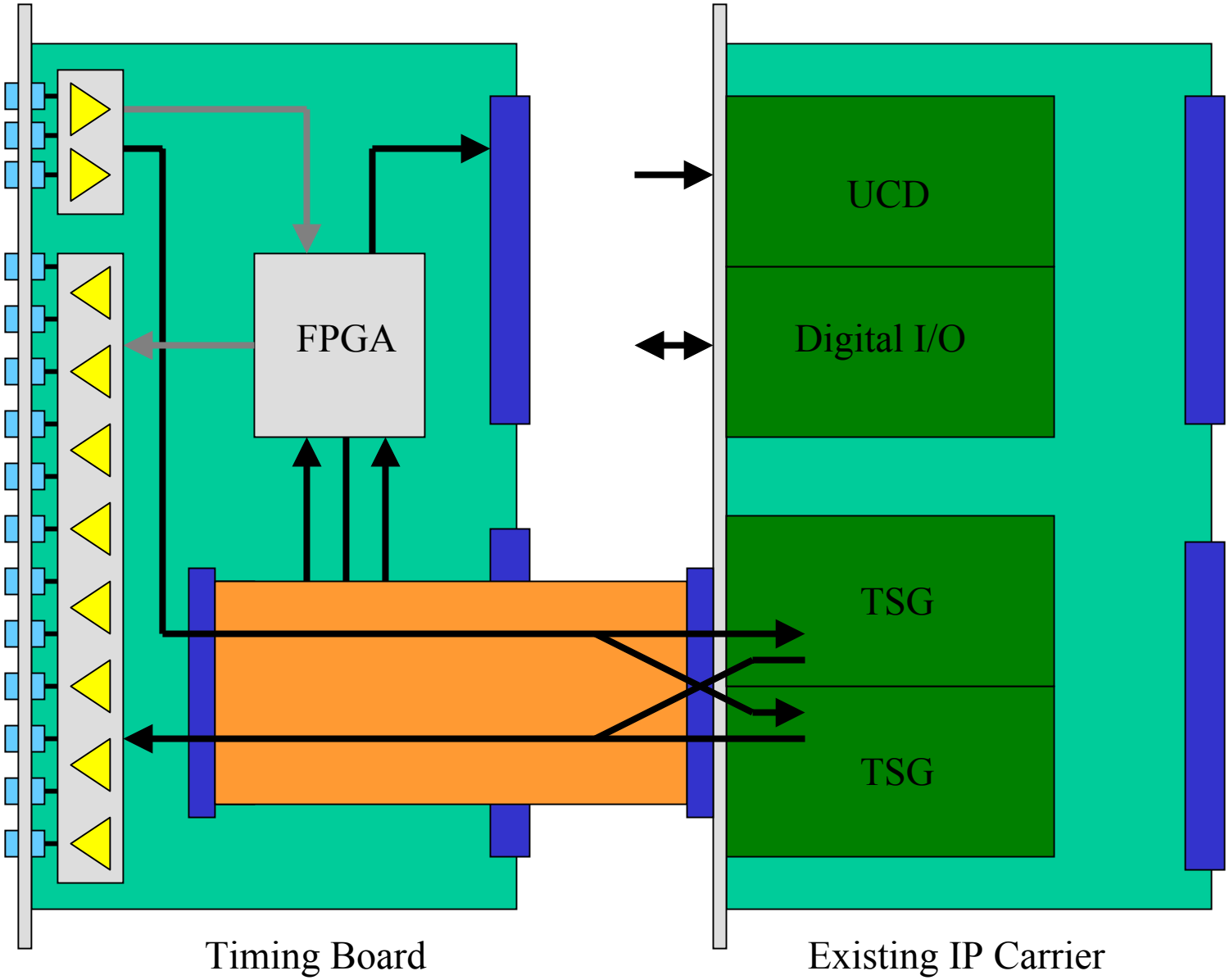
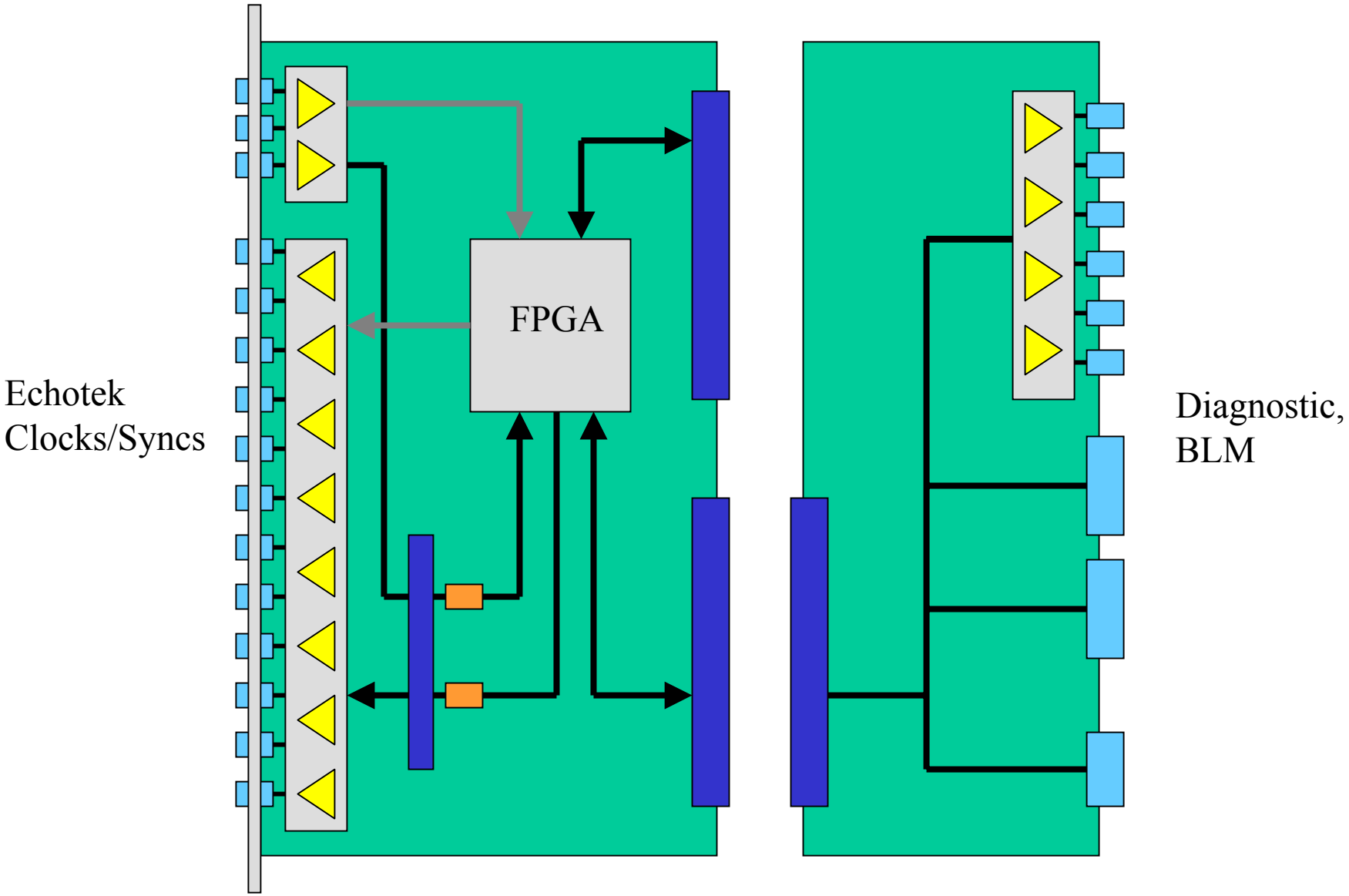


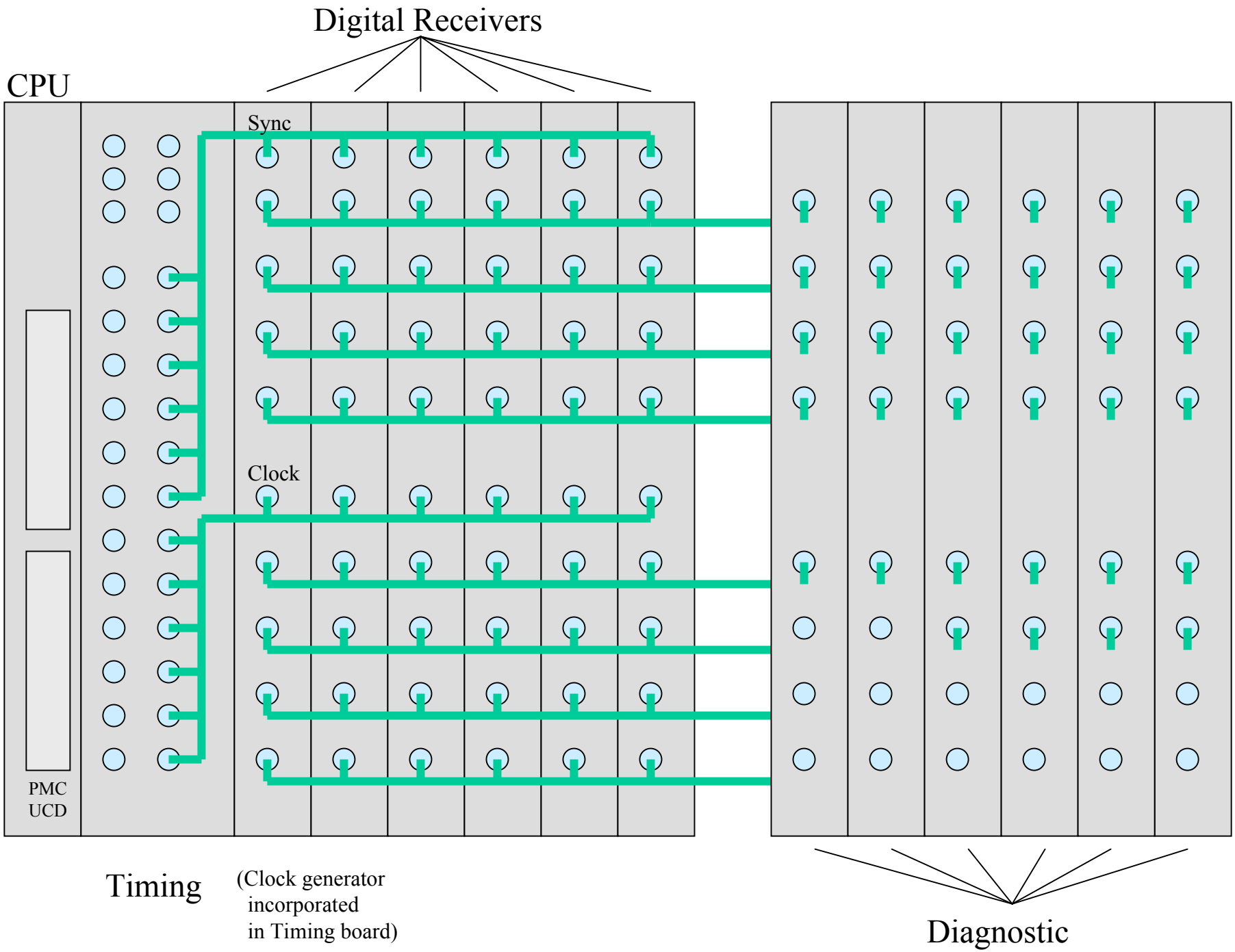
Timing Board

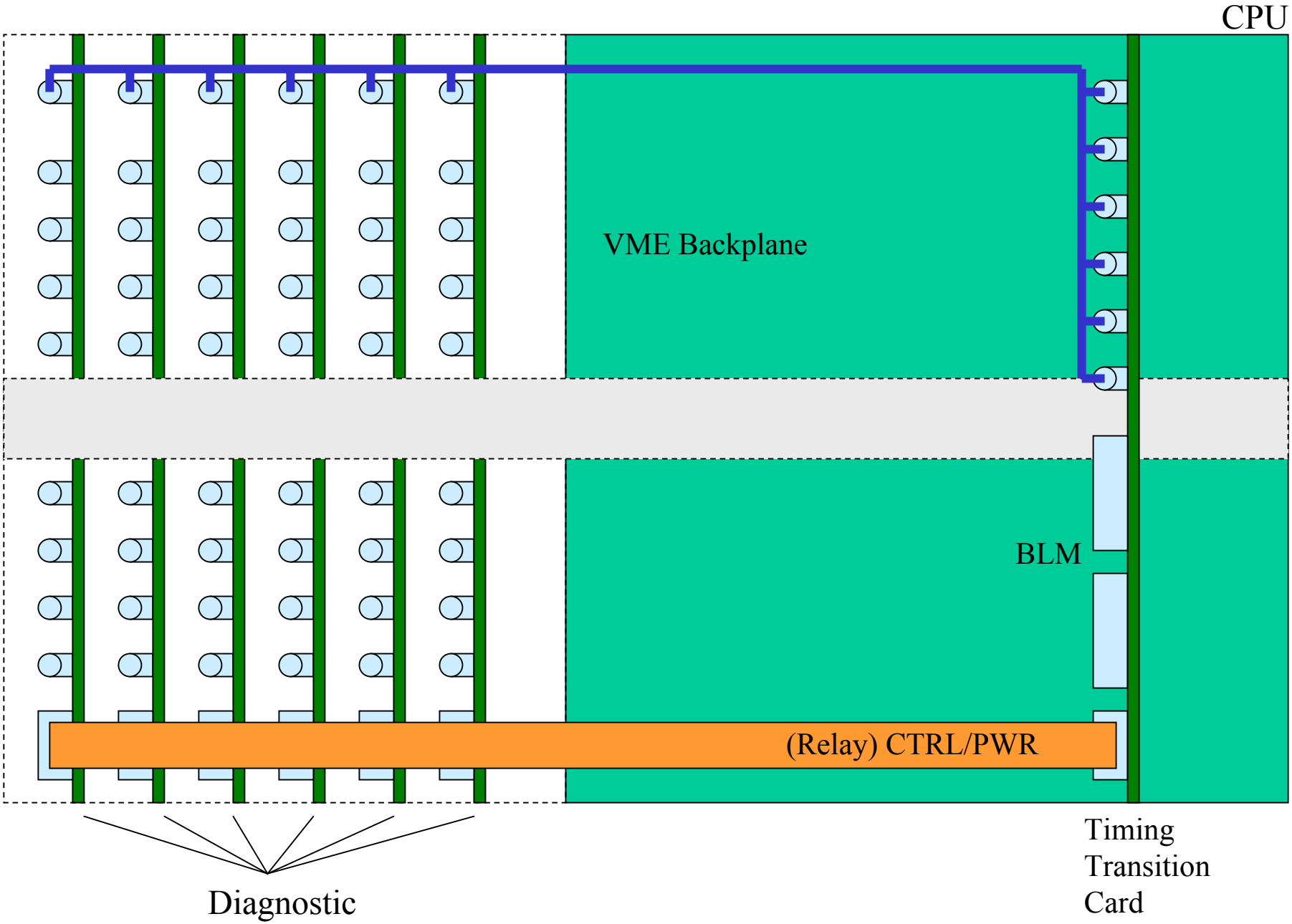


Use existing IP version until firmware is ported to new FPGA



Back to 2 boards (reduce front panel crowding)


Digital Receivers
CPU
Sync
Clock
PMC
UCD
Timing
(Clock generator
incorporated
in Timing board)
Diagnostic


CPU
VME Backplane
BLM
(Relay) CTRL/PWR
Timing
Transition
Card
Diagnostic

Clock Requirements?

- sync to Tev RF

- tradeoff between jitter and tracking range
  (VCXO vs. VCO)

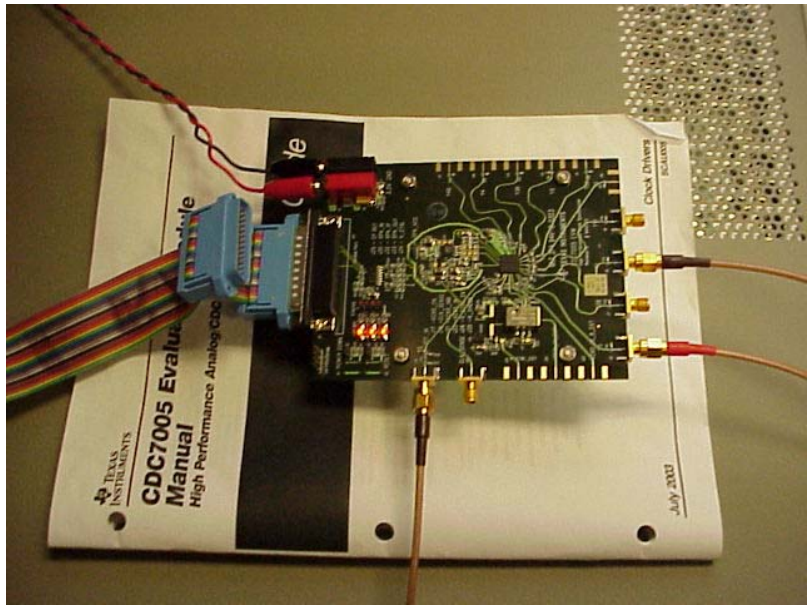
- 14 bit ADC, 53 MHz signal
  1 LSB = < 0.5 psec

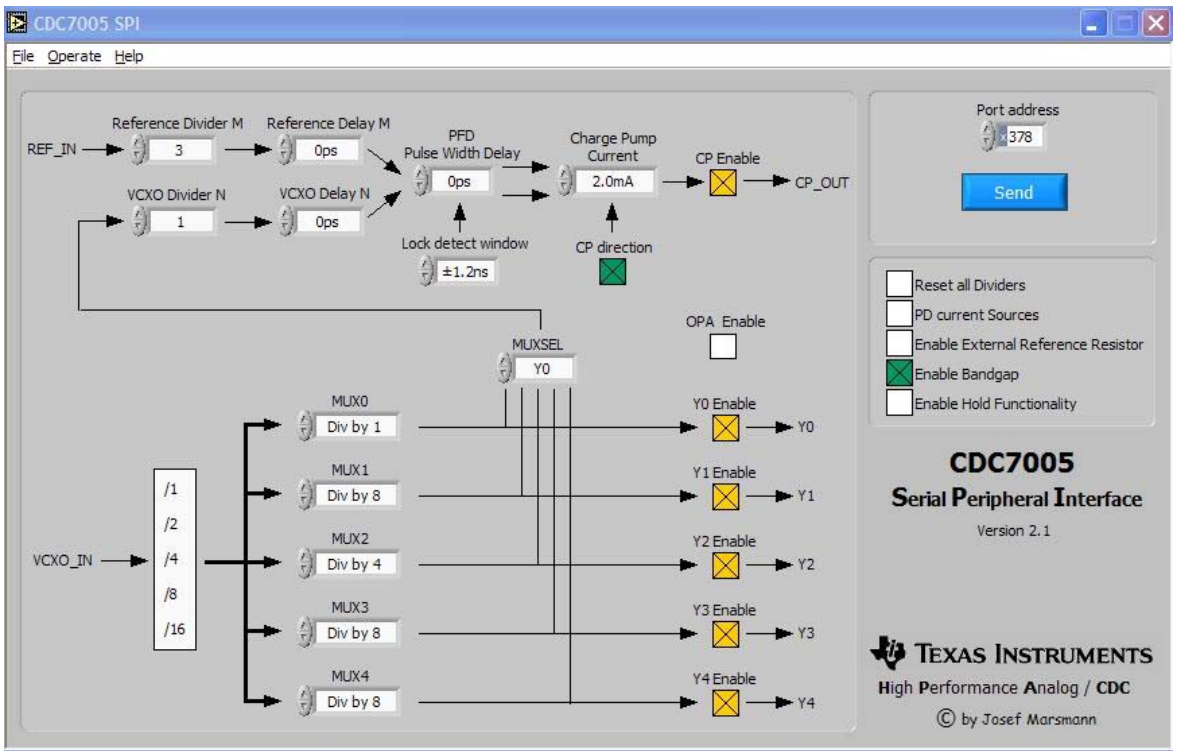
- we would like to measure Echotek and Tev RF jitter (250 psec?)

Echotek Clock Generator

- VCO

- tracking range 47.9 - 56.3 MHz

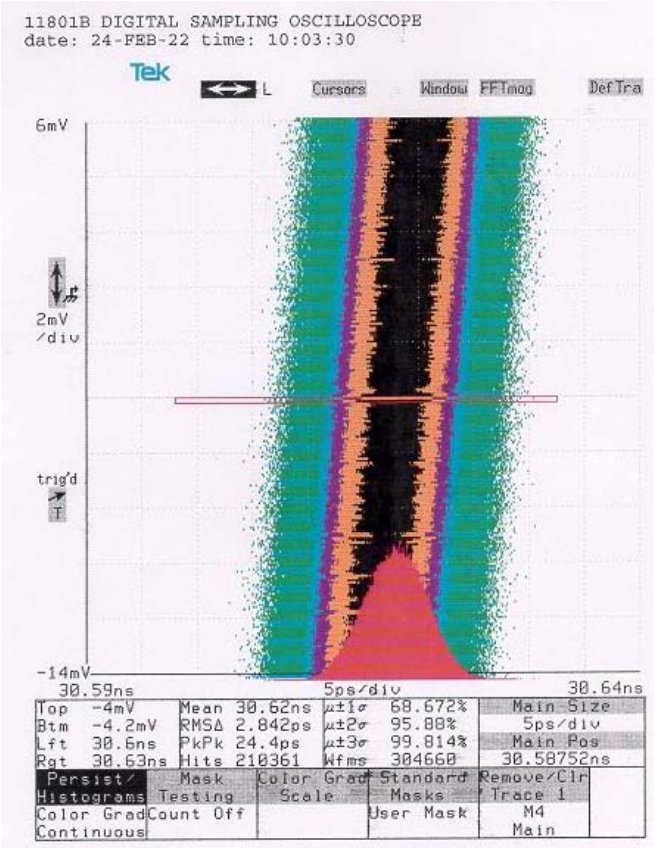




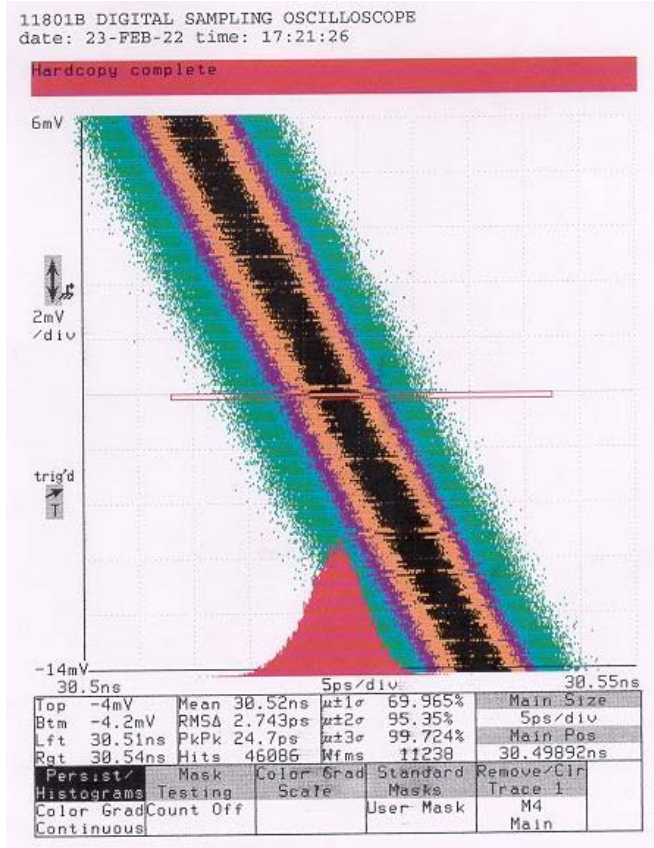
Test with TI CDC7005

- similar to Echotek Clock Generator ($99 evaluation module, not PMC)

- used VCXO (better frequency stability, but narrow tracking range)



input



output

SCG102A Synchronous Clock Generators

PLL

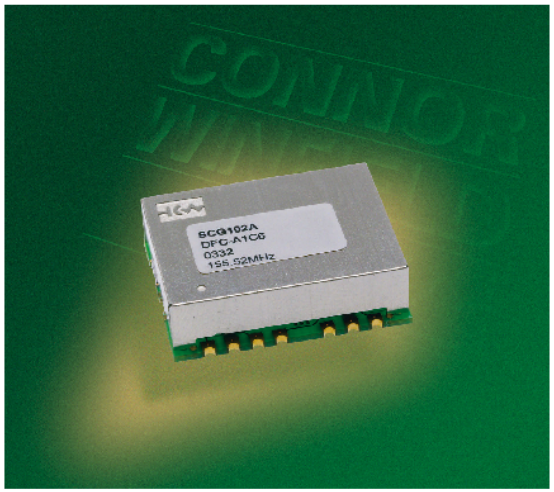
CONNOR WINFIELD

Input

53.104 MHz (+/- 2.5 KHz)

Output (3/2)

79.656 MHz (0.5 psec)

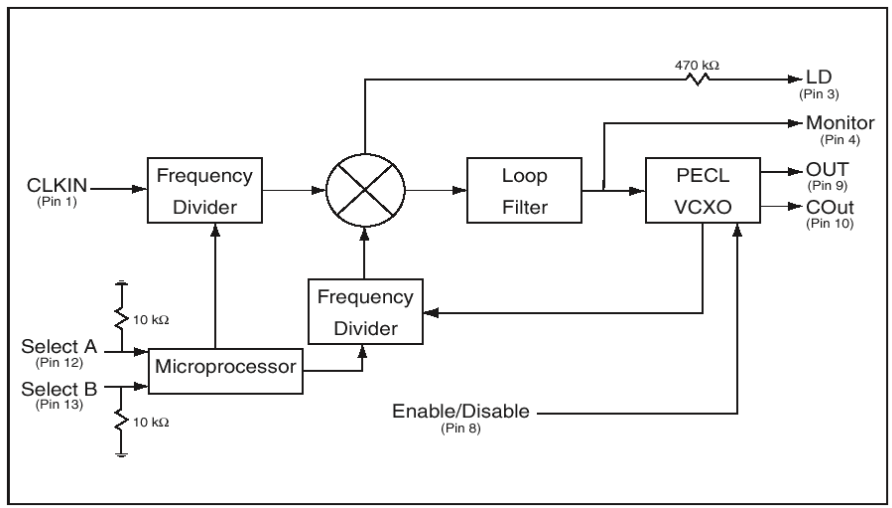


Applications

- SONET / SDH / ATM
- DWDM / FDM
- DSL-PON Interconnects
- FEC (Forward Error Correction)

Features

- 3.3V High Precision PLL
- Accepts 1 of 4 Selectable, Pre-determined Input Frequencies
- 77.76 MHz to 170 MHz Output Frequencies Available.
- Jitter Generation OC-192 Compliant
- 1.0" x 0.80" x 0.285", Surface Mount



Timing Board

- FPGA comparison

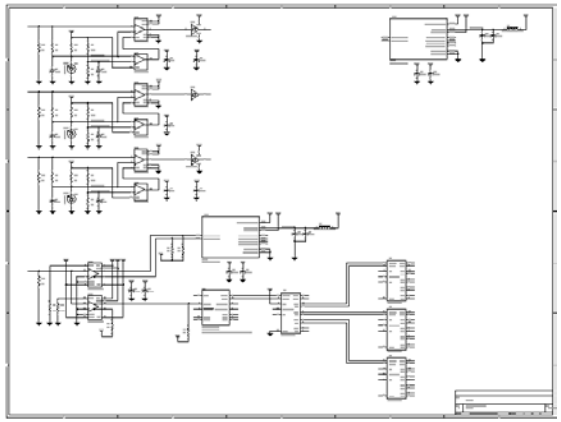
Table 1–1. Stratix Device Features — EP1S10, EP1S20, EP1S25, EP1S30

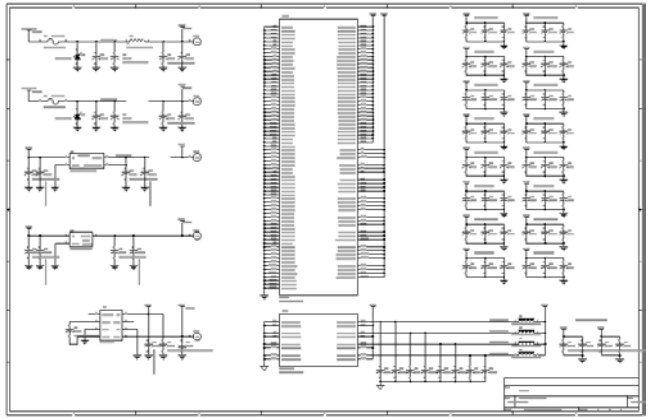
Feature	EP1S10	EP1S20	EP1S25	EP1S30
LEs	10,570	18,460	25,660	32,470
M512 RAM blocks (32 × 18 bits)	94	194	224	295
M4K RAM blocks (128 × 36 bits)	60	82	138	171
M-RAM blocks (4K × 144 bits)	1	2	2	4
Total RAM bits	920,448	1,669,248	1,944,576	3,317,184
DSP blocks	6	10	10	12
Embedded multipliers *(1)*	48	80	80	96
PLLs	6	6	6	10
Maximum user I/O pins	426	586	706	726

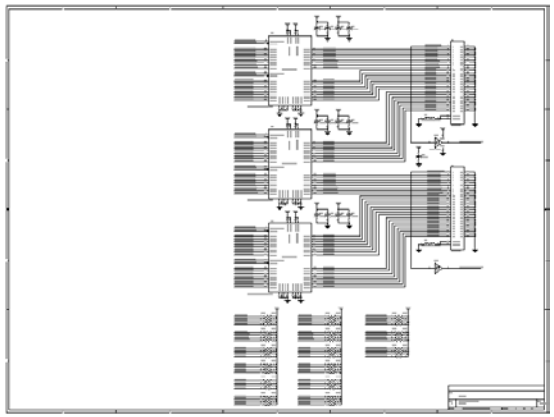
TSG 10K40
2300 LEs

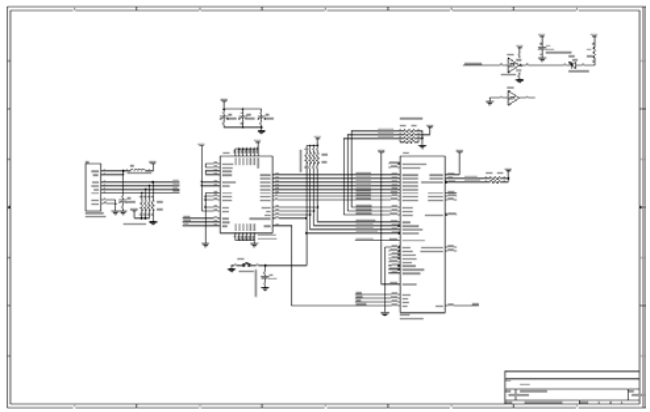
- existing VME interface and TSG code ported, not compiled

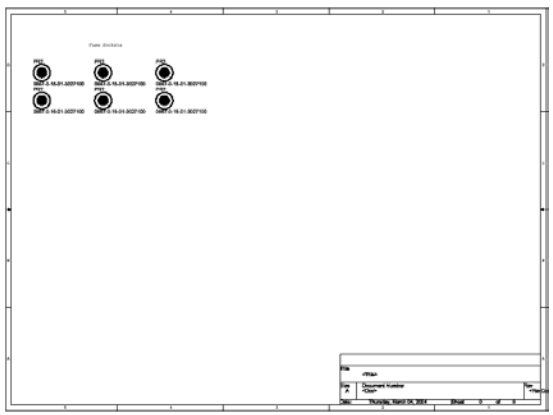
- partial schematics

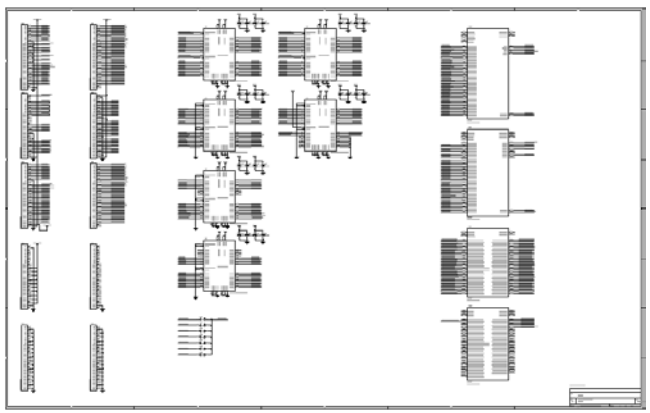




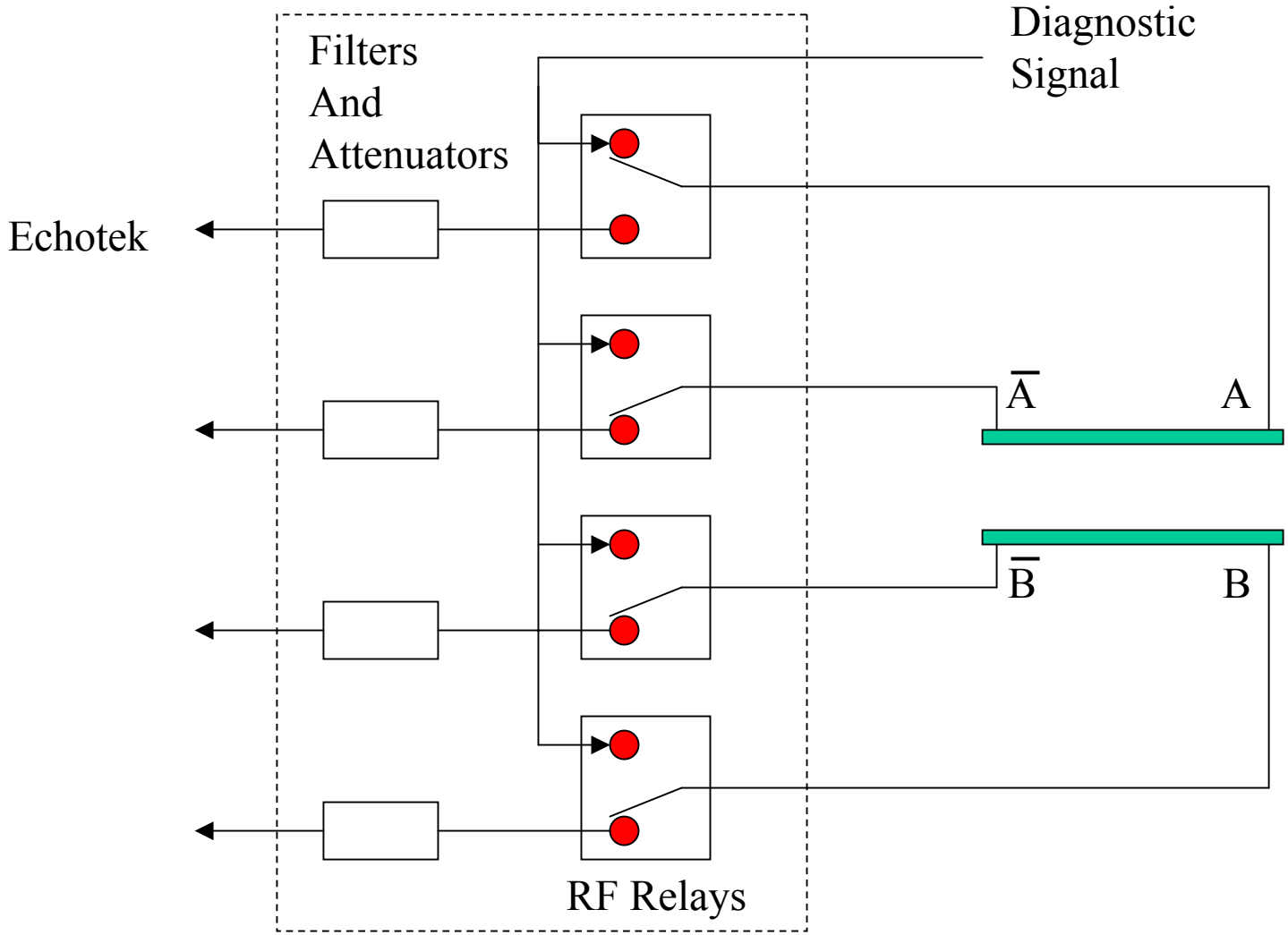




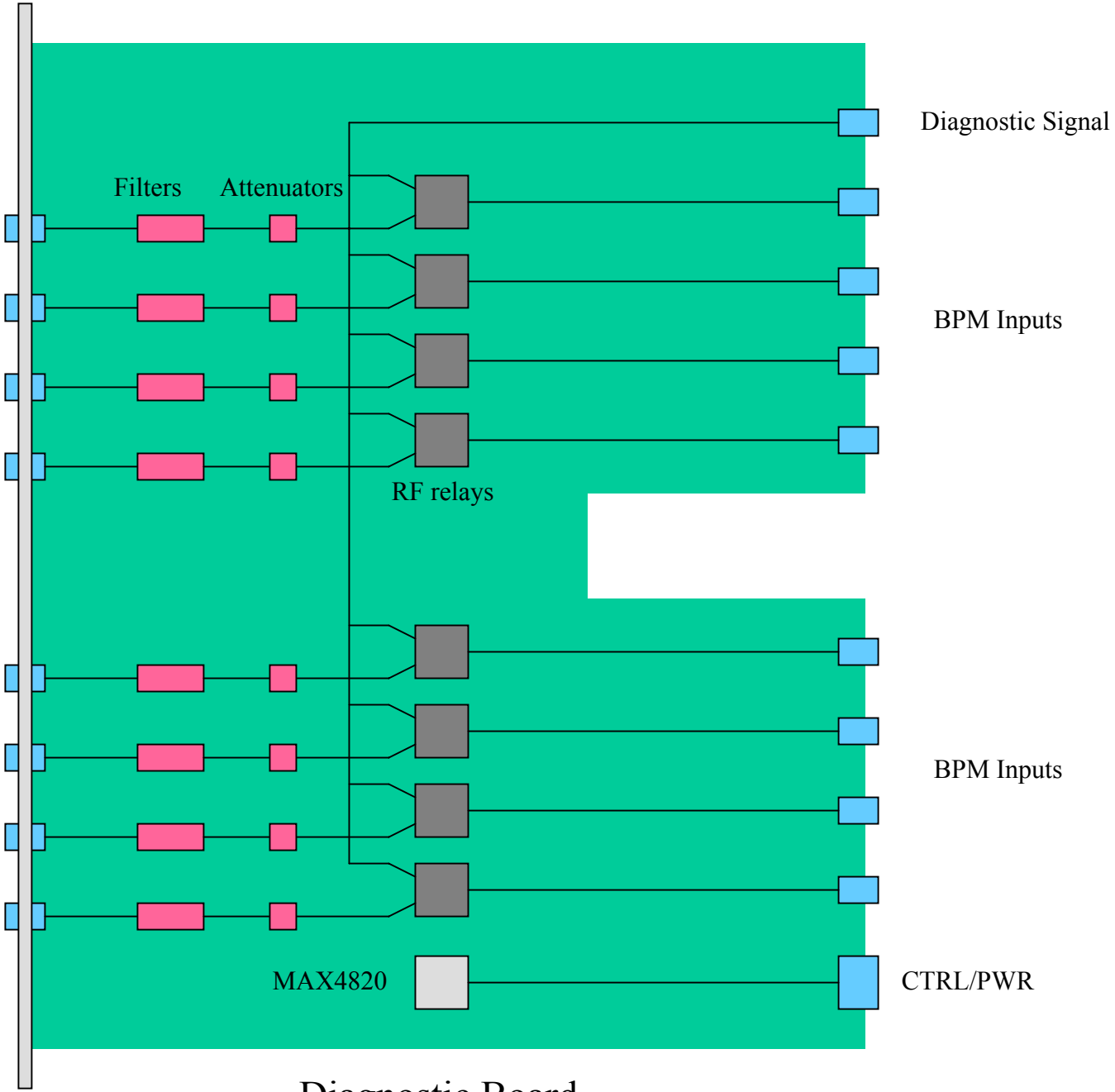




Timing Board



Diagnostic signal applied to any one of four BPM ports can be monitored on other three ports.



Diagnostic Board