



Tevatron Beam Position Monitor (BPM) Upgrade Hardware Specifications for Data Acquisition

DRAFT

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Abstract

This document contains the specification for the Beam Position Monitor/Beam Loss Monitor (BPM/BLM) upgrade data acquisition hardware. Expected operating modes and interactions with the BPM/BLM software are described. Analog signal processing, timing system and diagnostic circuits are specified in this document. Calibration and diagnostics procedures are described.

While this document is in draft form, Vince Pavlicek will be the editor. If you have suggestions or changes, use a copy of the document, turn on change tracking, and send the document to Vince@fnal.gov. He will integrate the changes into the database document. Thanks.

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Overview

This document describes the hardware needed for the data acquisition component of the Tevatron Beam Position Monitor (BPM) upgrade project. The data acquisition (DA) hardware will digitize the analog position signal from the BPM sensors, digitally filter the signals and make them available to a VME front-end computer. The DA will also provide the interface to the Beam Loss Monitor (BLM) circuitry through the External Device Bus (EDB) to replace the functionality of the existing system. Figure 1 shows the functional block diagram and the different elements involved with the BPM upgrade project.

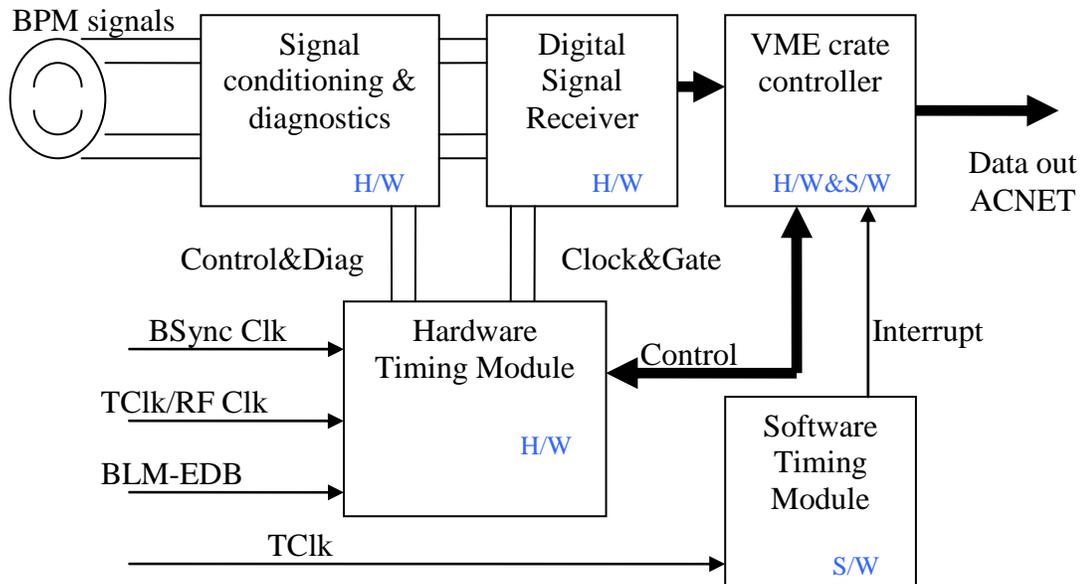


Figure 1 BPM Front End Functional Block Diagram

The hardware functions described in Figure 1 are implemented in four modules that match the hardware blocks above. The signal conditioning and diagnostics are implemented on the Filter/Diagnostic module being designed at FNAL. The Digital Signal Receiver (DSR) is a Commercial-Off-The-Shelf (COTS) module from Echotek Corporation, the ECDR-GC814/8-FV2. The timing functions are implemented on the VME Timing Fanout module designed at FNAL. The VME sub rack controller is a COTS Single Board Computer from Motorola Corporation, the MVME2400

Beam Position System

Sensor

The Tevatron BPM sensors¹ and² are two opposing curved stripline plates approximately 18 cm long along the beam and oriented to partially surround the beam. Each plate subtends approximately 110 degrees of the full circle around the beam. The circular aperture of the pair (the diameter of the opening) is 6.6 cm. There are connections at both ends of each plate, one connection emphasizing the proton direction of flight and the other the anti-proton direction. The signal taps are at the ends of the individual plates. The convention for the naming of the four signals from a specific BPM sensor are a letter designator for each of the two plates, the A plate, and the B plate, and whether it is the proton end or the anti-proton end. Each of the four BPM signals is treated identically in this Data Acquisition (DA) system except for a resistive attenuator which approximately matches the proton and anti-proton signal amplitude ranges into the Analog to Digital (A2D) converter input. The signal amplitudes are proportional to the number of particles passing through the sensor. In 2004 the amplitude of the proton signals at the proton outputs is approximately 5 times as large as the anti-proton signal at the anti-proton outputs. The 236 Tevatron sensors are on the end of quadrupole magnets in the beam tunnel and the BPM DA electronics modules are in service buildings around the ring. 200 to 300 meter long RG-8 cables bring the sensor signals to the DA system and the Filter/Diagnostic board.

BPM Data Acquisition System

The BPM signals pass through the Filter/Diagnostic board for amplitude conditioning and band pass filtering. The filter is centered at the 53.104 MHz accelerator RF frequency with a bandwidth of approximately 7 MHz. The filter specifications are in Appendix x. This module also has the capability to switch in a diagnostic signal and drive that signal out to the sensor or back toward the A2D module. By sequentially driving one output of a sensor and digitizing the other three sensor signals the general condition of that sensor and its associated cable plant can be determined. Short coaxial cables move the signals from the Filter/Diagnostic module outputs to the Analog to Digital converter board, an Echotek commercial digital signal receiver module. These signals are converted from analog to digital representation, passed to a Digital Down Converter (DDC) signal processing chip for base banding, filtering and then placed in memory that is accessible through the VME backplane bus. The data movement is controlled by firmware in a reprogrammable FPGA device. The VME sub rack controller is a Motorola MVME2400 type processor that controls the data acquisition process. The software that resides on the front-end microprocessors, also referred to as the Data Acquisition (DA) software, is described in Beams Document #860, Tevatron BPM Upgrade Software Specifications for Data Acquisition. The system timing is controlled by the VME BPM Timing Fanout module. The timing is based on three Tevatron timing signals. 1) the Main Ring RF Clock (RfClk) at 53.104 MHz, 2) Tevatron Beam Sync (TVBS), running at 7.5 MHz synchronous with the RfClk and containing some Tevatron commands and the encoded

¹ *The Tevatron Beam Position and Beam Loss Monitoring Systems (Beams-Doc-806)*

² *Fermilab Energy Doubler Beam Position Detector (Beams-DOC-809)*

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turn marker, BC0, and 3) Tevatron Clock (TClk) and Main Ring RF Clock (RFClk) running at 10 MHz and containing many Tevatron commands.

The sensor front-end electronics depicted in Figure 1 are contained within a VME sub rack holding a series of pairs of Filter/Diagnostic modules and BPM VME digitizing boards, the BPM Timing Fanout card, the sub rack controller and BLM interface hardware. **Error! Reference source not found.** illustrates the organization of the cards in the BPM VME sub rack. One sub rack can hold the necessary electronics needed for a service building (sometimes called a house). There are 30 service buildings or houses around the Tevatron ring, 27 of them contain BPM electronics and each BPM house has up to 6 BPM digitizing boards and up to 23 BLM digitizing boards in separate BLM analog crates. Table 1 is the current organization of BPM and BLM sensors relative to the service buildings.

Table 1

Service Building	BPMs	BPM Modules	BLMs
A0	4	2	12
A1	10	5	9
A2	9	5	9
A3	8	4	8
A4	9	5	8
B0	6	3	22
B1	10	5	9
B2	9	5	9
B3	8	4	8
B4	9	5	12
C1	10	5	12
C2	9	5	9
C3	8	4	8
C4	9	5	8
D0	6	3	23
D1	10	5	9
D2	9	5	9
D3	8	4	8
D4	9	5	8
E1	10	5	9
E2	9	5	9
E3	8	4	8
E4	11	6	11
F1	12	6	12
F2	9	5	9
F3	8	4	8
F4	9	5	8

The BPM digitizing modules are Echotek module ECDR-GC814/8-FV2, and each module digitizes signals from 8 channels. An individual BPM sensor generates information on 4 channels – the A and B plates for the proton end of the sensor and the A and B plates for the antiproton end. Therefore one Echotek module will be capable of accepting signals from two BPM sensors. The digitized output that results from each channel of the digitizing module may be either a calculated position or the digitized and filtered signal data. The details are in the Software Specifications document. If it is the digitized and filtered signal data, each channel is actually represented by two components: a real (Q) and imaginary (I) part.

The operation of the Echotek module is controlled by two inputs that are common for all eight channels. They are the CLK and SYNC signals. The digitizing clock paces the Echotek module and comes from the BPM Timing Fanout Module. A phase-lock-loop on the Timing module creates a clock output that has a fractional relationship to the Tevatron RF clock frequency. TeV RF is approximately 53.104 MHz. The Echotek clock is $7/5^{\text{th}}$ or approximately 74.346 MHz. This means that the 53.104 MHz signal is technically under-sampled but the signals-of-interest are modulated onto that RF signal and filtering and signal processing techniques allow the module to extract those signals-of-interest. The digitization process can be gated, singly triggered or triggered for a specified number of samples by the SYNC signal. SYNCs are generated in the BPM Timing Fanout Module and normally initiated with respect to the Tevatron-wide TCLK signal which carries Main Control Room (MCR) commands and state information. There are two TCLK decoders, called UCD modules) in a given house; one PCMUCD on the sub rack controller, in a PMC slot, and one on the BPM Timing Fanout Module. The TCLK decoder on the BPM Timing Fanout Module can initiate digitizing sequences based on selected TCLK commands and can add fixed delays, with a resolution of one RFClk period, in order to remove cable delays (w/ a resolution of one RFClk period) or to time-in similar actions between the widely separated service buildings around the Tevatron ring. The ACNET/MOOC software infrastructure and applications can also be triggered by interrupts generated by the same or other TCLK signals that are decoded by the PMUCD card and this is discussed in detail in front-end software design document (#1067).

Beam Loss Monitor

The BLM analog circuitry and digitizers are in separate analog crates and the data is readout into the VME sub rack through a bus interface designed into the Timing Module or through a COTS digital I/O PMC board. The BLM appears ³as a read-write memory block over the External Device Bus (EDB). The VME sub rack processor writes to specific memory locations to set up and control the BLM hardware and reads from specific locations to acquire BLM data and status.

³ **BLM Data Structures and General Information (Beams-Doc-764)**

BPM Requirements

The requirements for this system are based on the system requirements documented in Tevatron BPM Upgrade Requirements Document (Beams Doc #554). A summary of the functional requirements are:

- Continuous closed orbit sampling with ~ 1kHz of IF bandwidth and 500 Hz measurement rate.
- Closed orbit position should be stable for single bunch, multiple bunches and uncoalesced bunches.
- Turn-by-turn sampling with ~ 100 kHz of IF bandwidth and 47 kHz measurement rate. Store 8192 points/turn-by-turn request.
- Simultaneous measurement of protons and pbars. Measure pbars with closed orbit sampling and proton de-convolution (no change from closed orbit sampling) or use short gate sampling.

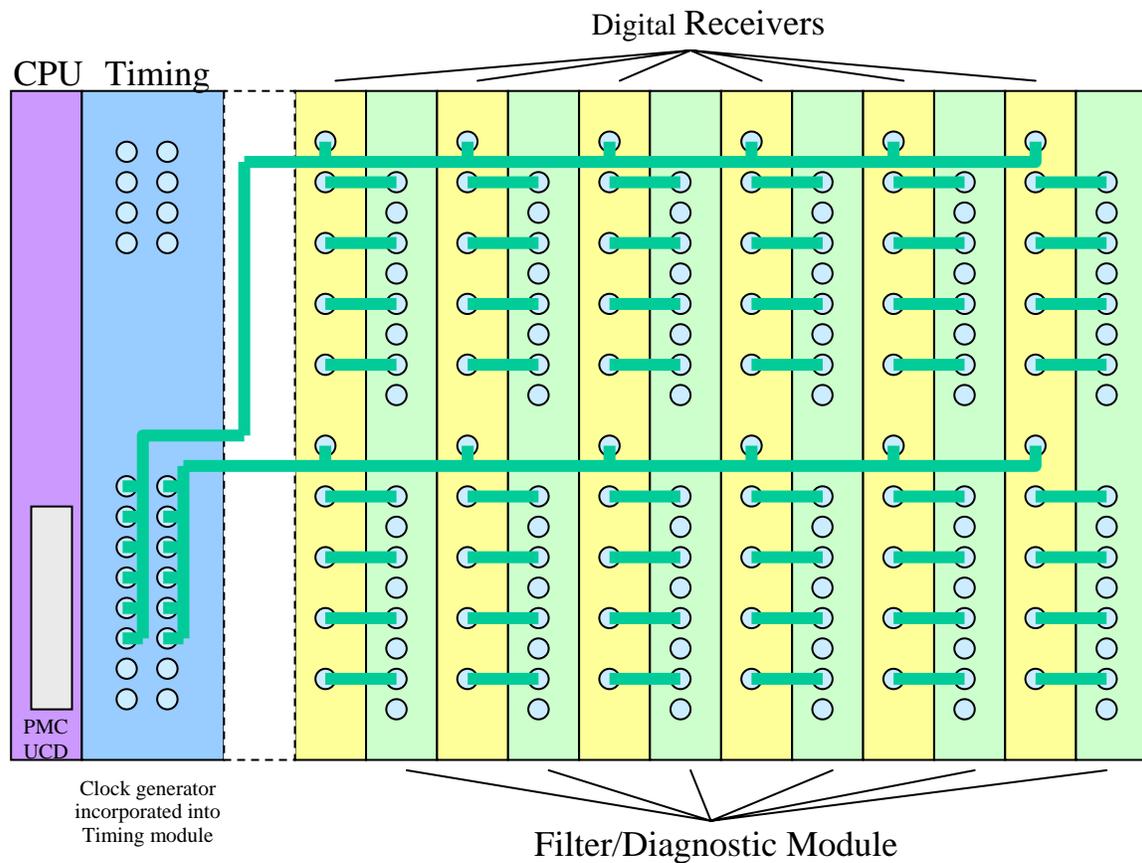


Figure 2 Sub Rack Module Example

Data Acquisition Operation

Functional Overview

The communication between the front-end processor and the Echotek modules happens through the VME backplane. For the BLMs, data is exchanged through a digital I/O interface on the timing board or as an I/O daughter board on the sub rack processor.

Data coming from the BPM and BLM digitizers are stored into a set of buffers in the sub rack controller. The depth and number of logical buffers that reside on the sub rack controller is defined in the Data Register document (Beams Doc #903). Some of the buffers, most notably the turn by turn data, is first stored in memory on the Echotek boards and then transferred to the sub rack controller on demand, as the processor/backplane does not have the bandwidth to acquire it in real time. The actual physical implementation of the sub rack controller buffers will be described in the front-end software design document (Beams Doc #1067).

Filter/Diagnostic Module

The Filter/Diagnostic Module (FDM) conditions the signals from the Tevatron BPM sensors for input to the Data Converter Module. It also provides for injecting a diagnostic signal back into the sensor, into the Data Converter Module, or both. Schematics for the Filter Card are in Appendix x.

The Filter Card has eight channels so that one module is required for each Data Converter Module. Each channel (Figure x) consists of an attenuator network, a band pass filter, and two relays. The BPM signals enter and exit via SMB connectors on the front panel.

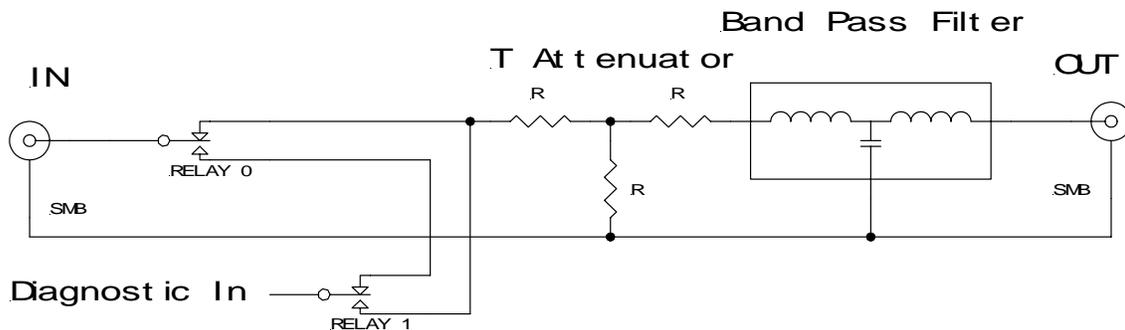


Figure 3 Filter Card BPM Channel Block Diagram

The Timing Generator Fanout Card (TGF) controls the relays and provides the diagnostic signal via bused TTL lines on the VME backplane. The Filter Card has a three position DIP switch to set the card address. This allows up to eight modules per sub rack. The Timing Card interface consists of the following lines:

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- TFO_A(0-2) – Module Address lines from the TFO.
- TFO_CS* – Card Select line From the TFO, active low.
- TFO_CLK – Clock line from the TFO (2 MHz maximum).
- TFO_DOUT – Serial Data from the TFO.
- TFO_DIN – Serial Data to the TFO.
- TFO_RST* – Reset signal from the TFO, active low.
- TFO_DIAG – Diagnostic signal from the TFO.
- TFO_SP(0-3) – Spare outputs from the TFO.
- TFO_SPIN – Spare input signal to the TFO.

The TFO configures the relays by sending a 16 bit serial word to the Filter Card. It Drives the A(0-2), CS* to select a module and then clocks out the 16 serial bits RC(0-15) MSB (RC15) first as shown in Table 2. It then raises the CS* line to complete the operation. The state of the relays is changed on the rising edge of the CS* signal. R0 and R1 are the control bit for the relays shown in Figure 3. If the bit is a one the relay is activated and switches to the normally open connection. Otherwise it is in the normally closed position.

Table 2

Ch8		Ch7		Ch6		Ch5		Ch4		Ch3		Ch2		Ch1	
R1	R0	R1	R0	R1	R0	R1	R0	R1	R0	R1	R0	R1	R0	R1	R0
RC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RC0

The Filter Card receives the TTL diagnostic signal from the TFO, buffers it, sends it through a low pass filter and then distributes it on a bus to buffers on each of the eight channels.

The Filter Card has the following LEDs on the front panel:

- SEL – Indicates that the card is currently being address by the TFO (yellow).
- SW(0-2) – Indicates the setting of the address switches (green).
- 5V, 12V, -12V – Power supply indicators (green).

Data Converter Module

The Echotek module ECDR-GC814/8-FV2 is the baseline data converter. This module belongs to a general type of modules called Digital Signal Receivers (or Radios) (DSR). These modules have high speed digitizers that convert the analog radio frequency inputs into digital information very early in the module. The following digital circuitry is used to down convert or base band the RF information, removing the high frequency carrier (53 MHz in this case) and revealing the information modulated onto that carrier, 48 KHz revolution information, 20 KHz betatron signals etc. The base banded signals are filtered in n stages of digital FIR filters and the output data is stored in a First-in-first-out

memory on the module. The sub rack processors can readout the data memory over the sub rack VME backplane.

The data sheets for module are in the Appendix as Echotek DSPR Module.

BPM Timing Generator Fanout (TGF) Module

The Timing Generator Fanout (TGF) is a double width, 6U VME card that generates timing signals that control and initiate acquisition of the BPM signals. The timing signals are based on inputs from the accelerator controls clock system. These signal inputs include the Tevatron Beam Sync clock (TVBS), the Tevatron event clock (TCLK) and the Main Ring RF Clock (RFClk). The RFClk is the synchronization clock for the major functionality of the BPM Timing Generator Fanout Module (TGF). The RFClk is used to over sample and decode the TVBS and TCLK signals. The TVBS base frequency is the same as the rate of the bunches in the Tevatron (7.5 MHz) and the revolution timing mark (0xAA, also called BSync) is encoded on the carrier and can be extracted from it. The revolution timing mark allows synchronization with whole cycles of the train of particles circling around the Tevatron ring. The TCLK signal is very similar to TVBS with a 10MHz carrier frequency and from it the module can extract a large number of commands from the Main Control Room and changes in the state of the Tevatron. The TGF can be set to look for up to eight specific commands at any one time.

For each Echotek Data Converter module the BPM Timing Fanout Module (TGF) creates a time base clock that paces the data conversions and filtering on the board as well as supplies a gate or trigger signal for control of the data inputs. For the Tevatron BPM system, the TGF multiplies the RF clock frequency by exactly 7/5 to produce the digitization clock. The RF frequency shifts as the energy of the beam changes. At approximately 980 GeV the RF clock frequency is typically 53.10468 MHz which produces a digitization rate of 74.346552 MHz.

Gate/triggers will typically be based on the revolution timing mark so that the signals can be related to the particle bunches and measurements in separate service buildings can be related to each other as necessary.

The Hardware Timing Module inputs are:

- RFCLK - Main Ring RF Clock (53.10468 MHz)
- TVBS – Tevatron Beam Sync is an approximately ~7.5 MHz carrier with a modified Manchester encoding of beam specific events.
- TCLK – Tevatron Clock, a 10 MHz carrier modulated by a fixed protocol of bit patterns that can carry commands and data events to electronics associated with the Tevatron.
- MDAT – A 10 MHz carrier modulated like TCK to carry additional data and events. Not required for BPM project.
- An External Trigger Input – Permits the TVBS decoding to be bypassed by creating a hard trigger rather than a decoded trigger. Used for testing and future expansion.
- BLM External Device Bus – actually bidirectional but predominately a readout link for data from the BLM Analog Box that processes the signals from the BLM sensors.

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The Hardware Timing Module outputs are:

- A2D Clock signals [0-7] – the digitization clock to the Echotek modules
- A2D Sync signals [0-7] - the synchronization for a sequence of digitization
- Diagnostic clock – A 53.104 MHz clock to the Filter/Diagnostic board for the diagnostic functions. This signal is routed on the VME backplane.
- An External Trigger Output –Allows an external device to be triggered from a internal firmware trigger condition such as a decoded BSync event. Used for testing and future expansion.
- DAC Output –14-bit DAC for testing and possible future expansion
- VME Interrupts for signaling the sub rack controller.
- Backplane connections that allow the TGF to control the Filter/Diagnostic modules. These lines will also allow a level of auto-detection on a per sub rack basis so that the TGF will ‘know’ how many FDMs there are to control.

The A2D gate signal variations are:

- TCLK trigger direct
- TCLK + programmable delay
- TCLK + repeated programmable delay
- TVBS trigger direct AA detect.
- TVBS + programmable delay
- TVBS + repeated programmable delay
- External Input Triggered – Similar to above TCLK or TVBS except it is a direct trigger and bypasses the Manchester decoding section.

The sub rack controller can be programmed to read out BPM/BLM values based on a specific TCLK signal (e.g. TCLK \$77 which is a TeV Flash command). The sub rack controller does not receive Tevatron Beam Sync (TVBS) events. In the sub rack controller, the preparation for digitization and read out is signaled by an arm event. An arm event is usually originated by commands from the MCR. For example, a turn by turn measurement could be armed by a TCLK command or state change and then started on the next ‘AA’ turn marker plus a pre-programmed delay.

The overall TGF firmware will not be changeable remotely. The board and programmer workstation or laptop will need to be directly connected together to change the firmware. However the functional programmability is controlled by the following registers that are accessible over the VME bus by the sub rack controller.

BPM Timing Generator Fanout - Register Map from Offset = 0h

Register Number	I/O Address	Register Name	Register width	Effective width	
0	0x00	Acquisition Bucket Delay 0	16-bits	11-bits	R/W
1	0x02	Acquisition Bucket Delay 1	16-bits	11-bits	R/W
2	0x04	Acquisition Bucket Delay 2	16-bits	11-bits	R/W
3	0x06	Acquisition Bucket Delay 3	16-bits	11-bits	R/W
4	0x08	Acquisition Bucket Delay 4	16-bits	11-bits	R/W
5	0x0A	Acquisition Bucket Delay 5	16-bits	11-bits	R/W
6	0x0C	Not Used	16-bits	11-bits	R/W
7	0x0E	Not Used	16-bits	11-bits	R/W
8	0x10	Gate Count 0	16-bits	11-bits	R/W
9	0x12	Gate Count 1	16-bits	11-bits	R/W
10	0x14	Gate Count 2	16-bits	11-bits	R/W
11	0x16	Gate Count 3	16-bits	11-bits	R/W
12	0x18	Gate Count 4	16-bits	11-bits	R/W
13	0x1A	Gate Count 5	16-bits	11-bits	R/W
14	0x1C	Not Used	16-bits	11-bits	R/W
15	0x1E	Not Used	16-bits	11-bits	R/W
16	0x20	Not Used	16-bits	11-bits	R/W
17	0x22	Not Used	16-bits	11-bits	R/W
18	0x24	Not Used	16-bits	11-bits	R/W
19	0x26	Turn Scaler for Background	16-bits	11-bits	R/W
20	0x28	Mdat Type	16-bits	8-bits	R/W
21	0x2A	Mdat Frame Value	16-bits	16-bits	R/W
22	0x2C	Mdat scale factor			Read
23	0x2E	Pre-Trigger Delay All	16-bits	6-bits	R/W
24	0x30	Control		See Table 5	R/W
25	0x32	Status	16-bits	See Table 6	Read Only
26	0x34	Bsync Turn Event	16-bits	8-bits	Wait on read/W
27	0x36	Bsync Start Event	16-bits	8-bits	R/W
28	0x38	Diagnostics Counter	16-bits	16-bits	Read Only
29	0x3A	Diagnostic Counter w/ wait	16-bits		Wait on read
30	0x3C	MDAT Data sampled	16-bits		

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		on Start			
31	0x3E		16-bits		
32	0x40		16-bits		
33	0x42		16-bits		
34	0x44		16-bits		
35	0x46		16-bits		
36	0x48		16-bits		
37	0x4A		16-bits		
38	0x4C		16-bits		
39	0x4E	Switch	16-bits		Read Only
40	0x50		16-bits		
41	0x52		16-bits		
42	0x54		16-bits		
43	0x56		16-bits		
44	0x58		16-bits		
45	0x5A		16-bits		
46	0x5C		16-bits		
47	0x5E		16-bits		
48	0x60	Irq Vector Reg 1	16-bits	See Figure 4	R/W
49	0x62	Irq Vector Reg 2	16-bits	See Figure 4	R/W
50	0x64		16-bits		
51	0x66		16-bits		
52	0x68		16-bits		
53	0x6A		16-bits		
54	0x6B		16-bits		
55	0x6C		16-bits		
56	0x70	IRQ1 Source Mux	16-bits	See Table 4	R/W
57	0x72	IRQ2 Source Mux	16-bits	See Table 4	R/W
58	0x74		16-bits		
59	0x76		16-bits		
60	0x78		16-bits		
61	0x7A		16-bits		
62	0x7C		16-bits		
63	0x7E		16-bits		

Note: Aggregate Delay Registers located at I/O addresses 0x3A through 0x5E have been deleted
1/15/2003 CRM

Table 4 IRQ SOURCE MUX		I/O Address 0x70..0x72	
DATA	SOURCE		
0x00	Null		

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0x01	Start Event		
0x02	Revolution Event		
0x03	MDAT Type Match		
0x04	Turn Counter Trigger Out		
0x05	Delay Timer Enabled		
0x06	Delay Timer Trigger		
0x07	Delay Timer Terminal Count		
0x08	Turn Counter Trigger		
0x09	Periodic timer (BGFlash rate)		

INTERRUPT STATUS/ID REGISTER DETAIL (Eight instances)

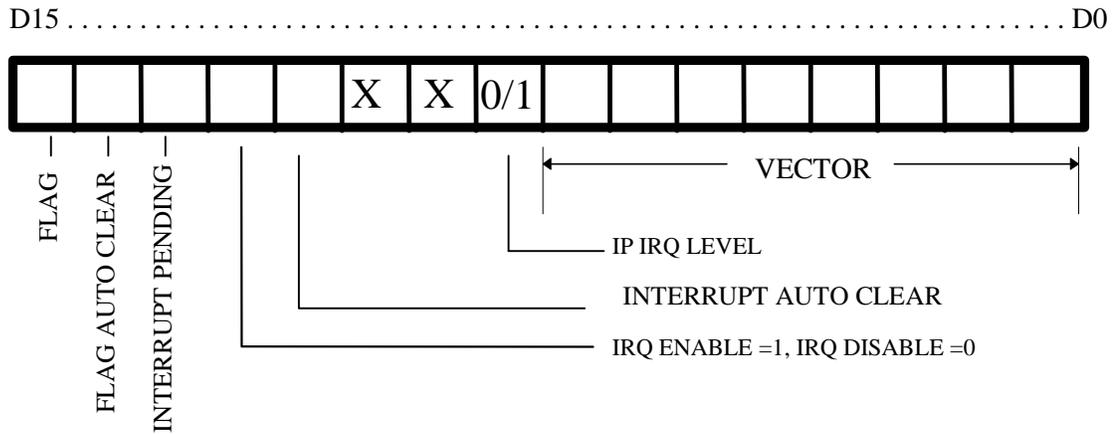


Figure 4

Table 5	CONTROL AND MODE REGISTER		I/O Address 0x30
DATA			
Low Byte			
0xXX01	Control[0]	Enable Pre-Trigger Counter	Zero = Disabled, One = Enabled
0xXX02	Control[1]	Enable Delay Timer	Zero = Disabled, One = Enabled
0xXX04	Control[2]	Not Used	
0xXX08	Control[3]	Enable MDAT DATA	
0xXX10	Control[4]	Trigger Source	Zero = PreTrigger, One = External,
0xXX20	Control[5]	Trigger Source	Two = Start Event
0xXX40	Control[6]	“Start” Source	Zero = Start Event, One = Null ,
0xXX80	Control[7]	“Start” Source	Two=Turn Scaler (periodic)

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High Byte			
0x01XX	mode[1]	Not Used	
0x02XX	mode[2]	Not Used	
0x04XX	Control[10]	Enable Beam Sync	Zero = Disabled, One = Enabled
0x08XX	Control[11]	Enable MDAT	Zero = Disabled, One = Enabled
0x10XX	Control [12]	Single/Repetitive gate out	Zero = Repetitive, One = Single
0x20XX	Control[13]	Reset Mdat Decoder	Zero = No action, One = Reset
0x40XX	Control[14]		Zero = Disabled, One = Enabled
0x80XX	Control[15]	Reset TSG	Zero = No action, One = Reset

Table 6	STATUS REGISTER BIT	I/O	Address
DATA	DEFINITIONS	0x32	
Bit-0	Turn Marker		
Bit-1	Start Marker		
Bit-2	Mdat Frame valid		
Bit-3	Mdat Parity Error		
Bit-4	Bsync Parity Error		
Bit-5	Mdat Strobe		
Bit-6	Mdat Enabled		
Bit-7	Mdat Clock		
Bit-8	Turn Counter Enabled		
Bit-9	53MHz present		

Table 7	Change trigger source to:	IP-TSG INPUT OUTPUT DEFINITIONS	SIGNAL ALIAS	ALTERA PIN OUT	IPTSG I/O
SIGNAL NAME		TEST POINT			
"MDAT_IN"				45	P2-45
"extTrigger"				199	P2-26
"bsync_in"				30	P2-44
"53Mhz"				79	P2-46
"tc0"	Trigger 23			167	P2-5
"tc1"	Trigger 22			168	P2-6
"tc2"	Trigger 21			94	P2-7
"tc3"	Trigger 20			103	P2-8
"tc4"	Trigger 3			89	P2-9
"tc5"	Trigger 2			40	P2-10
"tc6"	Trigger 1			143	P2-11

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"tc7"	Trigger 0			195	P2-12
"tc8"	Trigger 27			121	P2-13
"tc9"	Trigger 26			120	P2-14
"tc10"	Trigger 25			166	P2-15
"tc11"	Trigger 24			202	P2-16
"tc12"	Trigger 7			12	P2-17
"tc13"	Trigger 6			62	P2-18
"tc14"	Trigger 5			14	P2-19
"tc15"	Trigger 4			192	P2-20
"tc16"	Trigger 31			186	P2-21
"tc17"	Trigger 30			15	P2-22
"tc18"	Trigger 29			187	P2-23
"tc19"	Trigger 28			190	P2-24
"ADCTrigger/"				86	P2-25
Start Event		TP1	IRQ Source 1	39	P2-1
Turn Event		TP2	IRQ Source 2	158	P2-2
MDAT Type Match		TP3	IRQ Source 3	99	P2-3
Turn Counter Trigger Out		TP4	IRQ Source 4	164	P2-4
Delay Timer Enabled		TP5	IRQ Source 5	149	P2-39
Delay Timer Trigger		TP6	IRQ Source 6	28	P2-40
Delay Timer Terminal Count		TP7	IRQ Source 7	150	P2-41
Turn Counter Trigger		TP8	IRQ Source 8	13	P2-42
IP IRQ 0		TP9		147	P2-37
53/2 Mhz		TP10		10	P2-38
Mdat Strobe		TP11		127	P2-35
Bsync Strobe		TP12		148	P2-36
CS[7]		TP13		24	P2-33
ip_ack		TP14		16	P2-34
IP Cycle wait		TP15		71	P2-31
mValidFrame		TP16		57	P2-32
mdat Parity Error		TP17		63	P2-29
mvalid		TP18		19	P2-30
sclock		TP19		163	P2-27
sdata		TP20		85	P2-28
2xclock		TP21		36	U1-12

INTERRUPT CONTROL BIT	DEFINITION
8	IRQ LEVEL: ZERO OR ONE
9	NA
10	NA
11	INTERRUPT AUTO CLEAR
12	INTERRUPT ENABLE

13	NA
14	FLAG AUTO CLEAR
15	FLAG

TIMER COUNTER

A 16-bit counter with 200ns resolution exists at I/O address location 0x38. The counter is read-only. The counter will be reset to zero upon the occurrence of the START event. Note: writing a value to I/O location (xx Bill finish xx)

Sub Rack Processor Module

The sub rack controller CPU board is responsible for establishing the communication link between user applications and the Echotek modules. All control and data transferred to/from the BPM modules pass through the sub rack controller.

Data Acquisition Operations

BPM Measurement types

Rewrite this for the hardware perspective of bandwidth and data rate. There are two different types of measurements that can be made from the data in the digitizing cards. The data types are:

- Closed Orbit Measurements, also called Frame data. Frame data is an average of n measurements. The average is *usually* based on 8, 16, 32 or 64 single turn measurements, and is configurable. Frame data is the only data measurement made in normal operation mode. **Note:** the number used in the averages for normal operation mode is not necessarily the same number as in injection mode.
- Turn Data is the instantaneous single value (i.e., not averaged over n readings) of the sensors once the trigger is received. The BPM DA must operate in a Turn by Turn mode (TbyT) where a large number (8096?xx) of sequential turns are sampled without missing a turn. Then the DA can stop sampling, read-out the data from the A2D modules and do whatever processing and telemetry is necessary. Normal TbyT mode is continuous cycling between TbyT sampling and readout activities.
- A third mode is a variation on Turn by turn mode where a single measurement is acquired by

It is important to note that for turn measurements, all BPMs are triggered off the same bunch. However, for a closed orbit measurement, the specific bunches used in the averaging can be different across BPMs.

The data acquisition system must support systematic triggering of N events for both of these data types. For turn buffers, the arrays are of N consecutive measurements (i.e., Turn by Turn). On the other hand, closed orbit buffers are built by a N triggers of a specific type.

The measurement types require different setups in the Echotek DDC modules, and, therefore have a time penalty associated with changing setup. In general the data acquisition modes must switch to acquire a different type of measurement.

BPM Data Acquisition Modes

There are different modes of BPM data acquisition. These modes are mutually exclusive due to the necessity to configure the filters and timing in the Echotek modules for a specific mode. The modes are:

- Closed Orbit operation.
- Injection
- Turn by Turn
- Diagnostic
- Calibration

The modes are described in more detail in the following sections. The buffers are described in the Software specifications document.

Closed Orbit operation

This is the default mode of the data acquisition system. The 53 MHz signal from the BPM sensors is sampled by the 74 MHz digitization clock. These digital samples are down converted using a 21 MHz clock in order to select the modulation signals riding on the 53 MHz sensor signal. The resulting signal is band limited at 48 KHz to approximately 100 Hz bandwidth which averages together many turns of the accelerator particles. The resulting samples come out of the Echotek module at a xx Hz rate. The samples are stored in the output memory of the Echotek module until xx. The sub rack controller is then interrupted and the data is readout to be handled by the sub rack controller software.

The arming and triggering of the mode has not yet been specified.

Turn by turn

Turn by turn mode is used to take a sample every turn of the particle bunches in the accelerator, approximately every 21 microseconds. The 53 MHz signal from the BPM sensors is sampled by the 74 MHz digitization clock. These digital samples are down converted using a 21 MHz clock in order to select the modulation signals riding on the 53 MHz sensor signal. The resulting signal is band limited at 48 KHz to approximately 1 KHz bandwidth which produces a sample per turn. The resulting samples come out of the Echotek module at a xx Hz rate. 8K consecutive turns are taken and stored in the Echotek output buffer when a turn by turn request is made. At the end of the sampling

the sub rack controller is interrupted and the data is readout to be handled by the sub rack controller software.

The arming and triggering of the mode has not yet been specified.

Injection

Injection is a special type of turn by turn mode used to sample the first pass of a particle bunch. It is most often used when proton bunches are first introduced into the Tevatron. Only one sample is taken per data acquisition cycle and the timing of the data is set up carefully before the particles arrive at the BPM sensor. Injection mode needs to be disabled and re-enabled on request because there are times when closed orbit data is preferred during proton injection.

The arming and triggering of the mode has not yet been specified.

Diagnostic Mode

Normal or turn by turn modes can be used. The diagnostic signal is enabled and the relays in the Filter/Diagnostic module are activated to either inject the diagnostic signal out the input connector toward the sensor or out the output connector toward the Echotek module. Multiple channels can be driven at the same time but the data collected will be hard to interpret if more than one of the four connections to a specific BPM sensor has the diagnostic signal imposed on it. The best configuration is for one of the four connections to be driven and the four associated Echotek channels are recorded. If the signal is directed toward the sensor, the specific Echotek channel that was disconnected from the sensor should have no input and show local background noise while the other three channels of that sensor will have diagnostic signal that is coupled through the sensor itself. This will test the wiring to the sensors and the sensor itself. If all four connections to the sensor are diagnosed this way a complete picture of the health of the sensor and its wiring will be collected. If the diagnostic signal is directed toward the Echotek input that channel can be tested and a general calibration collected. All of the Echotek connection to the Filter/Diagnostic board can be tested this way.

BLM Operations

The BLMs are functionally simple devices with relatively long time constants from the BPM perspective. They are self paced and require very little control. BLM values are read out periodically on triggers as programmed in the DA application. The data are always available although they may not have updated since the previous read. There is no need for mode switching for BLMs and there are no turn by turn requirements. The BLM sub rack is read out through an External Device Bus (EDB), a parallel, bidirectional connection. The control, configuration and readout of the BLM devices is done through memory mapped registers within the EDB address space.

The External Device Bus is described in Beams document #772, Beam Loss Monitor System Description. The register structure is described in Beams document #764, BLM Data Structures and General Information

The upgrade project will provide the functional connection through the crate control through the EDB to the BLM Analog sub rack such that the BLM system appears identical to the existing system.

Appendix

Schematics, Layouts and drawings.

Timing Module

Schematic: Beams Document #xx

Layout: Beams Document #xx

Filter/Diagnostic Module

Schematic: Beams Document #1244

Layout: Beams Document #xx

Filter Specifications

Beams Document #1065

Sub rack Documentation

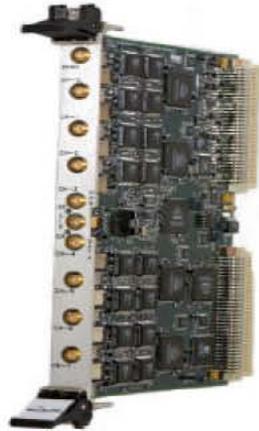
Beams Document #1245

Echotek DSPR Module



**EIGHT CHANNEL
ANALOG TO DIGITAL CONVERTER
WITH DIGITAL RECEIVER**

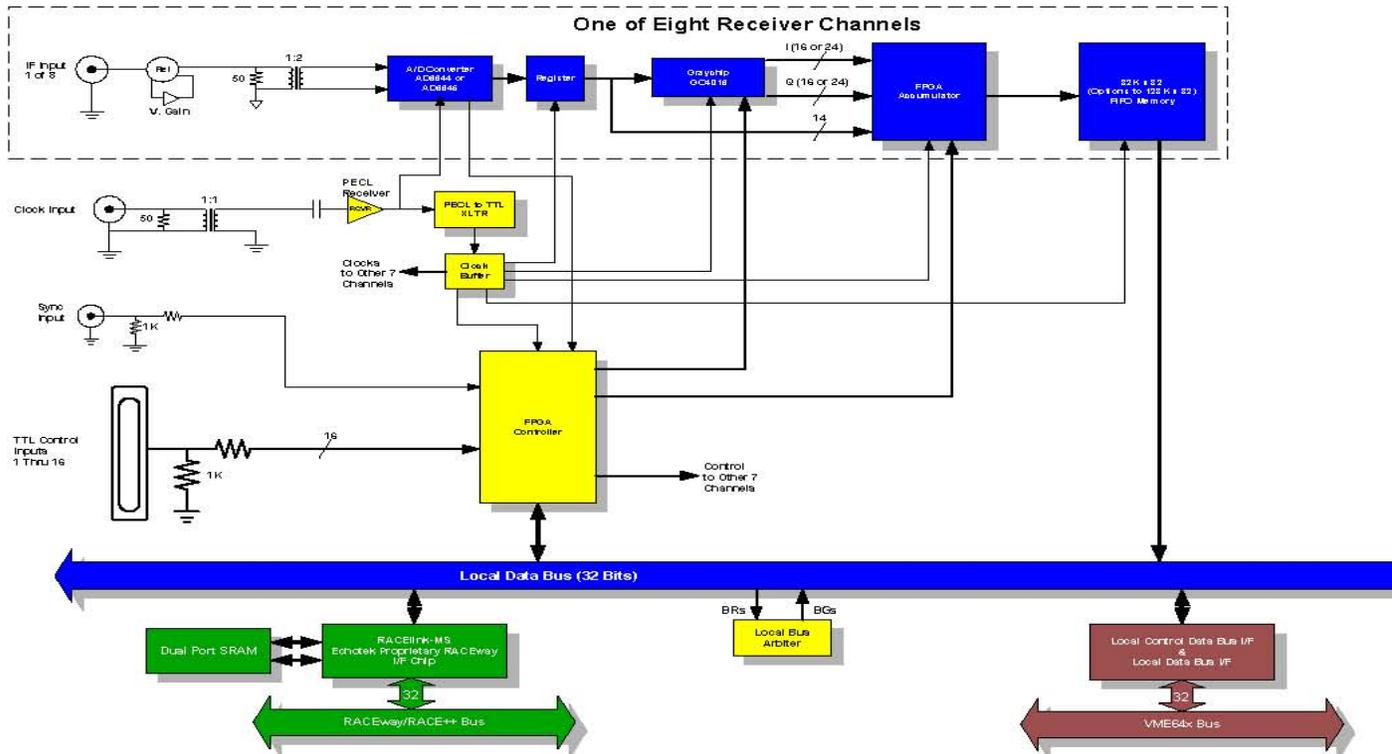
ECDR-GC814



FEATURES

- * 8 IF INPUTS
- * SIMULTANEOUS SAMPLING
- * EIGHT ANALOG TO DIGITAL CONVERTERS (ANALOG DEVICES AD 14 BIT, 65 MSPS, OR AD6845 FOR SAMPLING RATES TO 105 MHZ)
- * SFDR > 90 dB FS
- * 8 RECEIVER CHANNELS (GRAYCHIP GC4016)
- * DECIMATION RANGE 8-16K/CHANNEL
- * HEADER INSERTION
- * VME 64X, SINGLE SLOT
- * RACE++™ OUTPUT
- * ALSO AVAILABLE AS TWO OR FOUR CHANNEL MODEL
- * AVAILABLE AS A/D CONVERTER ONLY AS AN 8, 4, OR 2 CHANNEL
- * VARIABLE GAIN (~ -10 TO +20 dB)

ECDR-GC814 BLOCK DIAGRAM



ECHOTEK CORPORATION 555 SPARKMAN DRIVE #400 HUNTSVILLE, AL
35816 PHONE 256 721 1911 FAX 256 721 9266 E-MAIL: sales@echotek.com
ECCR-GC814

This analog to digital converter and digital drop receiver board provides eight channels of 14 bit, 105 MHz analog to digital conversion and digital processing suitable for wideband and narrowband down conversion and filtering in a single 6U VME slot. Data decimation range of each receiver channel is user programmable from 8 to 16384. The receiver section of each channel may be bypassed to output raw A/D data.

Data Inputs

Up to eight analog signals may be input to this board via front panel SMA connectors. Each signal is converted using Analog Devices AD6644, 14 bit, 65 MHz A/D converters or AD6645 for sampling rates to 105 MHz. Direct digitization for IF's > 200 MHz are supported. These high quality analog to digital converters exhibit Spur Free Dynamic Ranges in excess of 90 dBFS.

Clocks

The A/D clock is provided by the user via front panel SMA connector. This clock signal (sine wave into 50 ohms) is buffered and distributed to all eight channels so that all channels are sampled simultaneously.

Other Inputs

The user may also input a sync signal through the front panel and up to 16 bit wide digital word - normally used to insert a header into the data stream or for tagging data.

Receiver Channels

The digitizer outputs from each A/D converter interfaces to the input crossbar switch on the Graychip GC4016 multi-standard quad digital down converter chip. A receiver channel block diagram is shown below for clarity - the Graychip GC4016 contains four such channels that can be combined as mentioned below, only one Graychip 4016 channel or channel combination is output per receiver channel on the ECCR-GC814.

The ECCR-GC814 supports the various channel combination configurations allowed by the Graychip 4016, that is: Sample Accumulator :

A	No channels combined. In this mode, each channel supports decimations from 32 to 16384.
B	Channel pair combinations supports decimations of 16 to 8192 while in this mode
C	Four channel combination resulting in one wideband output channel:
	- supports decimations of 8 to 4096 while in this mode.

The output of the receivers, or the A/D converter (in receiver bypass mode) is directed to an FPGA that outputs the sum of a programmed number of samples. The output may be the sum of 1, 2, 4, 8, 16, 32, 64, 128, or 256 raw A/D samples or I's or Q's.

FIFO Buffer

Tevatron BPM Hardware Specifications

Data is output from the sample accumulator to each channel's FIFO buffer. The FIFO buffer is 16K x 32 bits (by default) and may be configured at the factory as large as 128K x 32 bits.

Data Output

Data, raw A/D output, complex receiver data, or either of the quadrature components, is output via the RACE++ interface. The data may also be output via the VME64X interface - but this interface was designed to be used for control in real time and, therefore, is not optimized for high speed data transfer.

Operating Modes

The ECDR-814 supports both CW and pulsed system applications. The board may be controlled in one of two basic operating modes:

Gate Mode - Data acquisition occurs when the gate signal is active. The gate signal may be provided via external front panel input or a software write.

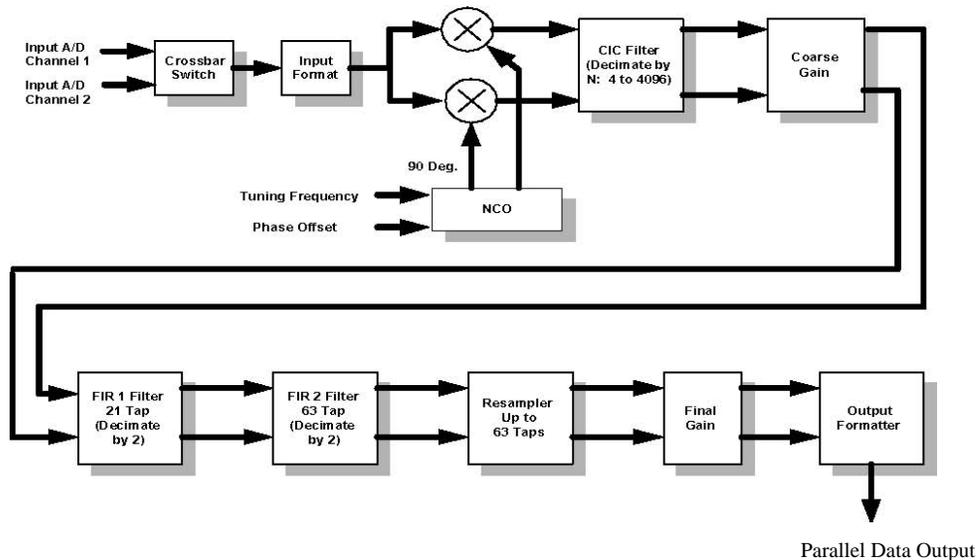
Counted Burst - A preprogrammed number of samples are acquired and processed with each occurrence of an external trigger pulse. This trigger pulse also has a software bit counterpart associated with it.

Set-Up and Control

All set-up and control registers are accessible via the VME interface. Additionally, the RACE++ interface may be programmed by either VME or RACE++ and can be a RACE++ master or slave.

Driver Support

Drivers are supplied for VxWorks Operating Systems.



Ordering Information

Model	Part Number	Ruggedization	Options
ECDR-GC814/8	12-0050/CC334A	Commercial	65 MHz A/D, 16K FIFO
ECDR-GC814/8	12-0050/CC335	Commercial	65 MHz A/D, 128K FIFO
ECDR-GC814/8-80	12-0050/CC450	Commercial	80 MHz A/D, 16K FIFO
ECDR-GC814/8-80	12-0050/CC512	Commercial	80 MHz A/D, 128K FIFO
ECDR-GC814/8-105	12-0050/CC495	Commercial	105 MHz A/D, 16K FIFO
ECDR-GC814/8-105	12-0050/CC496	Commercial	105 MHz A/D, 128K FIFO
ECDR-GC814/4	12-0057/CC339	Commercial	65 MHz A/D, 16K FIFO
ECDR-GC814/4	12-0057/CC337	Commercial	65 MHz A/D, 128K FIFO
ECDR-GC814/4-80	12-0057/CC494	Commercial	80 MHz A/D, 16K FIFO
ECDR-GC814/4-80	12-0057/CC451	Commercial	80 MHz A/D, 128K FIFO
ECDR-GC814/4-105	12-0057/CC477	Commercial	105 MHz A/D, 16K FIFO
ECDR-GC814/4-105	12-0057/CC497	Commercial	105 MHz A/D, 128K FIFO
ECDR-GC814/2	12-0058/CC350	Commercial	65 MHz A/D, 16K FIFO
ECDR-GC814/2	12-0058/CC498	Commercial	65 MHz A/D, 128K FIFO
ECDR-GC814/2-80	12-0058/CC420	Commercial	80 MHz A/D, 16K FIFO
ECDR-GC814/2-80	12-0058/CC340	Commercial	80 MHz A/D, 128K FIFO
ECDR-GC814/2-105	12-0058/CC499	Commercial	105 MHz A/D, 16K FIFO
ECDR-GC814/2-105	12-0058/CC500	Commercial	105 MHz A/D, 128K FIFO
LED OPTION:			
ECDR-GC814/8-DC	12-0107/CC426	Commercial	65 MHz A/D, 16K FIFO
ECDR-GC814/8-DC	12-0107/CC431	Commercial	65 MHz A/D, 128K FIFO

Tevatron BPM Hardware Specifications

Model Part Number Ruggedization Options

ECDR-GC814/4-DC 12-0108/CC427 Commercial 65 MHz A/D, 16K FIFO

ECDR-GC814/4-DC 12-0108/CC432 Commercial 65 MHz A/D, 128K FIFO

Shock Levels	Temp (°C)	Temp (°C)	Vibration	Shock	Humidity	Notes
	with 300ft./min airflow		from 10 to 2000Hz random sinusoidal from 5 to 500 Hz	saw tooth, 1000g duration	100% RH	Grade, cooled by blown air, for use in beam lines and software development applications

814/2-DC		12-0109/CC428		Commercial		65 MHz A/D, 16K FIFO
814/2-DC		12-0109/CC433		Commercial		65 MHz A/D, 128K FIFO