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Tevatron Beam Position Monitor (BPM) Upgrade Echotek ADC Board Testing

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Abstract

This document outlines the plan and necessary procedures for the pilot board acceptance tests of the modified Echotek ADC boards for the Tevatron Beam Position Monitor (BPM) upgrade. All of these tests should have been exercised with the existing board, or well prepared with the expected modifications, before the 4 example boards arrive in early June. These tests should be completed within 2 weeks of the arrival of the new boards, and a conclusion reached regarding whether or not the new boards can meet our present and possible future needs, and therefore whether or not the design can be released for production. A portion of these tests will likely morph into production acceptance tests. They will be identified in the text.

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Overview

Compared to the Recycler version, model “ECCR-GC814-FV”, the new Echotek ADC boards, model “ECCR-GC814-FV-A”, referred as the Tevatron version hereafter, will have a few hardware, and hence layout, changes. The goal of the pilot acceptance tests is to check a few basic functions and verify that the board layout is ok. More thorough and systematic tests can be done after the acceptance tests.

Details of the modifications include:

- front panel connectors from SMA to SMB;
- FIFO chip replaced by SRAM for the channel outputs;
- VME interface chip from Cypress CY7C961 to Tundra Universe II (CA91C142);
- ability to reload the FPGA flash through VME or JTAG.

With the 4 example boards, the SRAMs will be configured as FIFOs to minimize the needs to change our daq software, including the driver, so the testing can quickly start. The following sections document a collective knowledge, mainly from the Recycler BPM project, about how we want/need/choose to test the new boards:

1. Check the input impedance;
2. Verify basic VME read and write, perform the demo counting test with the Echotek supplied driver to verify the Echotek driver works and check the data path;
3. Incorporate necessary changes into Duane/Charlie’s existing “ecdrgc814multibrd” driver and perform their tests to verify the new multi-board driver works;
4. Perform the existing PREP quality control tests with the new “ecdrgc814multibrd” driver and repetitive external trigger;
5. Verify the ability to re-program the FPGA flash.

Here, tests 1 and 5 are independent of the others and hence can be performed with one of the boards while other tests are done with the 3 other boards, and done in the order listed. Test 2 is our first step and baseline because it uses only the Echotek supplied driver, with none of our modifications/additions. Test 3 can be run only when the Echotek driver

works, and when all our modifications/additions are done correctly. Test 4 uses repeated hardware triggers and analyses the data with real time graphing.

Check the input impedance

Goal:

Check the deviation of the input impedance from 50 Ohm for each channel, concentrating on the frequency range from 30 to 70 MHz.

Pass Criterion:

Smooth response, no rapid deviations of over +/- 10% from 50 Ohm, over the testing frequency range. Note: board is powered.

Required Hardware:

- Network analyzer
- Power Supply

Required Software:

None

Performer:

Stefano Rapisarda

Time Allocated for Final Tests:

One day

Verify VME access, perform counting test

Goal:

By doing basic VME read and write to the PCI_BS0 register, and by performing the counting test of the original driver, we verify that the Echotek supplied driver works and that the data path, including DMA transfers, is through, without any of our code involved.

VME Access Tests:

Do a read and write to the PCI_BS0 register on the console

Counting Test:

The Echotek driver will come with a few example board setup files and a demonstration program so that the user can perform a few stand-alone tests. With the current driver for the Recycler version, one of the 3 example setup files is “count.ch”, which configures the board to do the following:

- take a software trigger
- run in the “TRIGGER + BURST_COUNT” mode, where “BURST_COUNT” is set to 131072 so that the data fills the whole FIFO -- 512KB
- generate a fixed counting sequence
- bypass the ADC, DDC and resampler, directly store the data into the FIFO
- fire “Trigger Done (TDONE)” interrupt when “BURST_COUNT” is up
- use VME D32 DMA transfers

The processor then writes out the data to 8 output files – one for each channel, which should contain the same sequential countings. Any discontinuity in the final countings would indicate problem in the digital data path including the FIFO and the VME transfer. Here, the clock runs at 80 MHz.

Pass Criteria:

- VME read and write successful
- no discontinuity in the counting sequences, i.e. running “CountCheck” on the output files produces no printouts (complaints) on the screen.

Required Hardware:

The BPM test stand in FCC3 including the following:

- DAWN VME-64 crate
- MVME 2400 processor with ECSG-1R3ADC-PMC clock generator
- Tektronix TM5000A, with SG503 plug-in, sine wave generator
- HP 54542A oscilloscope

Required Software:

The Echotek driver, a few small C program “CountCheck.c”, see cvs module “echotek_tbpm”.

Performer:

Dehong Zhang, under supervision of Bob Webber and Vince Pavlicek

Time Allocated for Final Tests:

One day

Verify the new multi-board driver works

Goal:

Understand the modifications Echotek introduces in their driver to reflect the hardware changes, incorporate the necessary code into Duane/Charlie’s existing multi-board driver for the Recycler boards, perform the checks and demo tests included in the multi-board driver and verify the new multi-board driver supports normal operations.

Tests:

- run `ecdr814gcCopySetupBrd "board_no" "setup_index"`
This loads the specified board with the specified setup (image of the .ch file). 4 setup files are available:
 1. "rawDmaD64.ch" for raw data tests with D64 transfers
 2. "xlstest.ch" and "wsxlstest.ch" for complete tests of the ADC and DDC with D32 transfers
 3. "2.5MHz_cbcар_pbcар.ch" for some Recycler specific test
- run `ecdr814gcIoctlShowBrd "board_no" "verbose_level"`
This reads out the board setup over VME and dumps the information to the console for visual verification.
- run `start_loop "board_no" "setup_index"` and run `end_loop`
This reads the 4 setup files into the processors memory, then loads the specified board with the specified setup – given the index for "rawDmaD64.ch", runs in an end-less loop to read the board and write the data to an output file until the "end_loop" command is issued. The external trigger should run at a low rate.
- run `start_loopall "setup_index"` and run `end_loopall`
This test is identical to the above single board test, except it uses multiple boards. The minimum number is 2 boards. If more boards are available, they will be included.

Pass Criteria:

- The "ecdr814gcIoctlShowBrd" outputs consistent with the specified setups
- The data in the output files should show sine waves of the same frequencies as the input signals (3 MHz) when analyzed with "Raw_Test.vi"

Required Hardware:

The BPM test stand in FCC3 including the following:

- DAWN VME-64 crate
- MVME 2400 processor with ECSG-1R3ADC-PMC clock generator
- Tektronix TM5000A, with SG503 plug-in, sine wave generator
- HP 54542A oscilloscope

Required Software:

New driver from Echotek, the existing multi-board driver for the Recycler boards and the new multi-board driver for the Tevatron boards

Developer and Performer:

Dehong Zhang, under supervision of Bob Webber and Vince Pavlicek
(may need help from Charlie Briegel, Dinker Charak and Margaret Votava)

Time Allocated for Final Tests:

5 days

Perform the PREP quality control tests

Goal:

To run PREP quality control tests successfully on the new hardware, with new multi-board driver and repetitive hardware triggers. These tests will likely remain as the production board acceptance tests.

Tests:

- A full scale (1 Vp-p) sine wave of 3 MHz to test the ADC
In this test, raw ADC output is collected with D64 DMA transfers, bypassing the DDC and resampler. The “BURST_COUNT” is set to collect 512 samples after each external trigger.
- A filter test to check the DDC
In this test, the DDC runs in split-IQ mode and down-converts the ADC output to DC with a total decimation of 16, while the resampler is bypassed. The “BURST_COUNT” is set to collect 64 I&Q pairs after each external trigger. D32 DMA transfers are used.

In these 2 tests, a good quality, full scale (1 Vp-p) sine wave of 3 MHz is used as input. The clock runs at 80 MHz, while the external trigger runs at 50 Hz.

Pass Criteria:

- No gaps in the “Histogram” window, no spikes go beyond the +/- 0.7 red lines in the “Differential Nonlinearity” window after more than 1000000 samples.
- The “Magnitude” of the I&Q pairs should fall between 16920 and 19080 – the “Flattop” LED should be green.

Required Hardware:

The BPM test stand in FCC3 including the following:

- DAWN VME-64 crate
- MVME 2400 processor with ECSG-1R3ADC-PMC clock generator
- Accelerator controls fiber optic repeater
- Accelerator controls clocks box
- Tektronix TM5000A, with SG503 plug-in, sine wave generator
- HP 8110A pulse generator
- HP 54542A oscilloscope

Required Software:

- New multi-board driver
- “tstbpm” package and the corresponding LabView host program from Duane Voy

Performer:

Dehong Zhang

Time Allocated for Final Tests:

3 days

Verify that the FPGA flash can be reprogrammed

Goal:

Check to see whether we can load the FPGA flash through VME or JTAG

Tests:

Get familiar with the original/default firmware, modify it such that, for example, the counting sequence is altered in a known way; then re-load the original, the counting sequence should restore the original order.

Pass Criterion:

The final output shows the counting sequence in the modified way; restored when the original firmware is re-loaded.

Required Hardware:

The BPM test stand in FCC3

Required Software:

- Original FPGA firmware source code, board schematics file
- Original driver

Performer:

Mark Bowden with some assistance from Dehong Zhang

Time Allocated for Final Tests:

2 days

Tevatron BPM ADC Board Testing, Version 11

Concurrence

Following persons reviewed and concurred with the content of this document.

Steve Wolbers 10/13/04
Steve Wolbers, Project Manager (date)

Bob Webber 10/13/04
Bob Webber, Deputy Project Manager (date)

Jim Steimel 10/13/04
Jim Steimel, Technical Coordinator (date)

Vince Pavlicek 13 Oct 04
Vince Pavlicek, Subsystem manager (date)

Margaret Votava 10/13/04
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