Integrator / Digitizer Test Card

Purpose of the Test Card

- Evaluate the performance of the proposed integration, digitization and data processing methods.
- Evaluate the integrator, digitizer and other components and circuits in a realistic context.
- Discover sources of noise and EMI both on and off the circuit card.
- Experiment with techniques to improve the signal to noise ratio of the readout.

More →

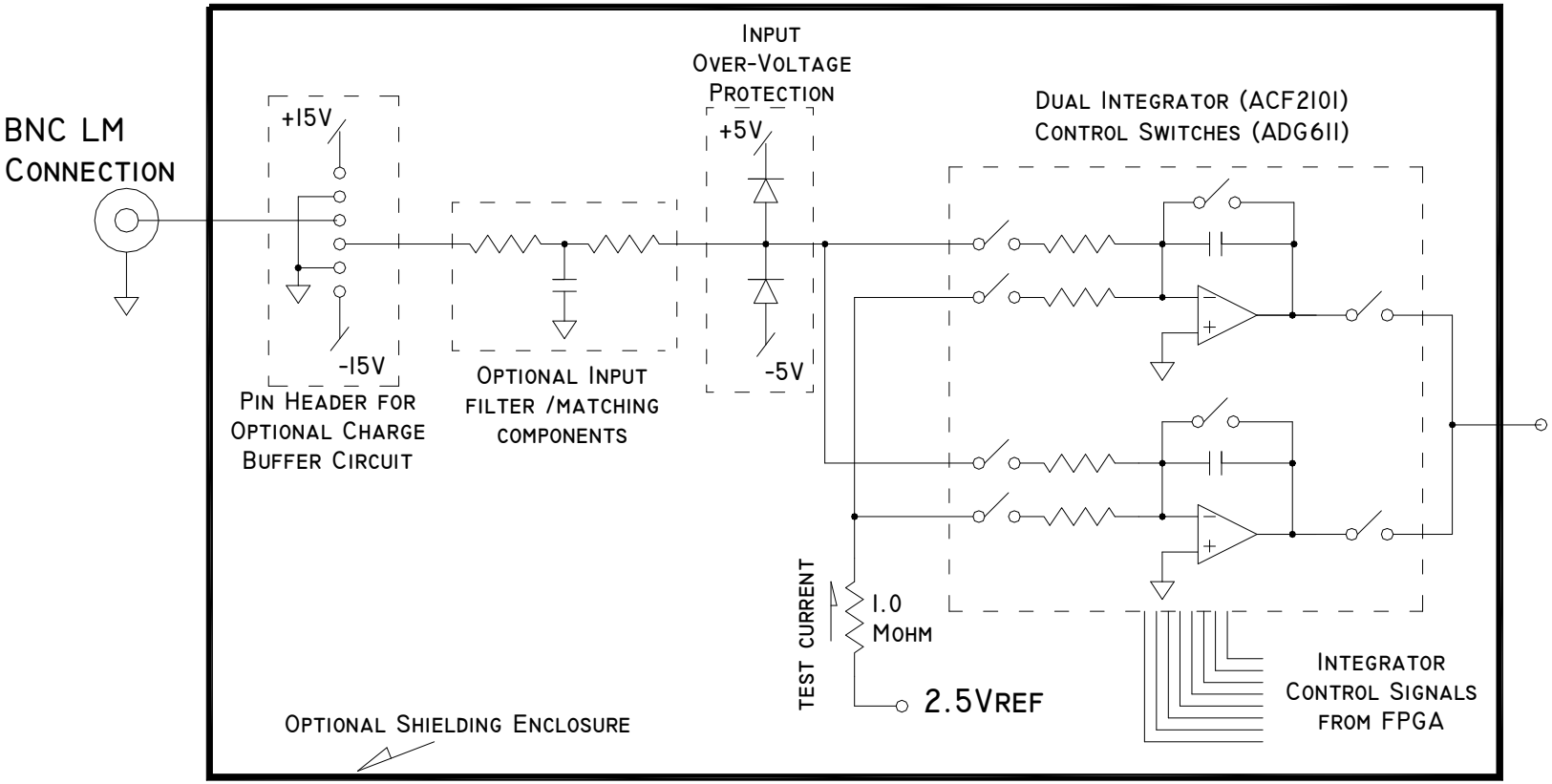
Integrator / Digitizer Test Card

Purpose of the Test Card

- Explore the impact of cabling on our measurement.
- Measure the actual power requirements.
- Work through the procurement, assembly and other mechanical details of the card.
- Determine which features are unnecessary and which may need to be improved or added.

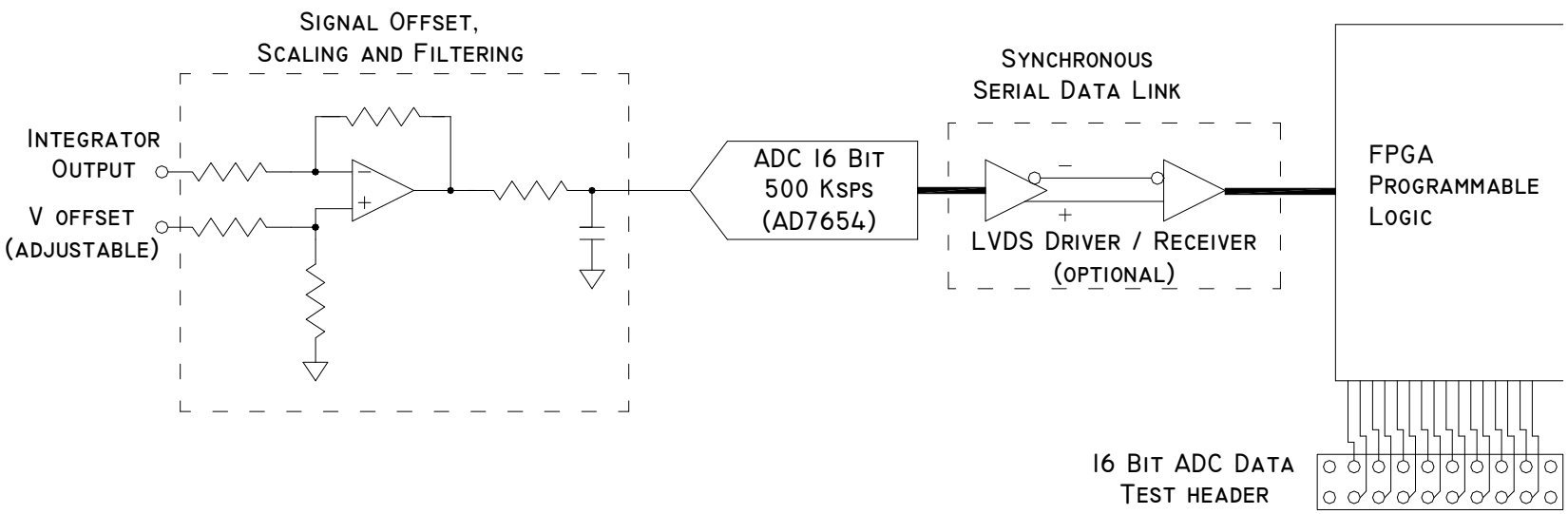
Integrator / Digitizer Test Card

Integrator Input Section



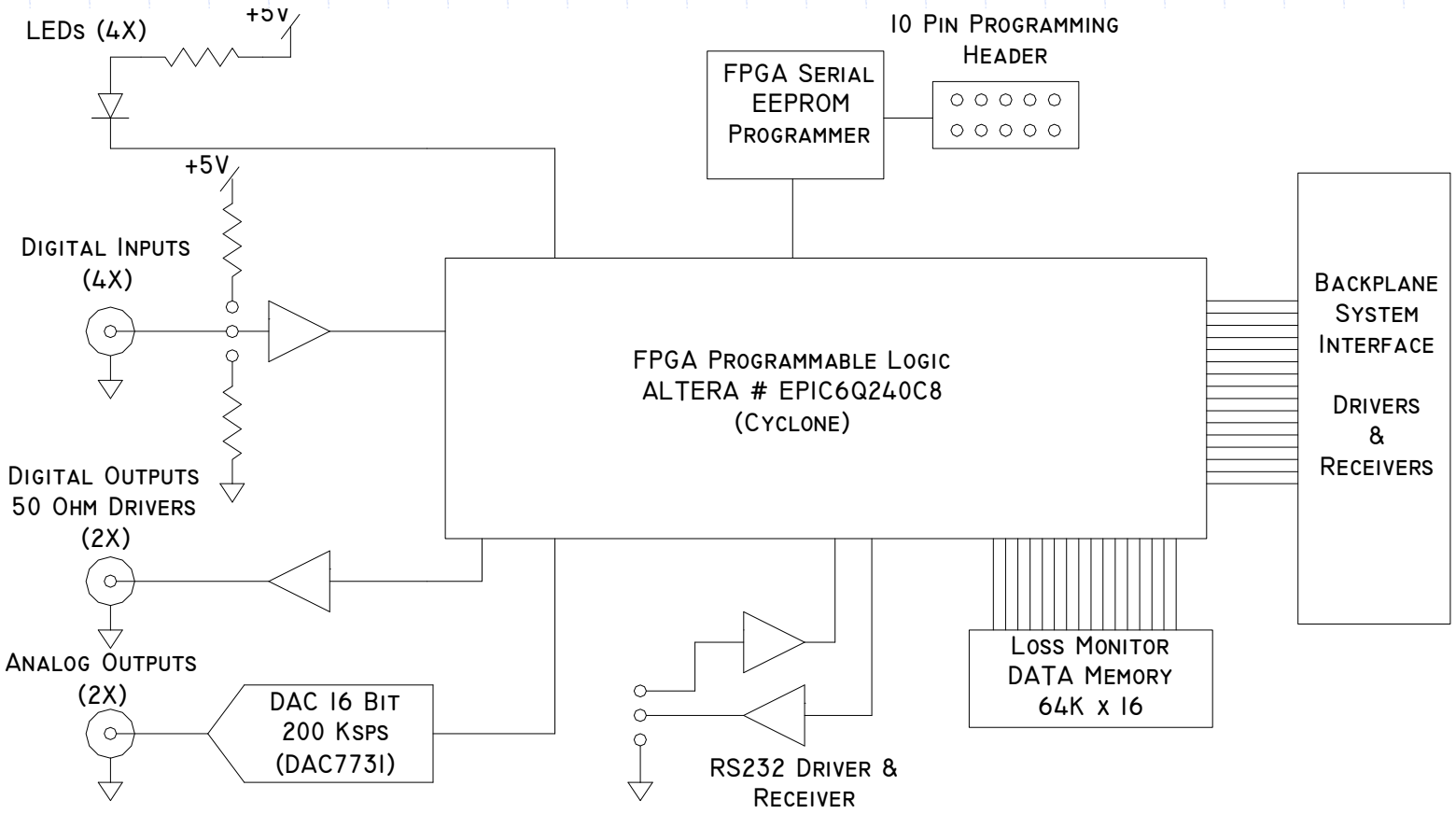
Integrator / Digitizer Test Card

Digitizer Section



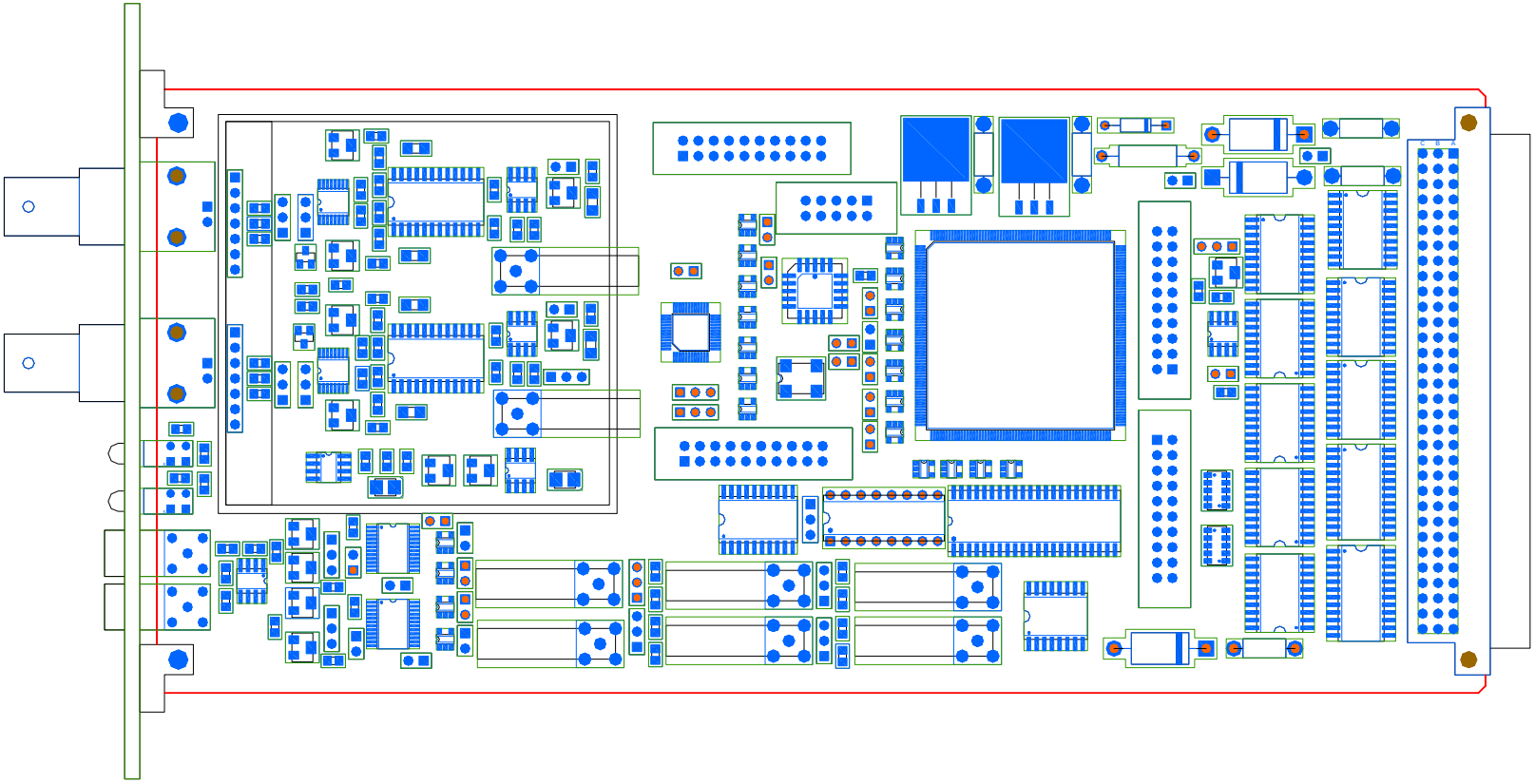
Integrator / Digitizer Test Card

Digital Section



Integrator / Digitizer Test Card

PCB Layout



Integrator / Digitizer Test Card

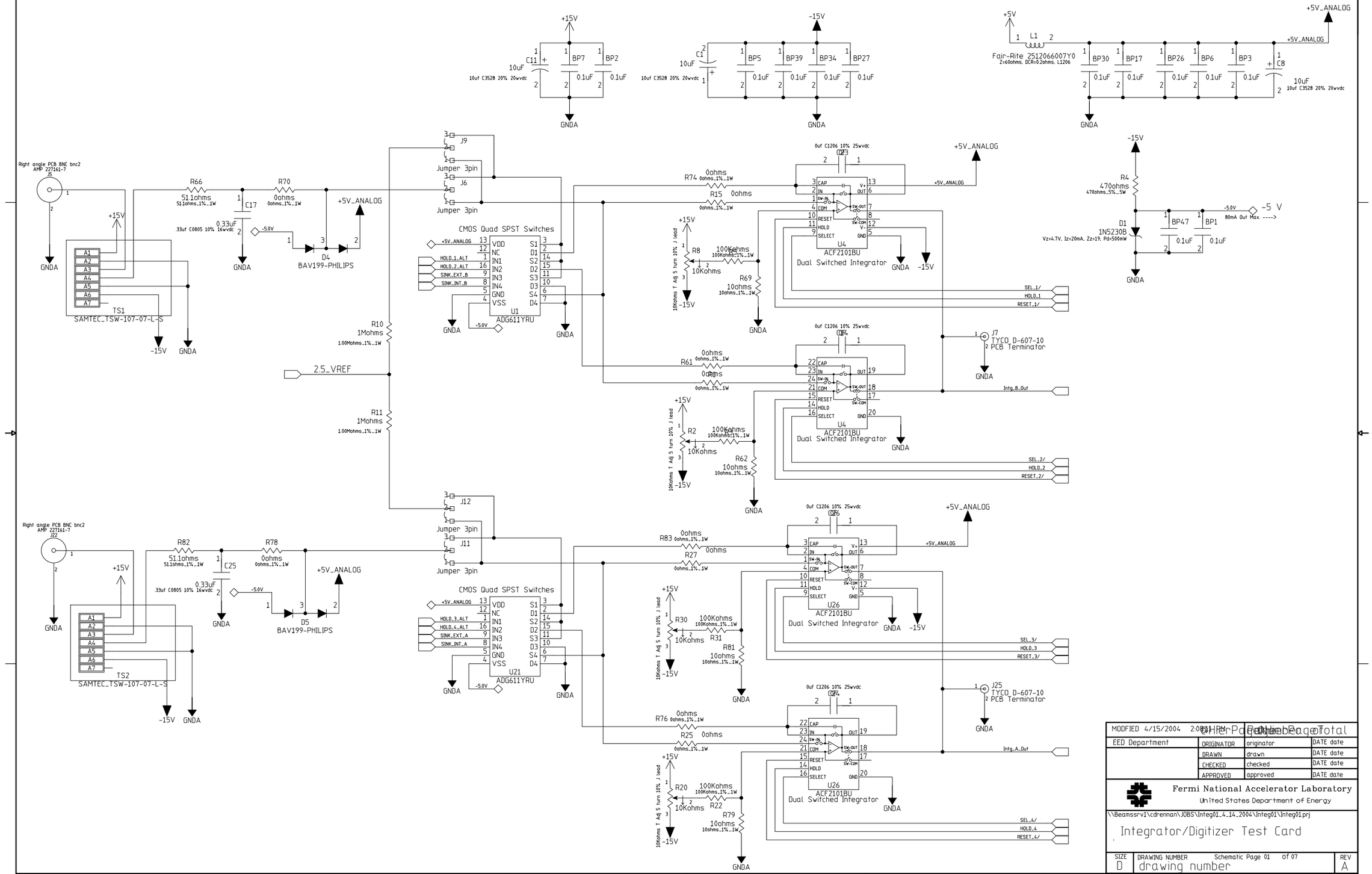
Candidate Test Signal Sources

- Precision DC voltage source in series with a large value resistor.
- Pulse or other arbitrary signals generated by on card FPGA and DAC in series with a large value resistor.
- Precision charge currents produced using a Keithley 236 Source Measurement Unit.
- Actual charge currents from Loss Monitors in the Tevatron or Booster.

Integrator / Digitizer Test Card

Acquiring and Evaluating Test Data

- The PPD ASIC Test Stand will connect to the 16 Bit ADC Data Test Header, and process and display results using Visual Basic routines.
- Tests in the field could use the RS-232 serial port implemented in the FPGA.
- Later test will use the proposed backplane interface to collect data.


+15V
-15V
+5V
+5V_ANALOG
GNDA
C11 10uF
10uf C3528 20% 20wvdc
BP7
BP2
0.1uF
C1 10uF
BP5
BP39
BP34
BP27
L1
Fair-Rite 2512066007Y0
Z=60ohms, DCR=0.2ohms, L1206
BP30
BP17
BP26
BP6
BP3
C8 10uF
Right angle PCB BNC bnc2
AMP 227161-7
J2
R66 511ohms
R70 0ohms
C17 0.33uF
33uf C0805 10% 16wvdc
-5.0V
D4 BAV199-PHILIPS
TS1
SAMTEC_TSW-107-07-L-S
A1
A2
A3
A4
A5
A6
A7
J9
Jumper 3pin
J6
CMOS Quad SPST Switches
U1
ADG611YRU
VDD
NC
IN1
IN2
IN3
IN4
GND
VSS
S1
D1
S2
D2
S3
D3
S4
D4
HOLD_1_ALT
HOLD_2_ALT
SINK_EXT_B
SINK_INT_B
R10 1Mohms
R11 1Mohms
2.5_VREF
R74 0ohms
R15 0ohms
C3 0uf C1206 10% 25wvdc
U4
ACF2101BU
Dual Switched Integrator
CAP
IN
SW-IN
COM
RESET
HOLD
SELECT
V+
OUT
SW-OUT
SW-COM
V-
R8 10Kohms
10Kohms T Adj 5 turn 10% J lead
R69 10ohms
SEL_1/
HOLD_1
RESET_1/
R4 470ohms
D1 1N5230B
Vz=4.7V, Iz=20mA, Zz=19, Pd=500mW
BP47
BP1
-5 V
80mA Out Max. ---->
J7
TYCO D-607-10
2 PCB Terminator
R61 0ohms
C4 0uf C1206 10% 25wvdc
R2 10Kohms
R62 10ohms
Intg_B_Out
SEL_2/
HOLD_2
RESET_2/
Right angle PCB BNC bnc2
AMP 227161-7
J22
R82 51.1ohms
R78 0ohms
C25 0.33uF
33uf C0805 10% 16wvdc
D5 BAV199-PHILIPS
TS2
SAMTEC_TSW-107-07-L-S
J12
J11
CMOS Quad SPST Switches
U21
ADG611YRU
HOLD_3_ALT
HOLD_4_ALT
SINK_EXT_A
SINK_INT_A
R83 0ohms
R27 0ohms
C6 0uf C1206 10% 25wvdc
U26
ACF2101BU
Dual Switched Integrator
R30 10Kohms
R31 100Kohms
R81 10ohms
SEL_3/
HOLD_3
RESET_3/
J25
TYCO D-607-10
2 PCB Terminator
R76 0ohms
R25 0ohms
C7 0uf C1206 10% 25wvdc
R20 10Kohms
R22 100Kohms
R79 10ohms
Intg_A_Out
SEL_4/
HOLD_4
RESET_4/
MODIFIED 4/15/2004 2:08:11 PM
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
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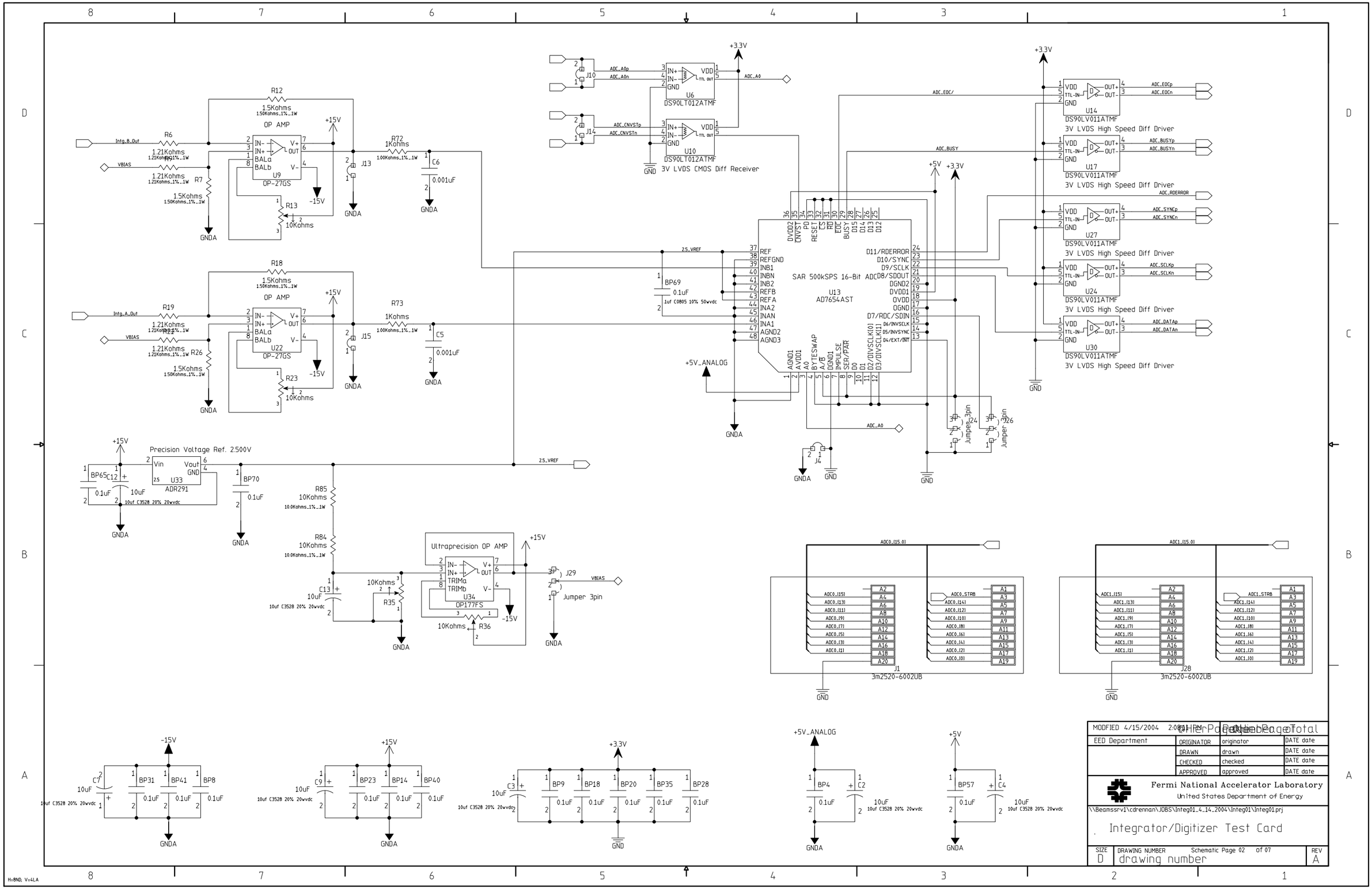
Integrator/Digitizer Test Card
SIZE D
DRAWING NUMBER drawing number
Schematic Page 01 of 07
REV A
H:8ND; V:4LA



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	DRAWN	drawn	DATE date
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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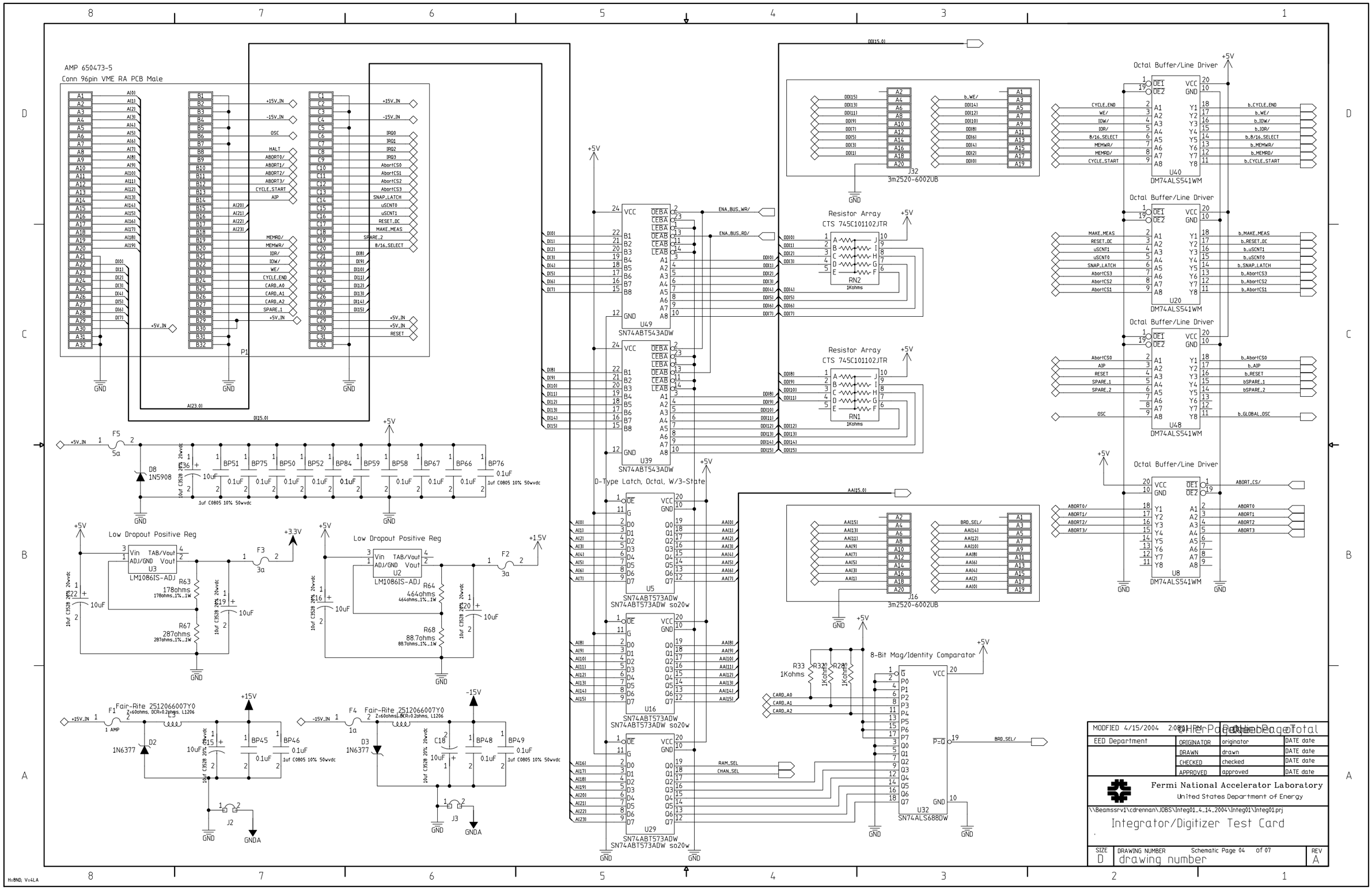
Integrator/Digitizer Test Card

SIZE	DRAWING NUMBER	Schematic Page 02 of 07	REV
D	drawing number		A

H=8ND; V=4LA


AMP 650473-5
Conn 96pin VME RA PCB Male
P1
Low Dropout Positive Reg
LM1086IS-ADJ
Fair-Rite 2512066007Y0
Resistor Array
CTS 745C101102JTR
RN2
RN1
1Kohms
J32
3m2520-6002UB
J16
3m2520-6002UB
Octal Buffer/Line Driver
DM74ALS541WM
U40
U20
U48
U8
U49
SN74ABT543ADW
U39
SN74ABT543ADW
D-Type Latch, Octal, W/3-State
U5
SN74ABT573ADW
SN74ABT573ADW so20w
U16
SN74ABT573ADW
SN74ABT573ADW so20w
U29
SN74ABT573ADW
SN74ABT573ADW so20w
8-Bit Mag/Identity Comparator
U32
SN74ALS688DW
MODIFIED 4/15/2004
EED Department
ORIGINATOR originator DATE date
DRAWN drawn DATE date
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
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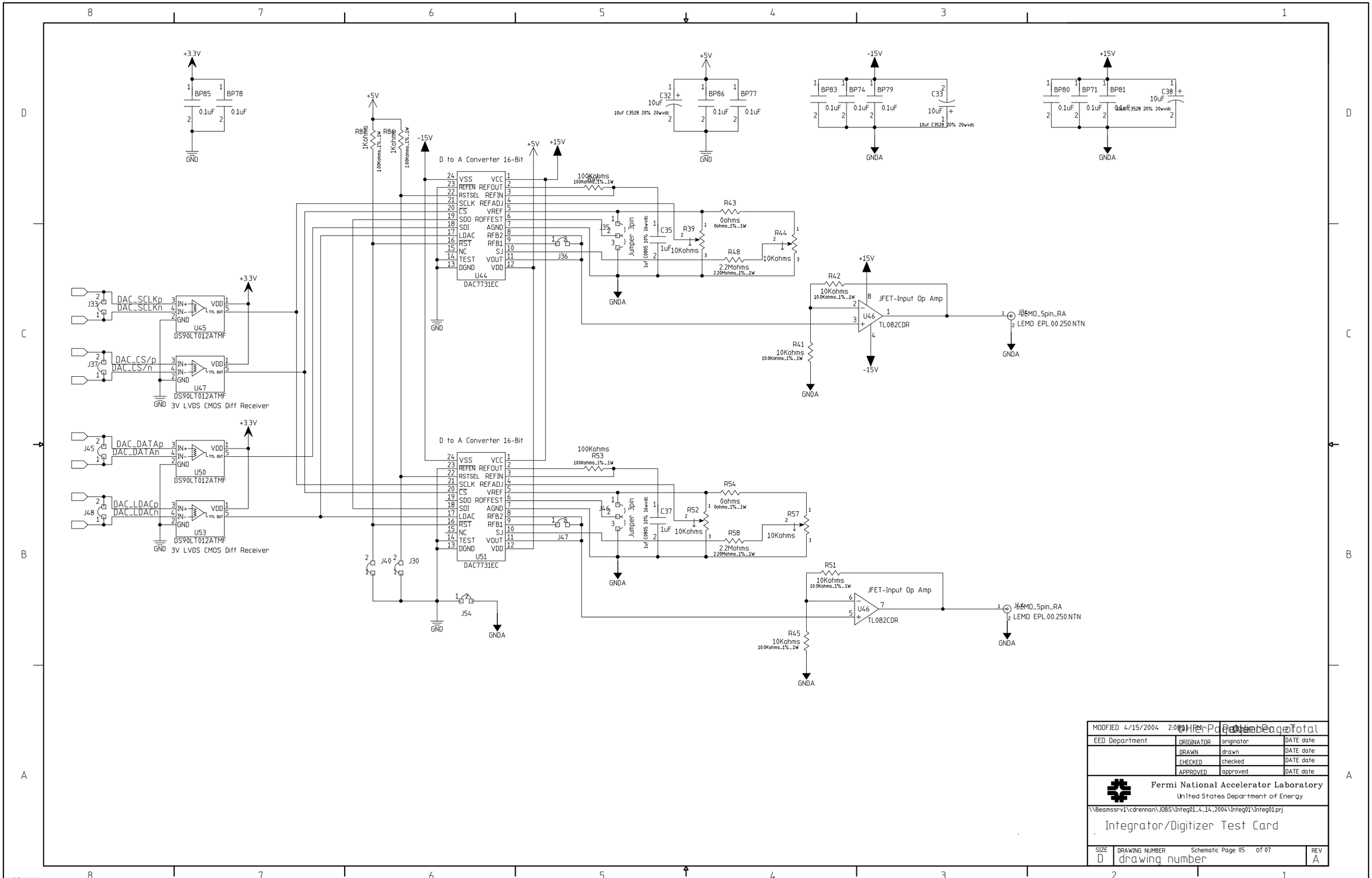
Integrator/Digitizer Test Card
SIZE D
DRAWING NUMBER Schematic Page 04 of 07
drawing number
REV A
H=8ND; V=4LA



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	APPROVED	approved	DATE date

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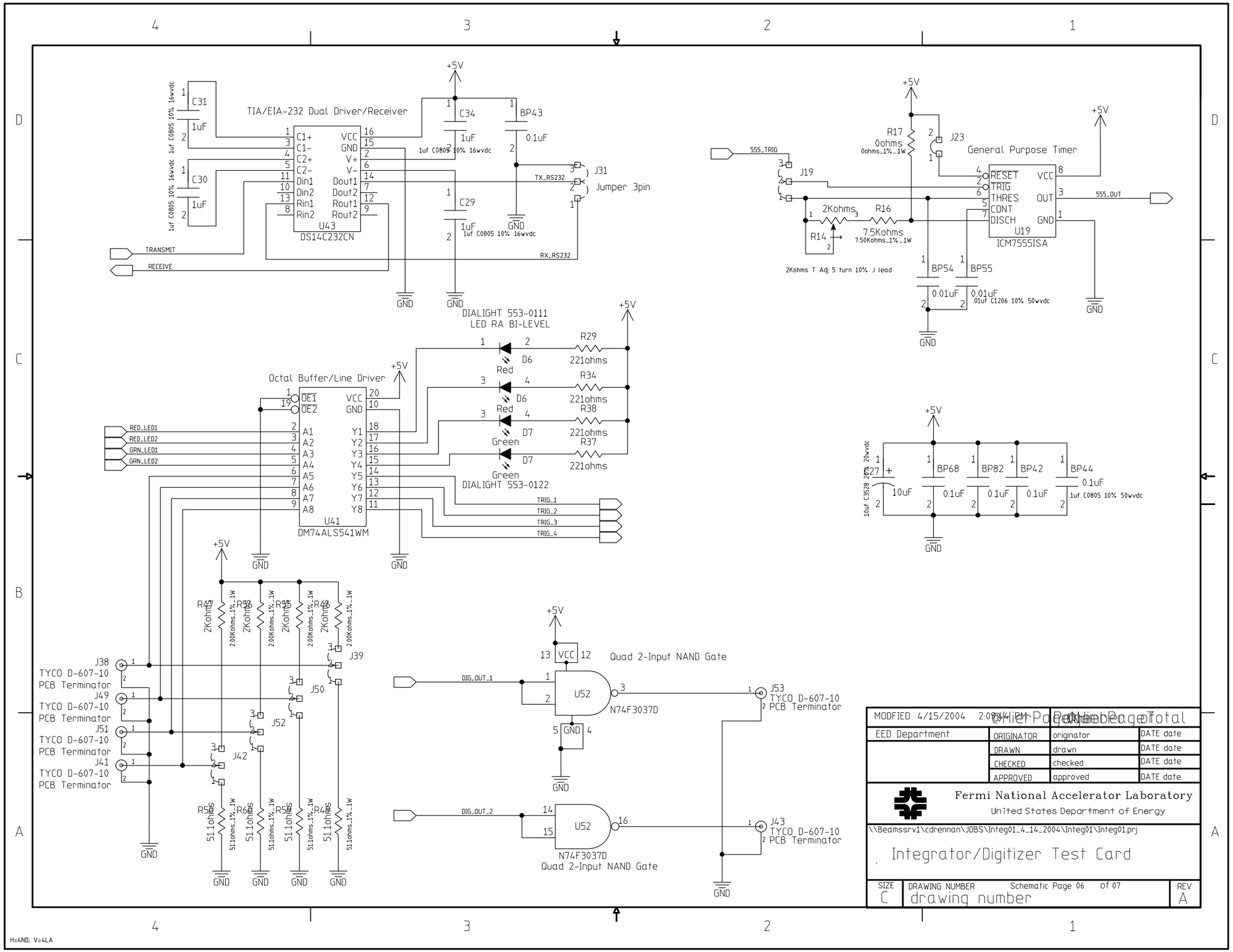
Integrator/Digitizer Test Card

SIZE	DRAWING NUMBER	Schematic Page 05 of 07	REV
D	drawing number		A

H=8ND; V=4LA


TIA/EIA-232 Dual Driver/Receiver
U43
DS14C232CN
C31
C30
C34
C29
BP43
J31
Jumper 3pin
TX_RS232
RX_RS232
TRANSMIT
RECEIVE
GND
+5V
DIALIGHT 553-0111
LED RA BI-LEVEL
D6
D7
Red
Green
R29
R34
R38
R37
221ohms
DIALIGHT 553-0122
Octal Buffer/Line Driver
U41
DM74ALS541WM
RED_LED1
RED_LED2
GRN_LED1
GRN_LED2
TRIG_1
TRIG_2
TRIG_3
TRIG_4
J38
J49
J51
J41
J39
J50
J52
J42
TYCO D-607-10
PCB Terminator
Quad 2-Input NAND Gate
U52
N74F3037D
DIG_OUT_1
DIG_OUT_2
J53
J43
555_TRIG
J19
R17
0ohms
J23
General Purpose Timer
U19
ICM7555ISA
RESET
TRIG
THRES
CONT
DISCH
VCC
OUT
GND
555_OUT
2Kohms
R16
7.5Kohms
R14
2Kohms T Adj 5 turn 10% J lead
BP54
BP55
0.01uF
BP68
BP82
BP42
BP44
0.1uF
10uF
MODFIED 4/15/2004
EED Department
ORIGINATOR
DRAWN
CHECKED
APPROVED
originator
drawn
checked
approved
DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
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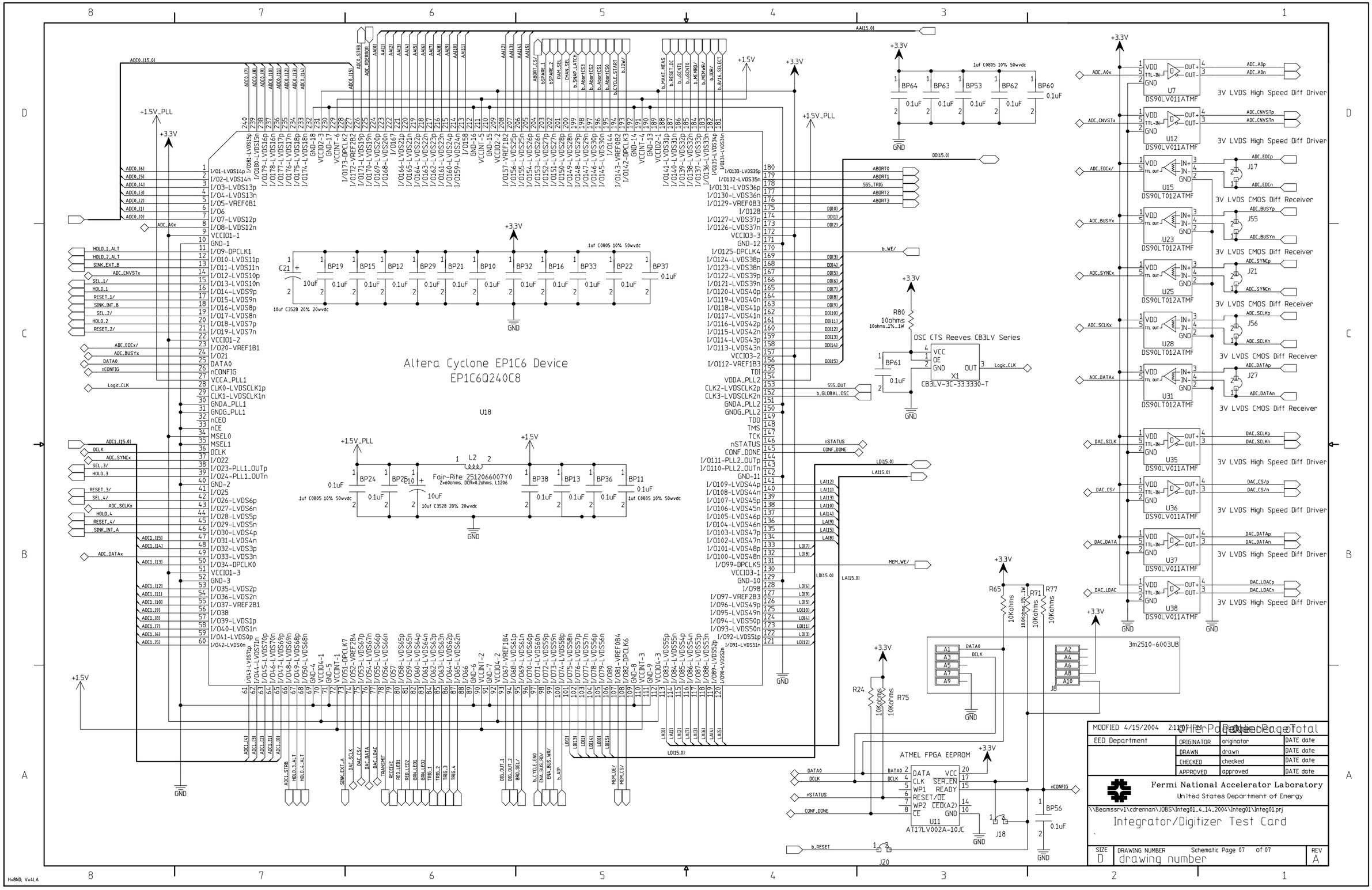
Integrator/Digitizer Test Card
SIZE
C
DRAWING NUMBER
drawing number
Schematic Page 06 of 07
REV
A
H=4ND; V=4LA


Altera Cyclone EP1C6 Device
EP1C6Q240C8
U18
Fair-Rite 2512066007Y0
Z=60ohms, DCR=0.2ohms, L1206
OSC CTS Reeves CB3LV Series
CB3LV-3C-33.3330-T
3V LVDS High Speed Diff Driver
3V LVDS CMOS Diff Receiver
DS90LV011ATMF
DS90LT012ATMF
DS90LV011ATMF
3m2510-6003UB
ATMEL FPGA EEPROM
AT17LV002A-10JC
MODIFIED 4/15/2004
EED Department
ORIGINATOR
DRAWN
CHECKED
APPROVED
DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
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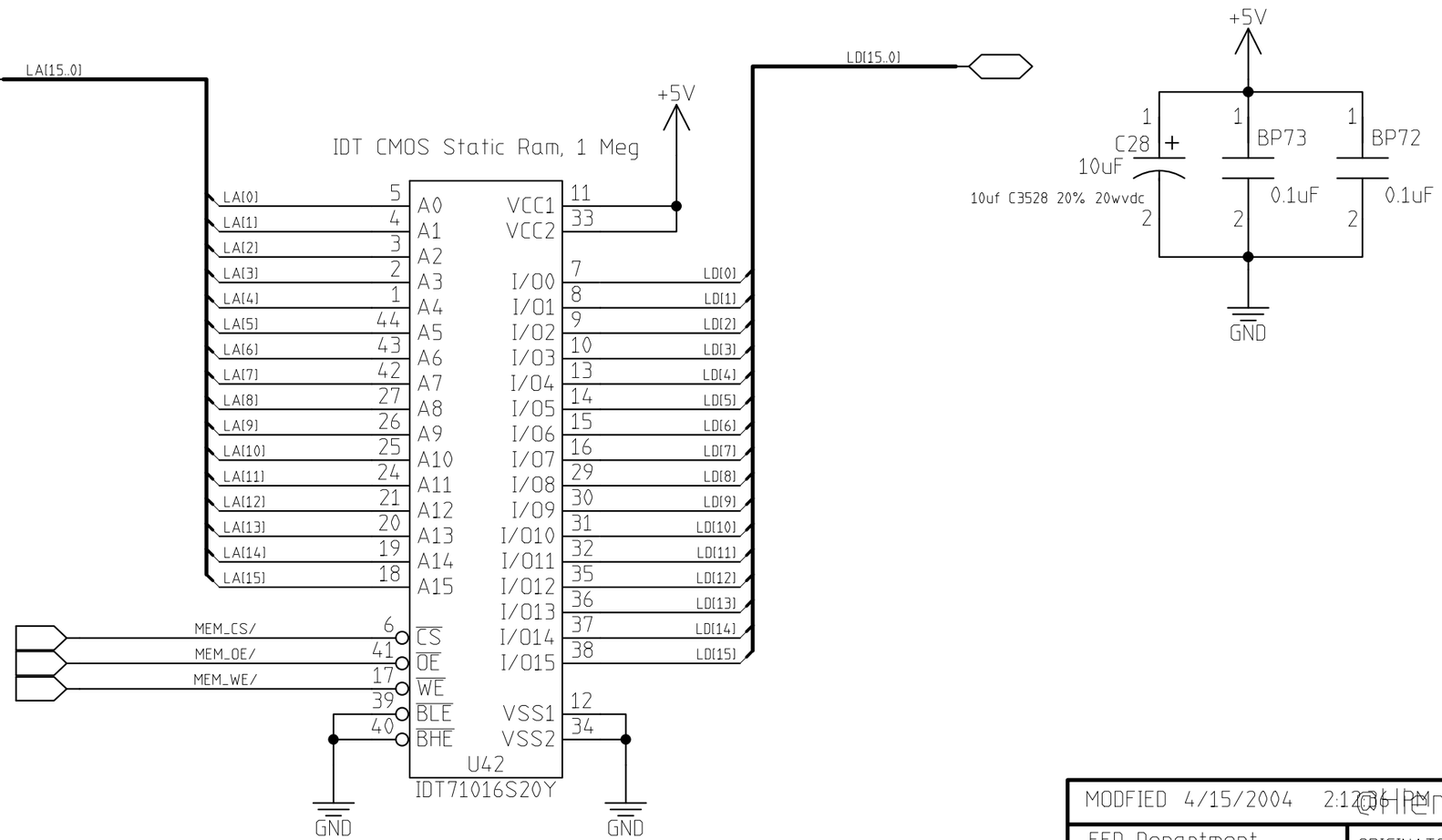
Integrator/Digitizer Test Card
SIZE
D
DRAWING NUMBER
Schematic Page 07 of 07
drawing number
REV
A
H=8ND; V=4LA



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Integrator/Digitizer Test Card

SIZE	DRAWING NUMBER	REV
B	drawing number	A

Schematic Page 08 of 07

H=2LA; V=2LA