Operating Modes

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ADC CLOCK RATE ~ 65 MHz

- Bunch by Bunch Measurement

  2.53 MHz

  decimation = x25

- Turn by Turn Measurement

  47.6 KHz

  decimation = x1365

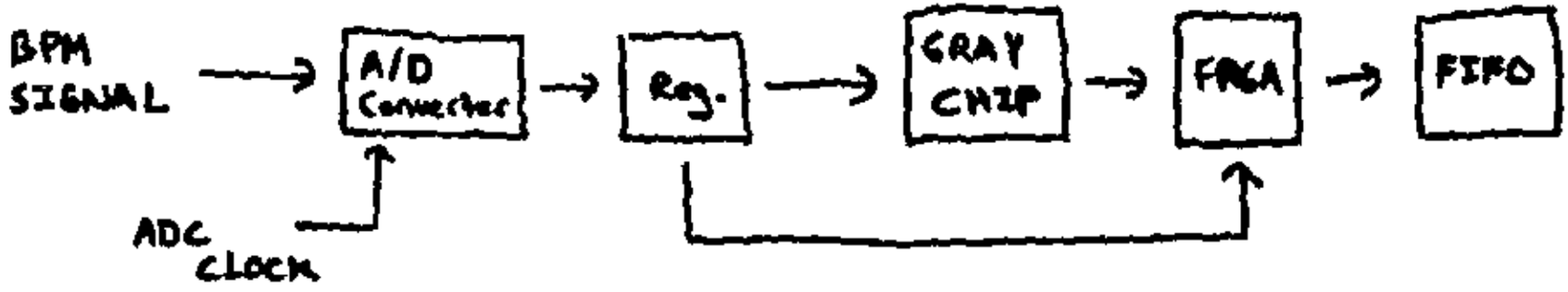
- Closed orbit Measurement

  100 Hz

  decimation = x650000

- $\bar{p}$ measurement ≡ Bunch by Bunch (gated)

Echotek :



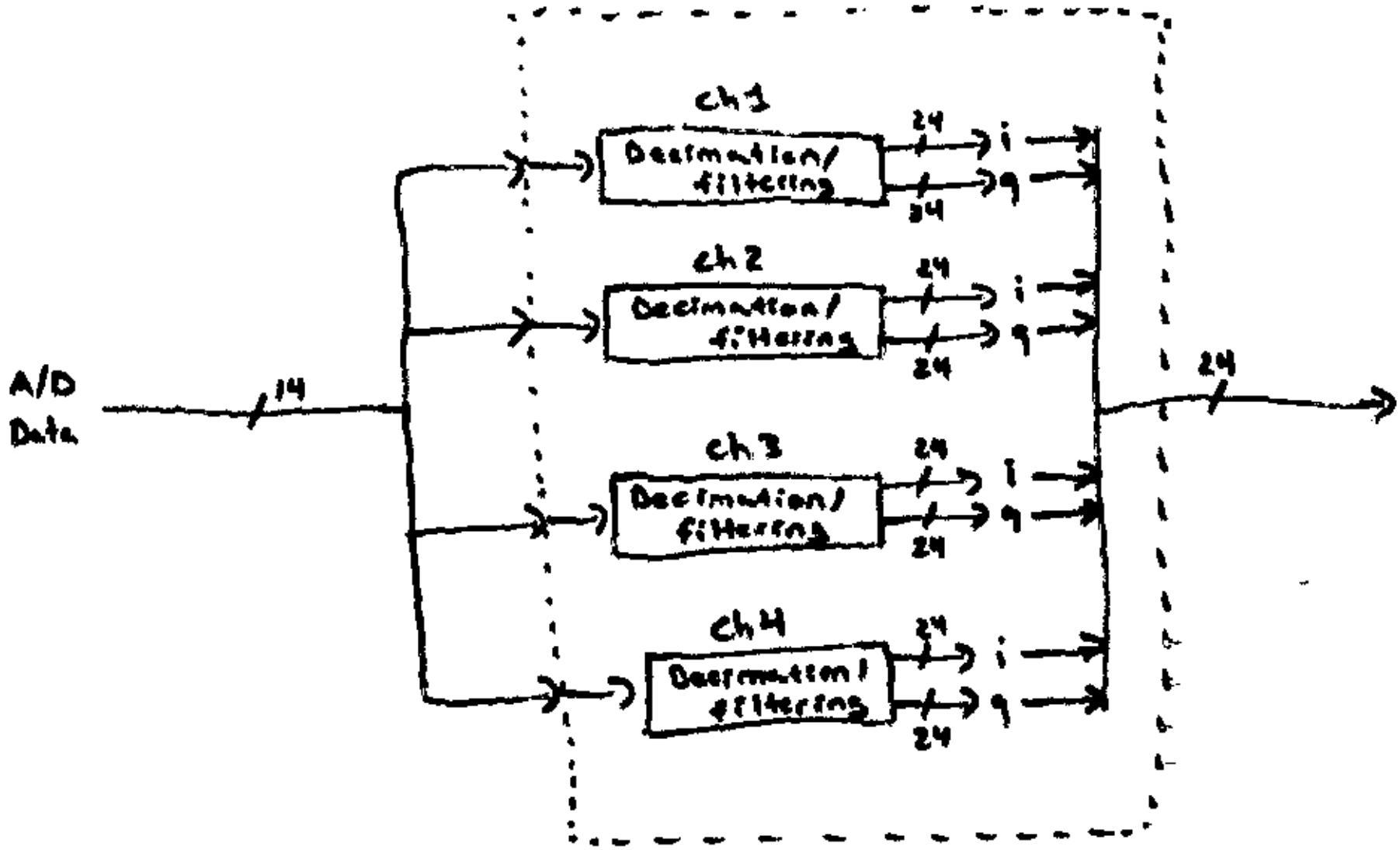
- eight channels
- 1 gray chip /channel
- pre-programmed FPGA has four modes
  - (1) pass raw A/D data
  - (2) average n A/D data points
  - (3) pass raw Gray Chip data
  - (4) average n Gray Chip data points

$n = 1, 2, 4, 8, 16, 32, 64, 128,$ or 256

more on GRAY chip :

- Output of each channel (4 total) is 16 or 24 bits of i and q data.
- Each channel can have unique decimation and filtering.
- Not clear in documentation how eight individual measurements are transfered over parallel output bus in assumed output mode.
- This would presumably be even more complicated if different output rates from each channel.
- Gustavo notes that minimum decimation for single channel is x32 → bunch by bunch measurements require use of two channels (multi-channel mode) to reduce decimation by additional factor of two.

GRAY chip (Input/output):



note: best guesses for input/output formats
(need to confirm)

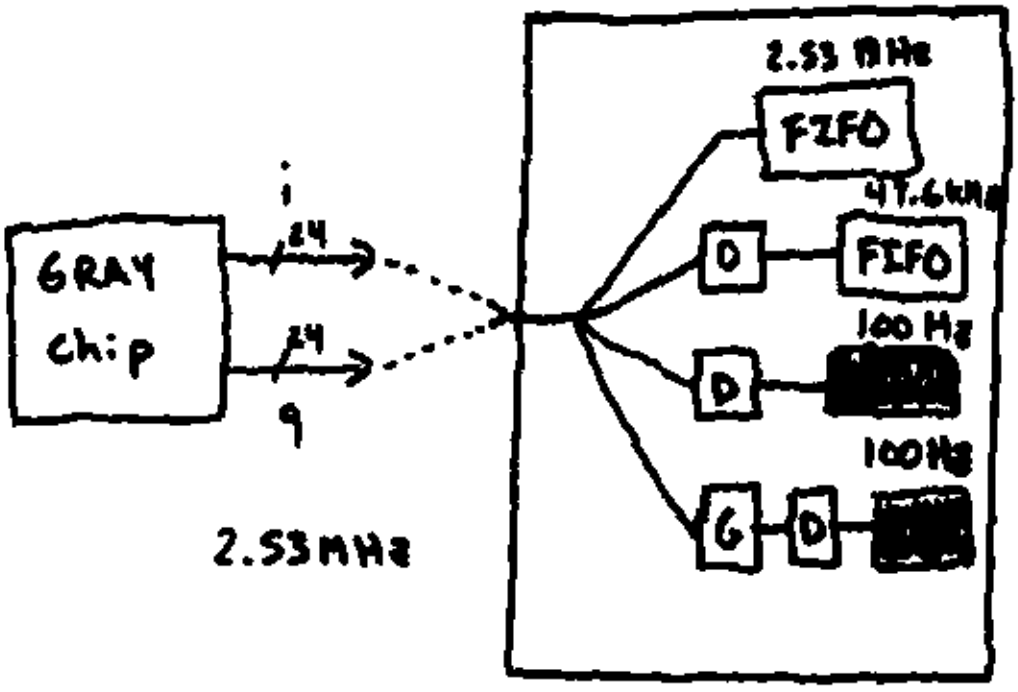
Two paths to explore:

(1) Use two GRAY chip channels to perform bunch by bunch measurement.

Output i, q GRAY chip output to FPGA at 2.5 MHz

FPGA performs additional decimation and filtering for Turn by Turn and closed orbit measurements.

FPGA also provides for gating necessary for $\bar{p}$ only measurement. Is there an available input?



(2) Use two GRAY chip channels for bunch by bunch, a third for turn by turn, and fourth for closed orbit.

$\bar{p}$ gating would still need to be done at FP6A (don't see an easy way to do this on GRAY chip).

Would require understanding how to output data from 3 channels with different rates over parallel output bus.

For now,

- Start by implementing three individual modes on GRAY chip (minimal FPGA processing).

- For closed orbit, maximum GRAY chip decimation is x 16,384 so either take advantage of x32 averaging on FPGA or write at faster rate to memory than readout rate (~100 Hz).

- For bunch by bunch and turn by turn, no FPGA functionality needed (pass-through). Bunch by Bunch will require two channel GRAY chip mode operation.

- Big question is where to get beam signals (TeV Marker for $\bar{p}$ measurement and Abort for halting FIFO at beam event). FPGA seems like the logical place, but are signals available?