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Tevatron Beam Position Monitor (BPM) Upgrade

Timing Generator Fanout Module Test Report

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Introduction

This document contains the results of the testing of the Timing Generator Fanout (TGF) module in satisfaction of the requirements needed to release the design to production. The TGF module must provide all of the functionality of the current Timing Signal Generator module in the Accelerator Division Recycler Ring BPM system (RR BPM). The functions are:

1) Accept and phase lock to the accelerator RF clock[1] and generate a clean clock multiplied up by 7/5ths the input frequency and then fan-out and buffer that clock to eight transformer coupled outputs compatible with the Echotek clock inputs..
2) Generate eight separate Sync outputs that can be programmed to be started and/or triggered by TVBSync events. The Sync outputs must be able to be delayed a programmable number of beam turn markers (pretrigger) and, independently, a programmable number of RF clocks after the start or pretrigger event. Once started, a programmable number of syncs must be generated. Programmable values must be accessible as read/write registers by the sub rack processor through the VME bus at addresses that match the Recycler system addresses.
3) A TVBS decoder must accept the distributed TVBS signal, lock to it and decode it searching for either of two programmable events. The two outputs from decoder should be able to trigger and delay the Sync generator as described above. In addition the decoder must be able to interrupt the sub rack processor.
4) A TCLK decoder must accept the distributed TCLK signal, lock to it and decode it searching for either of eight programmable events. The outputs from the event comparator should be able to interrupt the sub rack processor and the processor

[1] AKA 53 Mhz clock, Main ring clock, Tevatron Clock …

should be able to determine which event was decoded by setting the interrupt vectors for the eight events.

5) Additional interrupts. The interrupt circuitry must be able to generate processor interrupts from other events such as 1) state changes within the Sync generator, such as the Turn Counter count-down, and 2) from internal periodic counters for repetitive diagnostics and calibration. The list of events is in the Hardware document Beams #1065 in the IRQ SOURCE MUX table.

Test results

1) The RF clock circuits were assembled and tested first. The jitter of the 74.35 MHz output clocks was compared to and found to be much less than the 53.104 MHz input clock from the MCR. Large sample measurements of the output clock shows less than 4 picoseconds RMS of jitter which is as good as similar measurements of the commercial Echotek clock generator used in the RR BPM system. Spectrum plots showed good signal purity and the sidebands within 50 MHz were all more than 70 db below the clock level. All eight channels display similar jitter measurements and spectral purity plots. Example data is attached.
2) The Sync generator was tested using the data acquisition software and satisfactorily operated within that environment collecting data that was equivalent to the Recycler hardware. Some modifications were made to the software to accommodate the mix of hardware needed because of the absence of a TCLK decoder in the TGF firmware. Two output channels were checked completely with the Data Acquisition software collecting data from Echotek modules and filter cards. Sync delays were adjusted to confirm that function. The DA software will need to be modified to accommodate the finer granularity of the delay adjustments in the TGF firmware. Oscilloscope testing confirmed that all eight channels operate the same.
3) TVBSync decoder firmware has been tested with the data acquisition software and Beam Sync revolution marker events ($AA) and Main Injector Transfer events ($D8) from the MCR were decoded. Revolution marker events were programmed to interrupt the sub rack processor as part of the data acquisition software testing.
4) The TCLK decoder is an identical firmware design to the TVBS decoder. The only difference is that it operates at 10 MHz rather than 7.5 MHZ so there is a single counter set to divide by a different index. This specific firmware has been simulated but not operationally tested but the basic design was tested in part 3. The on-the-board connectivity to inputs and outputs for this section has been tested separately. This small task of firmware debugging should not hold up hardware production. The current operational FPGA firmware is using approximately 10% of the chip resources. The duplication of the interrupt logic that is behind the BSync decoder in order to have interrupt logic behind the TClk decoder will not double the resource usage. Even if it did only 20% of the resources of the FPGA would be used.
5) Interrupt and programmable vectoring capability has been demonstrated as part of the data acquisition software testing.
6) Not specifically mentioned above: Front Panel diagnostic outputs that are programmable within the FPGA have been used as part of the board and firmware diagnostics. Various signals have been provided to the operators at various times as needed to assist with the testing. These use extra front panel connectors. The front panel LEDs were tested individually and half of the programmable

functionality has been implemented and demonstrated. Additional LED functions can be added as needed. In the interest of full disclosure, there is a Digital to Analog converter on the board that has not been tested. It was envisioned as an additional diagnostic capability but has never been part of the requirements.

Conclusion

The connectivity requirements for inputs, outputs and within the board have been demonstrated. All VME operations including interrupts and programmable vectoring were tested. All of the Sync output functionality has been demonstrated in the test stand. One of two almost identical event decoders has been completely tested including the capability to interrupt the sub rack controller. Some firmware debugging still needs to be completed on the second decoder function but it consists of a replicated section of operational firmware and as such, is considered to be a straightforward task. This should not hold up the hardware production of this board.

Change Log

Version	Issue Date	Description of Change
1.0	17 Sept 2004	Original FVP
2.0	17 Sept 2004	Small modifications suggested by reviewers

Concurrence

Following persons reviewed and concurred with the content of this document.

Steve Wolbers, Project Manager (date) 9/22/04

Bob Webber, Deputy Project Manager (date) 9/22/04

Jim Steimel, Technical Coordinator (date) 9-22-04

Vince Pavlicek, Subsystem manager (date) 22 Sept 04

Margaret Votava, Subsystem manager (date) 9-22-04

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