Collider Run II Shot Setup Documentation

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Send suggestions and comments to ad-pbar-tuning-adminNOSPAM@fnal.gov (remove "NOSPAM").

Sequencer: Pbar

Collider Aggregate: Run II Start Reverse Protons

Previous Aggregate: Run II Start Shot Setup

Purpose of this Aggregate: The previous aggregate prepared the AP1 and AP3 beam lines for 8 Gev operation.   This aggregate enables 8 GeV beam for the Main Injector portion of the tune-up, and configures Accumulator cooling.   To prepare for 8 GeV beam, this aggregate toggles the P67 abort masks from 120 GeV to 8 GeV operation, sets the $16/$2D 8 GeV tune-up event to 2 turns/35 bunches, sets V:PSHOOT to 4 to allow the Main Injector to start 8 GeV tune-up on $2D, and clears the Pbar software beam switch.   This aggregate also has the Pbar Sequencer operator wait for the stacktail to pull the beam over into the core. When this is done, the stacktail is turned off, power leveling is setup on the core transverse and longitudinal systems and we switch over to the 4-8GHz core momentum system.   The VSA program should still be running on SC, and the Pbar Sequencer operator should still be trying to cool the Accumulator frequency width A:FRWDTH to 15Hz.

How to get back to stacking from here: Run the Run II Return to Stacking Aggregate.

::: INSTRUCT 210   .

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   This aggregate steps one through tuning up the Main Injector, P1,
P2, AP1, and AP3 lines as well as injection into the Accumulator
with reverse protons. Completing this tune up gives high assurance
that the Pbar transfer efficiency from the Accumulator to the MI
willl be maximized.

          Interrupt anywhere in this box to continue.
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::: SHOT_LOG COMMENT   .
   Enters the following comment into the Pbar portion of the shot scrapbook at http://www-bd.fnal.gov/cgi-mach/machlog.pl?nb=scrap03.
   🟢Time- Beginning Reverse Proton Tune Up in Pbar and MI. The Stack size is ###.#####. - Sequencer

::: INSTRUCT 213   D
   Proton Torpedo SA instruct is bypassed.

::: START_PGM P194   D
   Starts Proton Torpedo SA (keeper is Budlong). Command is bypassed.

::: CTLIT_DEVICE D:BSC925 OFF   .
   Closes AP3 Beam Stop

::: ABORT_MASK AP1_120_PS ENABLED .
   The P67 abort for 120 GeV power supplies is masked since we will be running 8 GeV beam.

::: ABORT_MASK AP1_8_PS DISABLED   .
   The P67 abort for 8 GeV power supplies is unmasked to prepare for 8 GeV operation.

::: ABORT_MASK PBAR_SOFT ENABLED   .

       The P67 software abort is unmasked.

::: EVENT 88 TRIGGER   .
     Triggers a TCLK event $81, which is a Debuncher beam permit system reset
     event.

::: BOOST_INTENSITY EVT16 2   .
     Booster event $16 is set to 2 turns 35 bunches.

::: SETIT_DEVICE V:PSHOOT =4   .
     V:PSHOOT having a state of 4 means "Ready for Main Injector Tune up."   The
     Main Injector Shot Transfer Line Tune-up aggregate waits for PSHOOT to be set
     to 4 before starting its beam line tune-up.

::: BEAM_SWITCH PBAR_SOURCE ON   .
     Turns on the Pbar beam switch to allow 8GeV beam for Main Injector tune-up.

::: ACKNOWLEDGE   .

Beam cooled into Core?

OK   Cancel

::: CTLIT_DEVICE A:SPPS01 OFF   .
     Turns off the Accumulator stacktail pin switch.   Once all of the beam that
     was in the stacktail is swept over into the core, the stacktail can be turned
     off.

::: SET_SEQ FILE 28   .
     File #28 turns off the Accumulator stacktail high level amps.
     A:SPAH11 TURN DEVICE OFF   ok
     A:SPAH12 TURN DEVICE OFF   ok
     A:SPAHD1 TURN DEVICE OFF   ok
     A:SPAHD2 TURN DEVICE OFF   ok
     A:SPAHD3 TURN DEVICE OFF   ok
     A:SPAHD4 TURN DEVICE OFF   ok

::: SET_SEQ FILE 94   .
     File #94 enables core power leveling.   Power Leveling (no relation to Pbar
     Expert Tony Leveling) automatically adjusts the cooling attenuation to obtain
     a target power setting.   After power leveling has been enabled, attempts to
     adjust the cooling power by moving the pin attenuator from a parameter page
     or P34 will fail, because the power leveling will readjust the pin
     attenuators to reach its target power.   The power levels are determined by
     the diode settings for each cooling band. The more negative the diode
     voltage, the higher the power. The diode settings are not obvious to the
     casual observer and what diode settings correspond to what power settings are
     determined by Pbar experts.   File #94 first sets the diode values for the
     three horizontal and vertical cooling bands.
     A:CH1D1 SET DEVICE   -2.1   ok
     A:CH2D1 SET DEVICE   -2.5   ok
     A:CH3D1 SET DEVICE   -2.4   ok
     A:CV1D1 SET DEVICE   -2.4   ok
     A:CV2D1 SET DEVICE   -3.0   ok
     A:CV3D1 SET DEVICE   -2.7   ok
     File #94 also sets the diode settings for both the 2-4GHz and 4-8GHz core
     momentum systems.
     A:CMPAD1 SET DEVICE   -3.0   ok
     A:CPPAD1 SET DEVICE   -.34   ok
     File #94 then enables power leveling on the core horizontal and vertical
     systems by issuing on commands to the diodes.
     A:CH1D1 TURN DEVICE ON   ok
     A:CH2D1 TURN DEVICE ON   ok

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        A:CH3D1 TURN DEVICE ON                                          ok
        A:CV1D1 TURN DEVICE ON                                          ok
        A:CV2D1 TURN DEVICE ON                                          ok
        A:CV3D1 TURN DEVICE ON                                          ok
        File #94 then enables power leveling on the core 2-4GHz and 4-8GHz momentum
        systems by setting the diode parameter polarity positive.
        A:CMPAD1 SET POSITIVE                                           ok
        A:CPPAD1 SET POSITIVE                                           ok
::: CHECK_DEVICE A:CH1D1 ON       .
        Verifies that power leveling is enabled for core horizontal band one cooling.
::: CHECK_DEVICE A:CH2D1 ON       .
        Verifies that power leveling is enabled for core horizontal band two cooling.
::: CHECK_DEVICE A:CH3D1 ON       .
        Verifies that power leveling is enabled for core horizontal band three
        cooling.
::: CHECK_DEVICE A:CV1D1 ON       .
        Verifies that power leveling is enabled for core vertical band one cooling.
::: CHECK_DEVICE A:CV2D1 ON       .
        Verifies that power leveling is enabled for core vertical band two cooling.
::: CHECK_DEVICE A:CV3D1 ON       .
        Verifies that power leveling is enabled for core vertical band three cooling.
::: CHECK_DEVICE A:CMPAD1 POSITIVE       .
        Verifies that power leveling is enabled for the core 4-8GHz momentum cooling.
::: CHECK_DEVICE A:CPPAD1 POSITIVE       .
        Verifies that power leveling is enabled for the core 2-4GHz momentum cooling.
::: SET_SEQ FILE 30               .
        File #30 turns on the 4-8GHz momentum cooling and sets the 2-4GHz momentum
        cooling pin attenuator such that very little power is in the 2-4GHz system.
        A:CPPA01 SET DEVICE           29.5                             ok
        A:CMPA01 SET DEVICE           20                               ok
        A:CMTW01 RESET DEVICE                                          ok
        A:CMTW02 RESET DEVICE                                          ok
        A:CMTW01 TURN DEVICE ON                                        ok
        A:CMTW02 TURN DEVICE ON                                        ok
        A:CMPS01 TURN DEVICE ON                                        ok
        A:CMPS01 DIG_ALARM ENABLE                                      ok
        A:CMTW01 DIG_ALARM ENABLE                                      ok
        A:CMTW02 DIG_ALARM ENABLE                                      ok
::: CTLIT_DEVICE A:CMTW01 ON       .
        Turns on one of the two core 4-8 momentum TWTs.  An "on" command was already
        issued to this device in file 30 above, but is issued again for redundancy.
        The CTLIT command issued here not only issues and "on" command to the device,
        but also waits for a short period of time and then verifies that the device
        is in the "on" state.
::: CTLIT_DEVICE A:CMTW02 ON       .
        Turns on one of the two core 4-8 momentum TWTs.  An "on" command was already
        issued to this device in file 30 above, but is issued again for redundancy.
        The CTLIT command issued here not only issues and "on" command to the device,
        but also waits for a short period of time and then verifies that the device
        is in the "on" state.
::: CHECK_DEVICE A:ISHTST READING .
        Verifies that the accumulator injection shutter is in the closed position
        (value =2) and displays the results in the message window at the bottom of
        the sequencer.
::: CHECK_DEVICE A:ESHTST READING .
        Verifies that the accumulator extraction shutter is in the closed position
        (value =2) and displays the results in the message window at the bottom of
        the sequencer.
::: CHECK_DEVICE A:R2HLSC ON       .
        Verifies that ARF2 HLRF is on.
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::: CHECK_DEVICE A:R3HLGS ON   .
     Verifies that the ARF3 gap is shorted. ARF3 is used during studies to move
     the beam.   From a parameter page, A:R3HLGS will show an "S" in the polarity
     bit when it is shorted.   If it is not shorted, the Pbar Sequencer operator
     can go to P8 ARF1 <1>.   Note that the A:R3LLT2 timer must be enabled for you
     to drive the cavity short in. Pbar experts should be consulted before
     driving the cavity short in.
::: ALARM_LIST PBAR 38   .
     Bypasses the "CORE HOR" alarm list.

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ok   ACKNOWLEDGE   .

Collider Aggregate: Run II Start Reverse Protons has been
completed.
Next Aggregate: Run II Switch to Shot Lattice
How to get back to stacking: Run the Run II Return to Stacking
Aggregate.