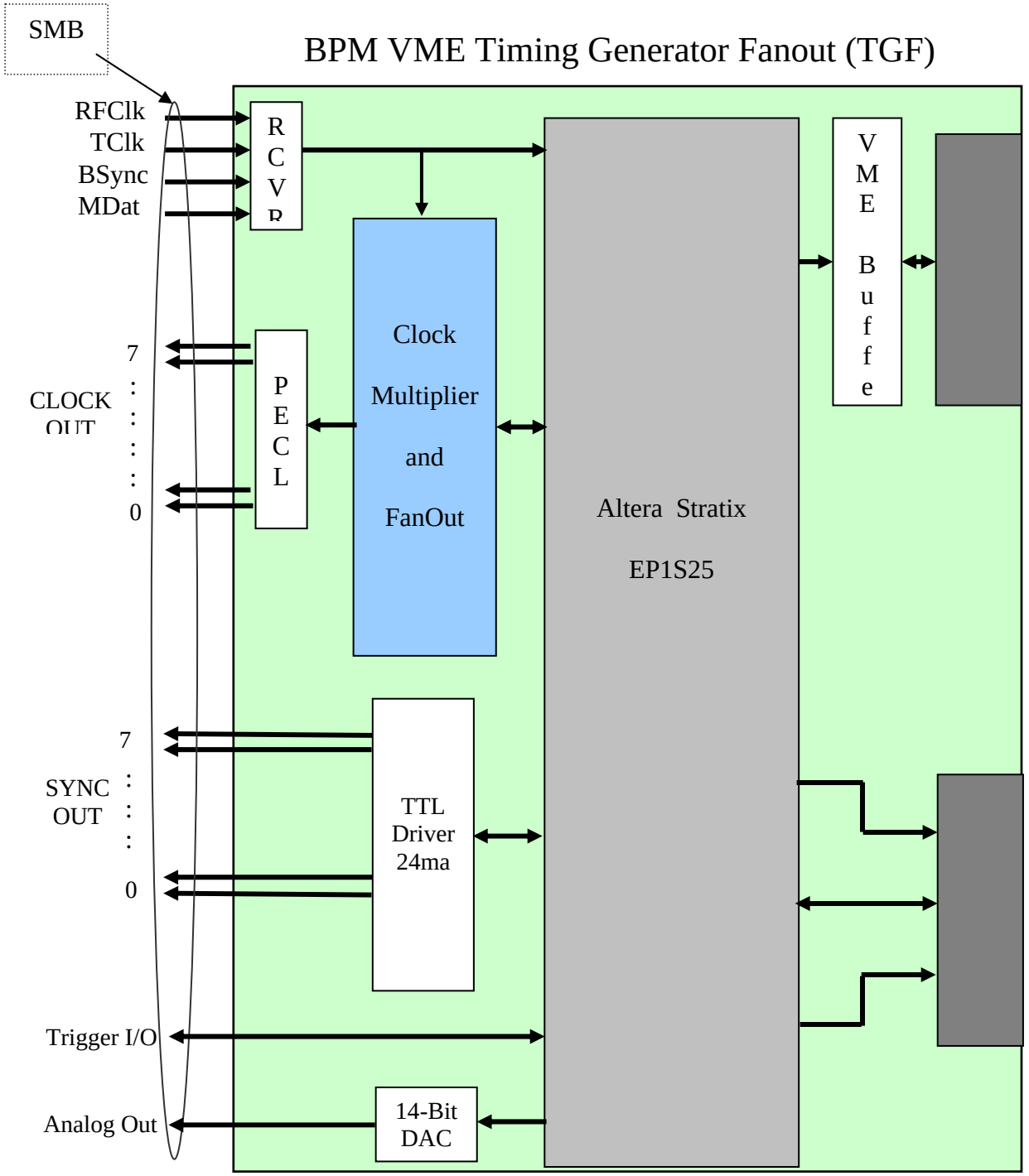
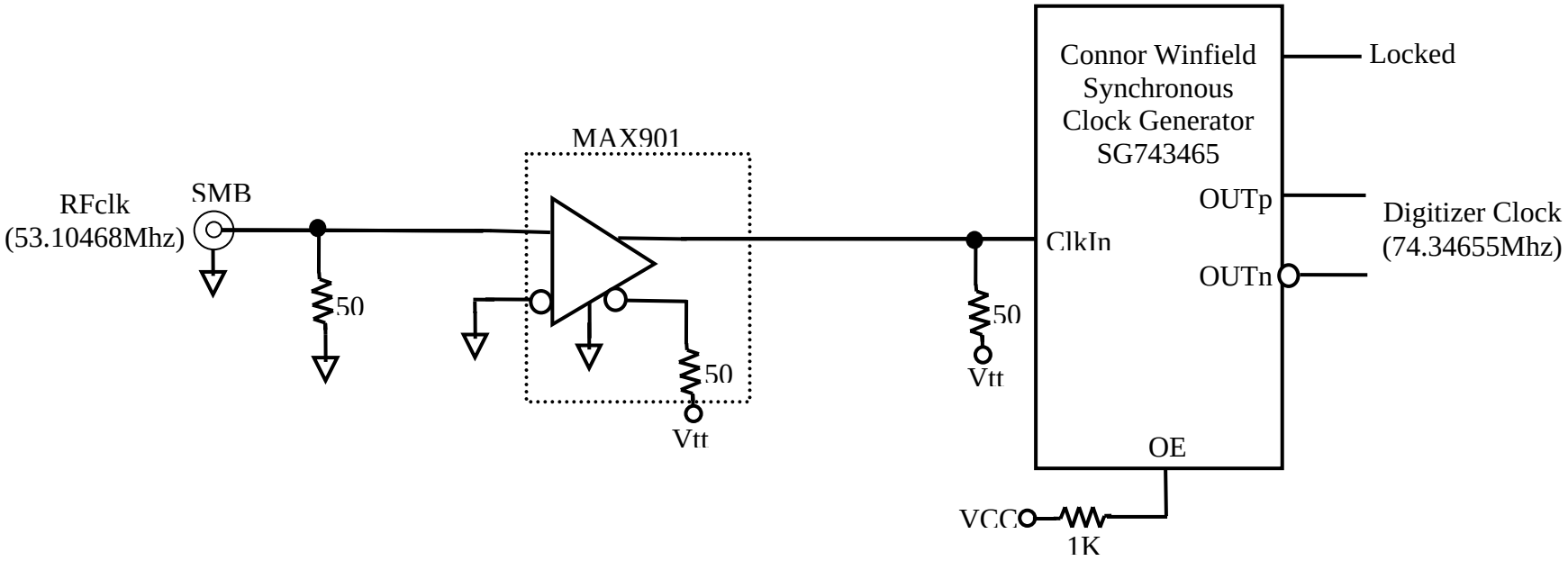
BPM VME Timing Generator Fanout (TGF)
Features

- 8 - Clock Outputs PhaseLocked to the 53.10468Mhz Clock
    - Currently Clock outputs are 7/5 x the RFClk
- 8 - ADCSync Outputs are Timed from the BSync input w/
    - One common Pretrigger delay (delay by # turns)
    - Number of ADCSync's generated (once per turn) per output
    - ADCSync delays per output are accurate to a ½ bucket resolution
    - All Timing and Delays are configurable by VME
- 2 - VME Interrupts (level 5 or 6) can be generated, typically for
    - From on BSync events
    - From on TClk events (up to 16 events)

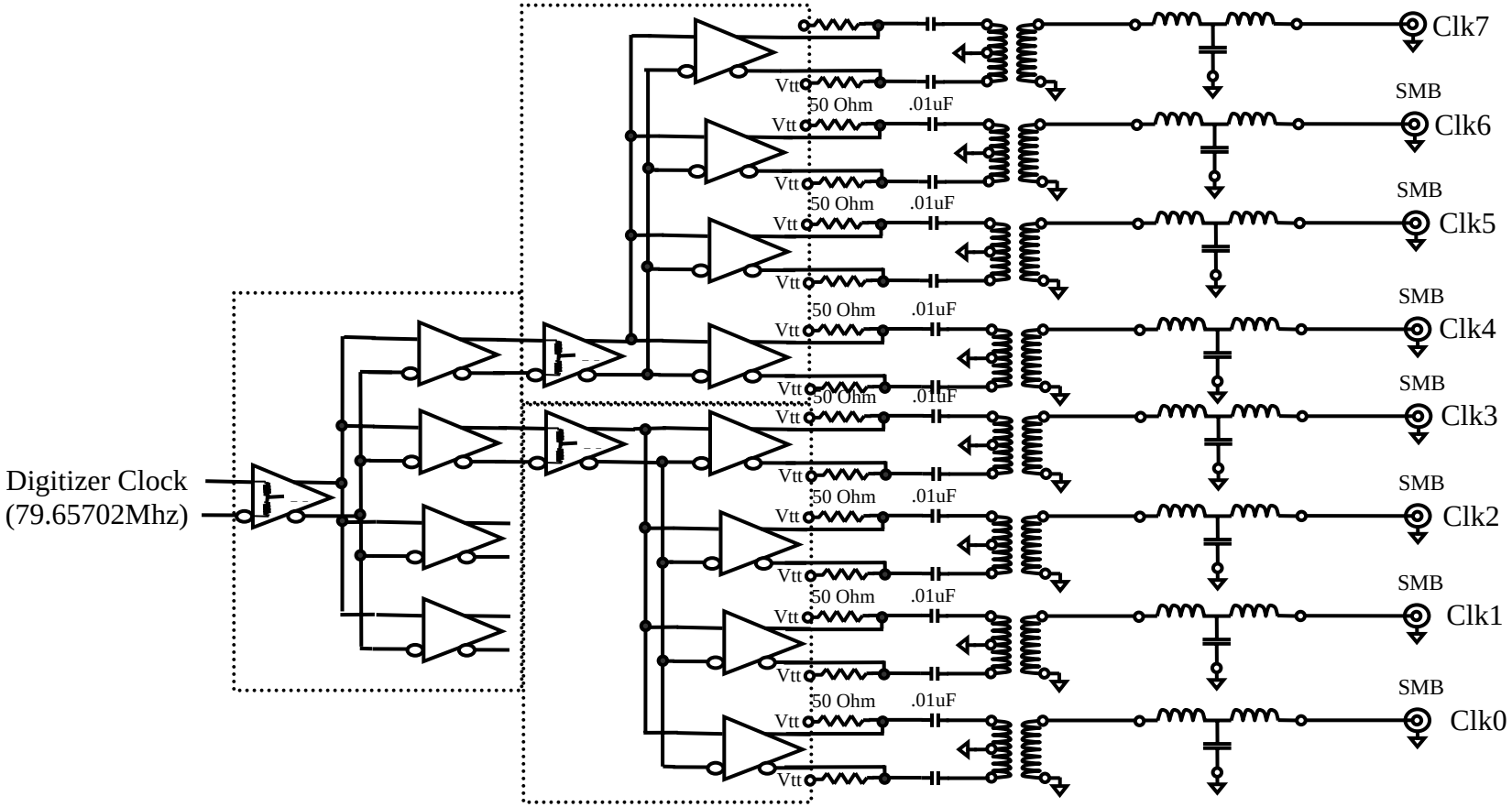
- Time Stamp counter (64-bits) with ½ bucket resolution
    - Cleared on a BSync start event
    - Records the First Turn Register after a start event
    - Records Bsync Time Stamp event
    - Records TClk Time Stamp event
- Stores the occurance of all Bysnc & TClk events
    - Used to verify that events are present at a particular location
- Controls diagnostics for inhouse designed filter cards
- Contains an ID Rom for version control

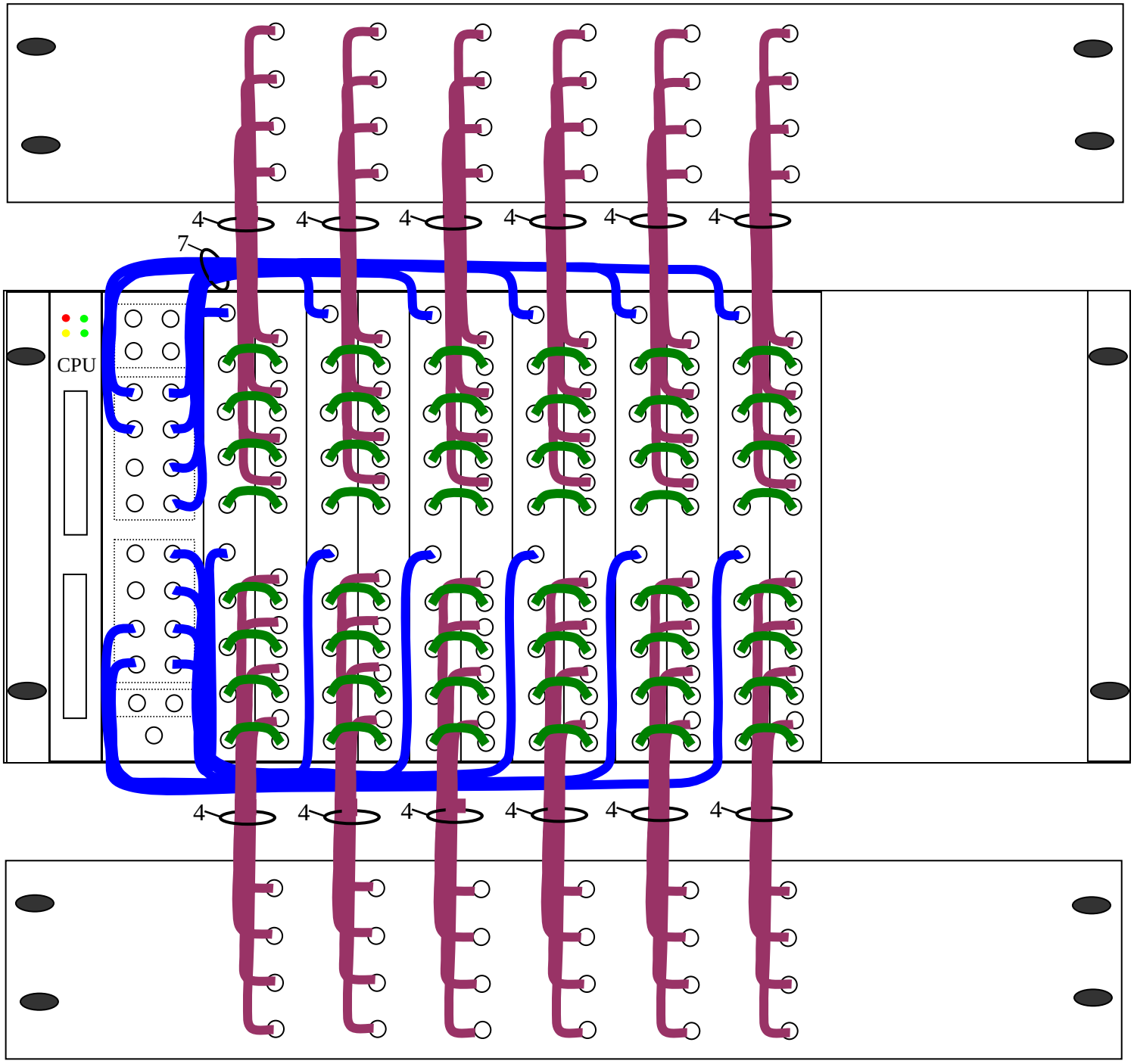

BPM VME Timing Generator Fanout (TGF)
SMB
RFClk
TClk
BSync
MDat
R
C
V
P
Clock
Multiplier
and
FanOut
P
E
C
L
7
:
:
:
:
0
CLOCK
OUT
Altera Stratix
EP1S25
V
M
E
B
u
f
f
e
7
:
:
:
:
0
SYNC
OUT
TTL
Driver
24ma
Trigger I/O
Analog Out
14-Bit
DAC

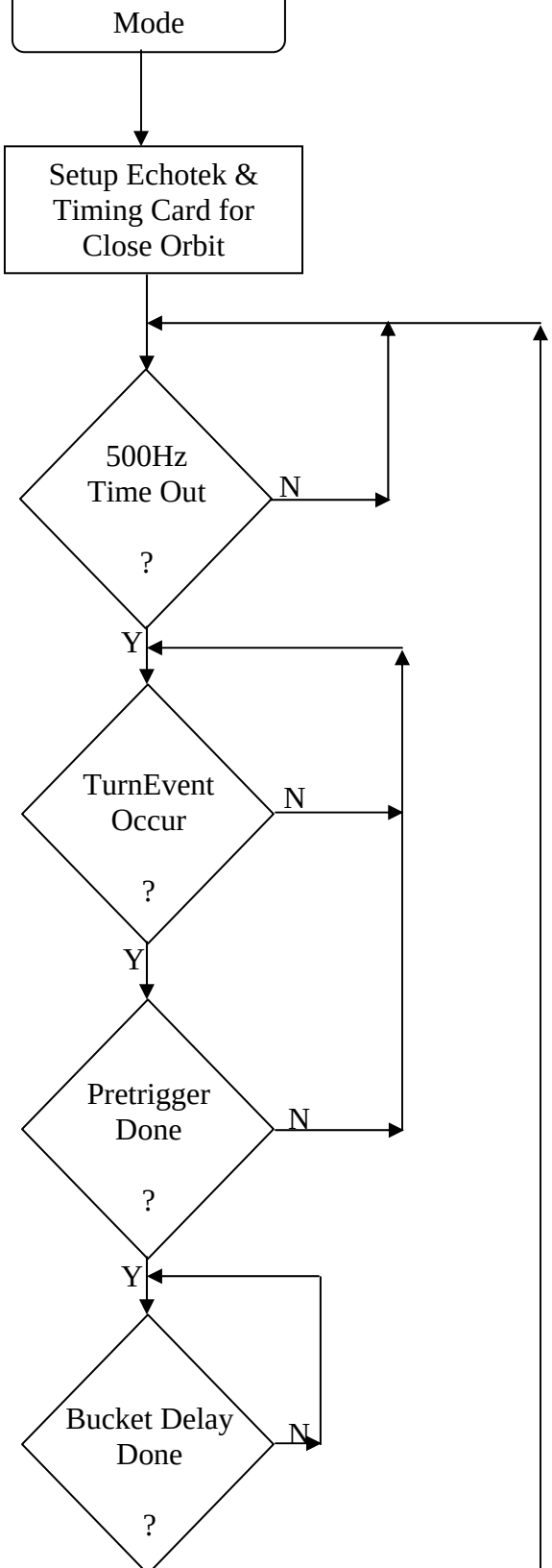
Clock Generation
(74Mhz)

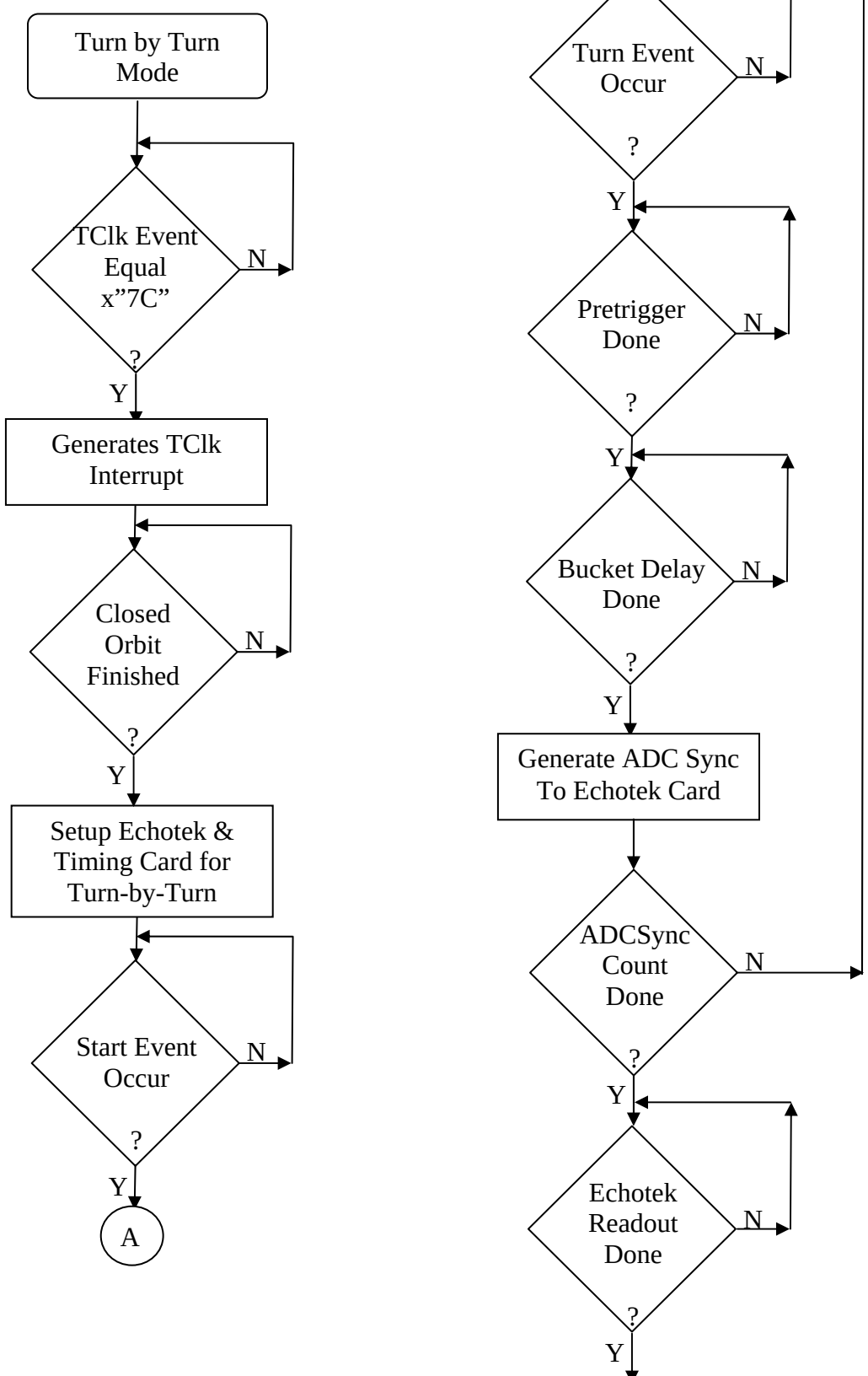


Clock Fan Out




4
4
4
4
4
4
7
CPU
4
4
4
4
4
4
CPU
Fanout
ADC
Relay
ADC
Relay
ADC
Relay
ADC
Relay
ADC
Relay
ADC
Relay


Mode
Setup Echotek & Timing Card for Close Orbit
500Hz Time Out ?
N
Y
TurnEvent Occur ?
N
Y
Pretrigger Done ?
N
Y
Bucket Delay Done ?
N


Turn by Turn Mode
TClk Event Equal x"7C"
N
?
Y
Generates TClk Interrupt
Closed Orbit Finished
N
?
Y
Setup Echotek & Timing Card for Turn-by-Turn
Start Event Occur
N
?
Y
A
Turn Event Occur
N
?
Y
Pretrigger Done
N
?
Y
Bucket Delay Done
N
?
Y
Generate ADC Sync To Echotek Card
ADCSync Count Done
N
?
Y
Echotek Readout Done
N
?
Y