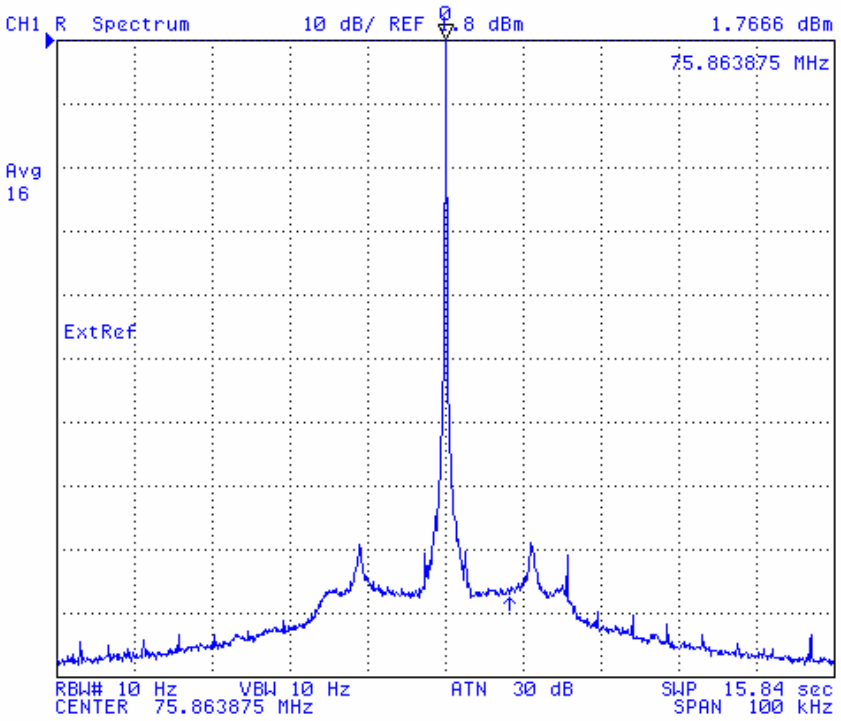
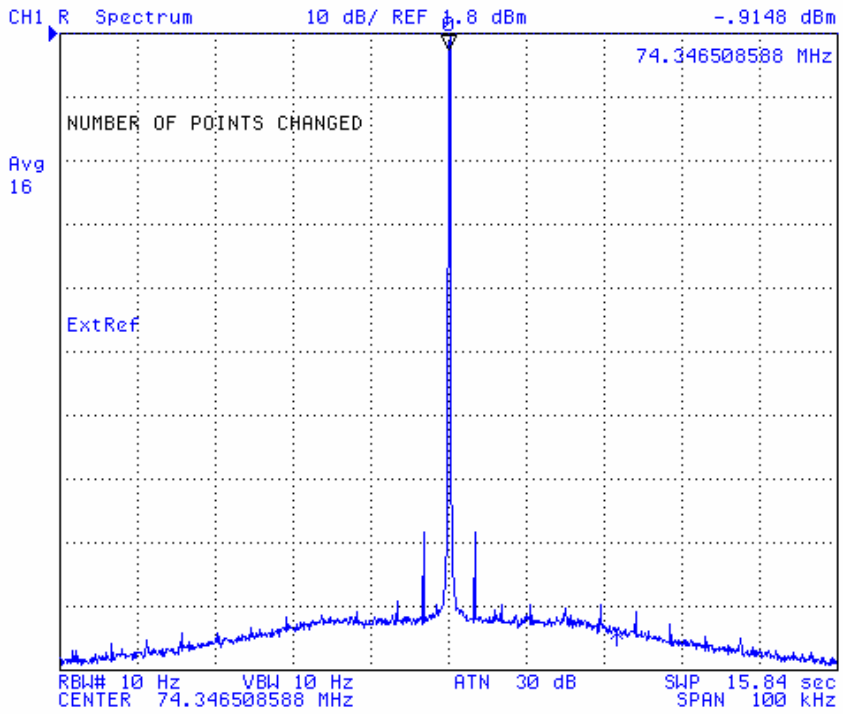
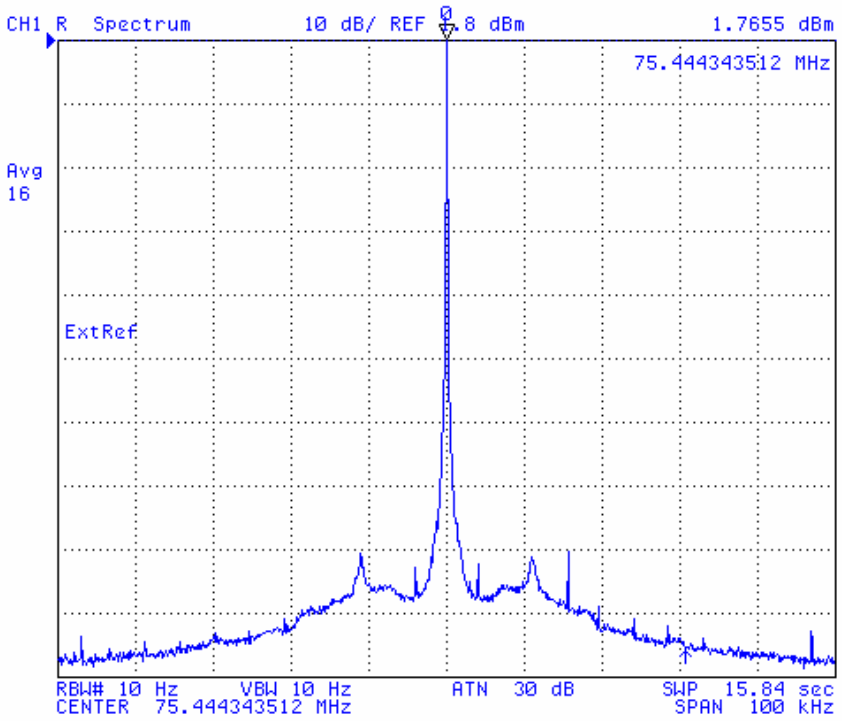
May 9, 2005



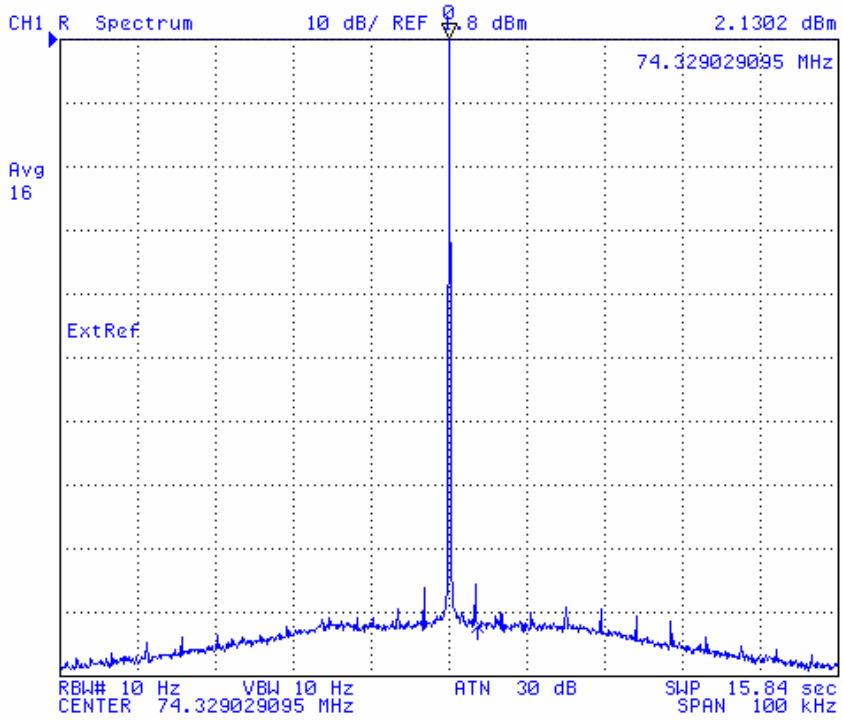
FPGA PLL with 10/7 ratio and 53.10468Mhz input



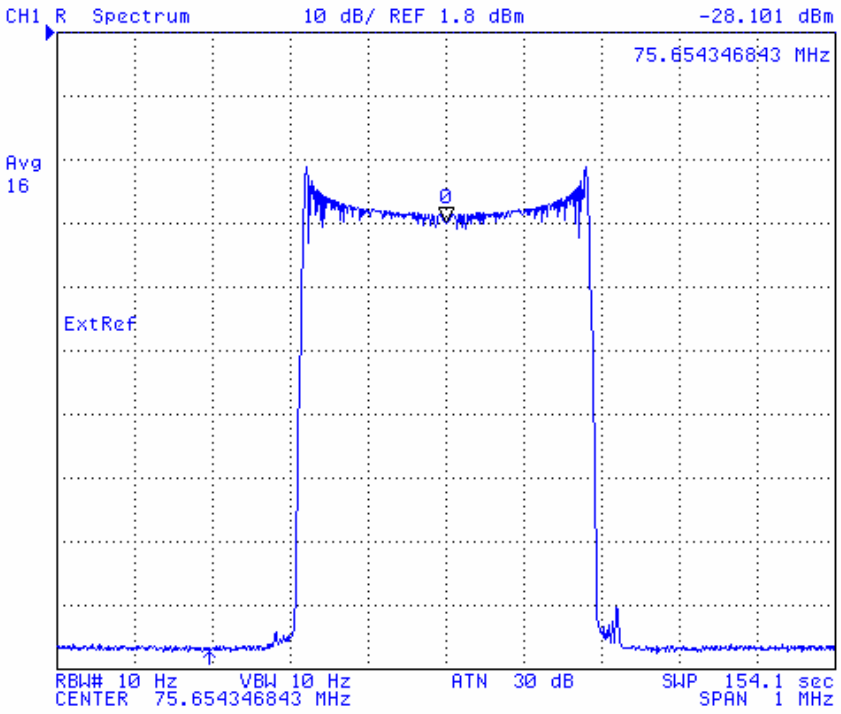
Conner Winfeld PLL with 7/5 ratio and 53.10468Mhz input



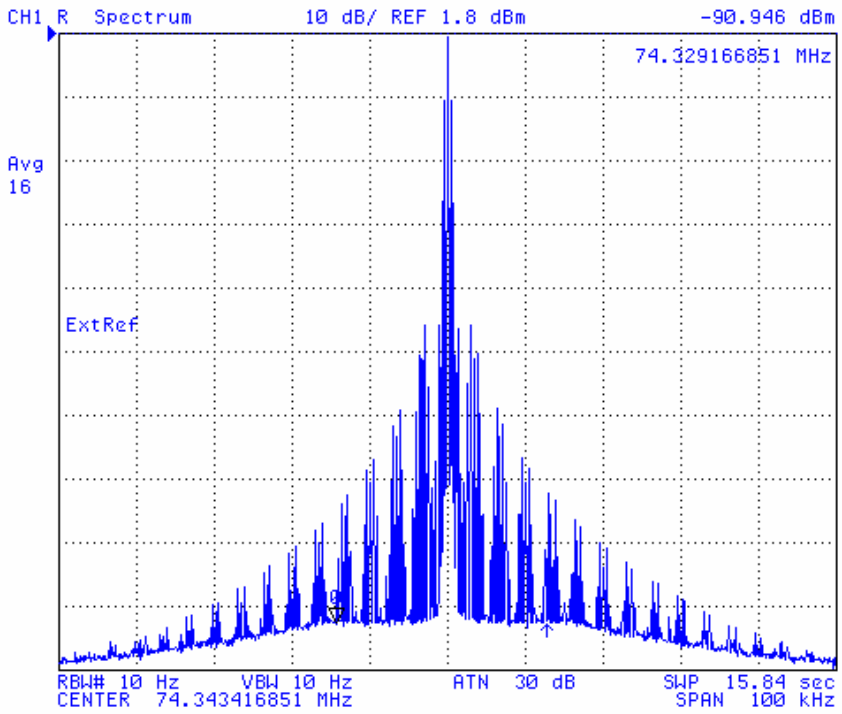
FPGA PLL with 10/7 ratio and 52.81100Mhz input



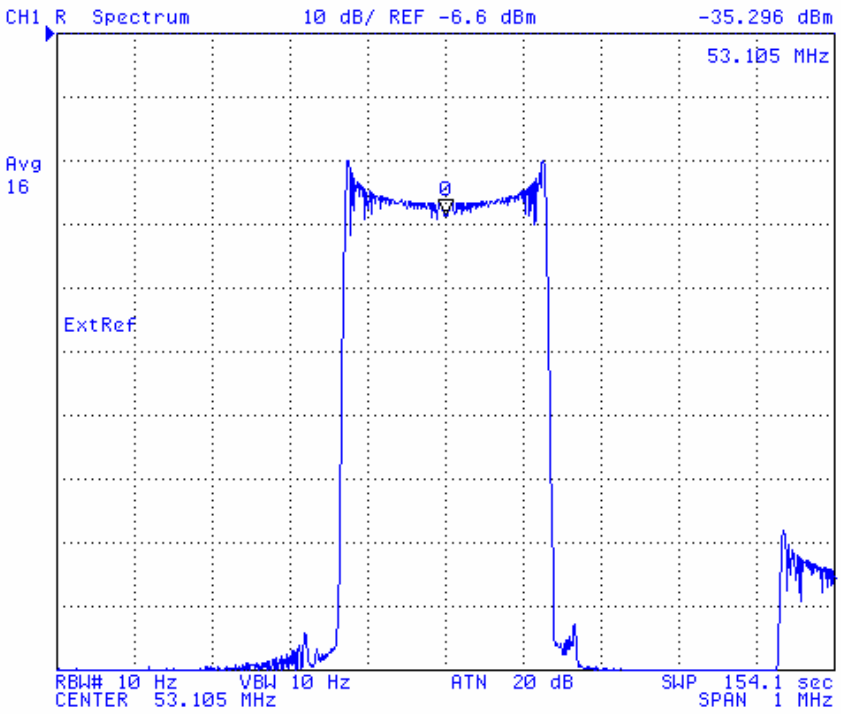
Conner Winfeld PLL with 7/5 ratio and 52.81100Mhz input
Does Not Lock to Input
Equal to 53.09215Mhz at input



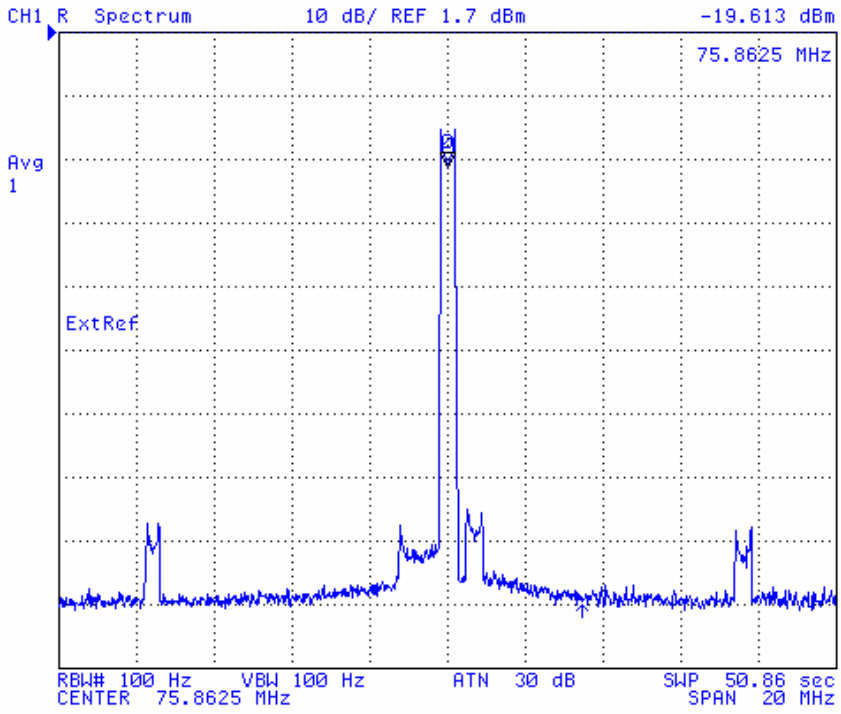
FPGA PLL with 10/7 ratio and 52.95784Mhz input
Modulated at 125Khz



Conner Winfeld PLL with 7/5 ratio and 53.10244Mhz input
Modulated at 20Khz



Marconi 2022D Generator set at 53.10468 Mhz
Modulated at 125Mhz w/ a sweep of 400Hz



FPGA PLL with 10/7 ratio and 52.95784Mhz input
Modulated at 125Khz (Span 20Mhz)