First Results of a Longitudinal Phase Monitor at the TEVATRON

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Abstract

A digital beam phase monitor has been installed on the TEVATRON ring. This device will be mainly use to diagnose the energy oscillations of each of the 36 × 36 proton and antiproton bunches as well as to study the transient beam loading. The first results obtained from the beam phase monitor is presented on the paper.

INTRODUCTION

The Fermilab TEVATRON is colliding 36 proton against 36 antiproton bunches with an energy of 1.96 TeV at the center of mass. The bunches are equally separated in 3 trains. The bunch spacing within a train is ∼396 ns corresponding to 21 RF buckets (53.106 MHz) and 139 empty buckets (∼2.6 μs) separate the trains. A longitudinal phase monitor has been developed in order to measure the phase of each proton and antiproton bunch with respect to the RF. This paper presents the first results obtained with the phase monitor which is operational at the TEVATRON since January 2005. Our experimental results are limited to one single coalesced proton bunch (the behavior with uncoalesced bunches as well as antiproton bunches being under investigation).

SYSTEM OVERVIEW

A schematic layout of the longitudinal phase monitor is presented in Figure 1.

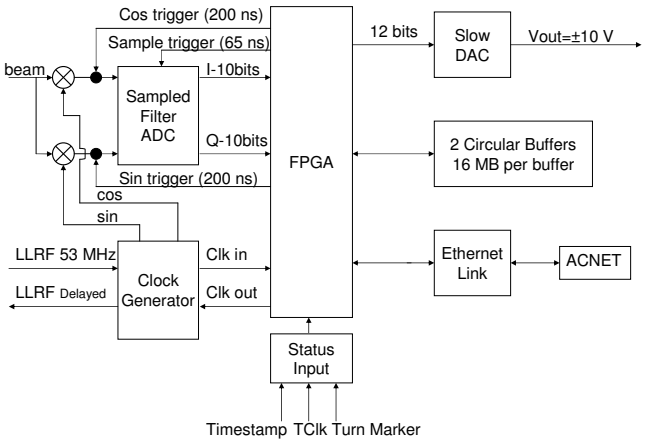

Figure 1: Schematic of the Longitudinal Phase Monitor

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Inputs

The input signal is supplied by summing the signals as the beam passes a top and bottom vertical strip lines located at the E0 hall. The strip lines signal is first received by a differential amplifier (not reported in Figure 1) which provides balanced output gain and phase matching. From the differential output, the signal is multiplied by a sine and cosine waveforms created by a lookup table with both phases locked to the 53 MHz input reference frequency. The sine and cosine products are each integrated in parallel over a 200 ns gate. The two integrated sine ("I") and cosine ("Q") products are then sampled by a 20 MSPS , 10-bit Analog Digital Converter (ADC). The ADC clock has a period of ∼65 ns. On the rising clock edge, the ADC samples both input channel. Valid data "I" and "Q" are available 3 clock cycles later. A Field Programmable Gate Array (FPGA) controls the synchronization so that the ADC samples at the end of the integration gate. The FPGA performs also the phase calculation by dividing "Q" samples by "I" samples and taking the arctan of the result. The final phase calculation is a 12-bit result.

Outputs

The longitudinal phase monitor provides three output modes : SLOW Digital Analog Converter (DAC), Circular Buffers and Oscillation Amplitude Detector. In the present time, only the two first are operational.

In the SLOW DAC mode, each phase of the selected bunch is calculated every turn and averaged over 128 turns. The resulting average phase is then converted into a voltage, using a 12-bit serial input DAC. This gives an effective output rate of 373 Hz.

The longitudinal phase monitor includes an external memory bank, consisting of two 10 minutes LIFO circular buffers. The format of the buffers consist of sequential arrays of 39 elements each. Each array, completed every 128 turns, has the following format:

1. an incrementing 32-bit sample count, indicating the start of the buffer
2. a 16-bit average phase of the following 36 data elements
3. the 16-bit average phase over 128 turns for each of the 36 bunches

Each buffer has the capability to be started and stopped either by a manual trigger or by a programmed TCLK

event. These controls can be accessed via the ethernet or the ACNET controls system.

In the Oscillation Amplitude Detector mode, the same 39 element array will be processed to output an envelope that contains the magnitude of the phase variation for each bunch. This output is still in progress.