



Fermilab/BD/MI
Beams-doc-2083
July 24, 2006

Electronic Design Document

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Abstract

This document contains the specification for the Timing Generator Fanout (TGF-II) for the Beam Position Monitor (BPM) upgrade for the Main Injector at Fermilab. All required operating modes, system timing, diagnostics and interactions with the BPM software are described in this document

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Overview

This document describes the Timing Generator Fanout (TGF-II) needed for the precision timing and synchronization of the data acquisition readout of the Main Injector Beam Position Monitor (BPM) upgrade project. The data acquisition (DA) hardware digitizes the analog position signal from the BPM sensors, amplify them and digitally filter the signals and make them available to a VME front-end computer. Figure 1 shows the functional block diagram and the different elements involved with the BPM upgrade project.

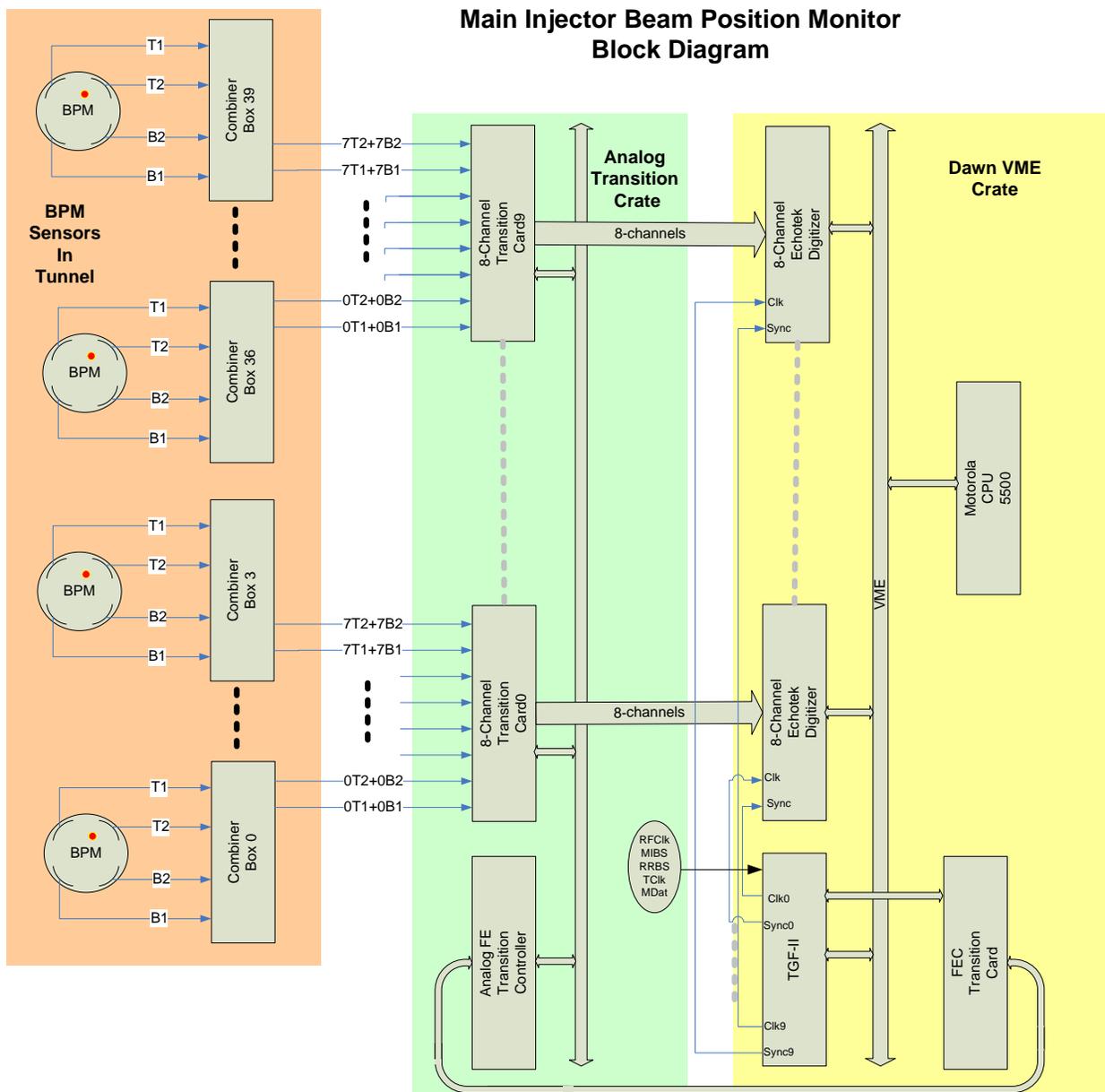


Figure 1 BPM Front End Functional Block Diagram

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The hardware of Figure 1 consists of:

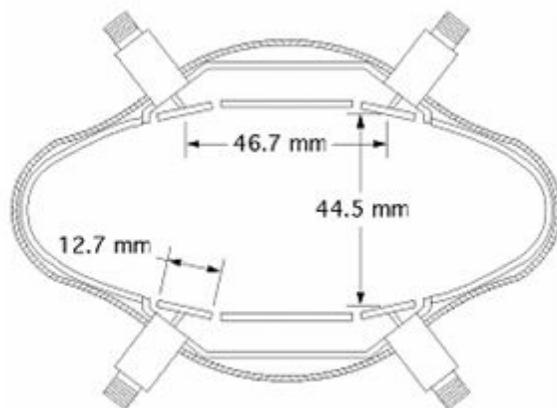
- 1) Amplification and signal conditioning of the BPM sensor signals in the Combiner Box and the Transition card, designed at FNAL.
- 2) The precision timing functions are implemented in the VME Timing Generator Fanout (TGF-II) module, designed at FNAL.
- 3) The control and diagnostics of the Transition Cards are performed by the Transition Controller interfaced to the TGF-II.
- 4) The Digital Signal Receiver (DSR) is a Commercial-Off-The-Shelf (COTS) module from Echotek Corporation, the ECDR-GC814/8-FV2.
- 5) The VME sub rack controller is a COTS Single Board Computer from Motorola Corporation, the MVME5500

Beam Position System

BPM Sensor¹

The Main Injector has four BPM detectors per betatron wavelength in both the horizontal and the vertical planes. There are a total of 208 BPMs for the 3320 m ring. Out of these, 203 are MI style ring BPMs, and are located in the downstream end of every MI quadrupole. The other 5 are wide aperture BPMs located at Q101, Q402, Q522, Q608 and Q620 locations.

The BPM detectors in MI consist of four transmission line strips, or strip-lines, located on the perimeter of the beam pipe. The strip-lines are 250 mm long and 12.7 mm wide. They are positioned at a distance of 46.7 mm horizontally and 44.5 mm vertically, center to center as shown below.



BPM Sensor inside quadrupole beam pipe

The pick-up has a characteristic impedance of 50Ω , determined by the gap between the strip and the beam pipe. The current BPM RF module input impedance is matched to 50Ω within a 5 MHz

¹ Requirements for the Main Injector BPM upgrade, D. Capista, A. Marchionni

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bandwidth centered at 53MHz. The outputs are combined in pairs externally to form either a horizontal or a vertical detector. Each strip-line is shorted at one end and connected to a ceramic feed-through at the other end, which makes these BPMs non-directional. At present any BPM measures either the horizontal or the vertical position per cycle at each quadrupole. It can be remotely switched to the orthogonal mode.

The wide aperture BPMs, with 6" long plates and a 4.625" aperture, are located adjacent to the Lambertson magnets and are mounted external to the quadrupole magnets.

BPM Data Acquisition System

The BPM signals pass through the Combiner Box for band pass filtering (53 MHz & 2.5 MHz) and to the 8-Channel Transition Card for and additional filtering and amplitude control. These conditioned signals are fed to an 8-channel digitizer from Echotek. Timing for the digitizer and the CPU are performed by the Timing Generator Fanout (TGF-II). Timing to the digitizer consists of a Clock and a Sync (or gate) input based on six Main Injector timing signals. 1) The Main Injector RF Clock (RFClk) operating from a range of 52.8Mhz to 53.1Mhz, 2) Main Injector BSync (MIBS), operating at 7.5Mhz and synchronous the MI beam, 3) Recycler BSync (RRBS), operating at 7.5Mhz and synchronous to the Recycler Beam, 4) Booster Extraction Sync (BES), 5) TCik operating at 10Mhz and asynchronous to the beam containing accelerator-complex-wide commands, and 6) MDat operating at 10Mhz also asynchronous to the beam and containing accelerator-complex-wide commands.

The sensor front-end electronics depicted in Figure 1 are contained in two separate sub racks. The 8-channel Transition cards is installed in a VME style sub rack but is strictly for mechanical purposes and convenience. Up to 10 Echotek digitizers can be installed in a standard VME sub rack and controlled by a commercial CPU and timed synchronously to the Main Injector beam by the TGF-II. The BPM sensor front-end electronics gain and filter selections are controlled by the Front End Controller (a VME transition card inserted in the rear I/O area in the same slot as the TGF-II card). Figure 2 illustrates the organization of the cards in the BPM VME sub rack. One sub rack can hold the necessary electronics needed for a service building (sometimes called a house). There are 7 service buildings or houses around the Main Injector ring and each BPM house can have up to 10 BPM digitizing boards.

The BPM digitizing modules are Echotek module ECDR-GC814/8-FV2, and each module digitizes signals from 8 channels. An individual BPM sensor generates information on 4 channels – the A and B plates for the proton end of the sensor and the A and B plates for the antiproton end. Therefore one Echotek module will be capable of accepting signals from two BPM sensors. The digitized output that results from each channel of the digitizing module may be sent on for further processing or be used to generate a calculated position when processed with data from the matching plate channel. The details are in the Software Specifications document. If the output is the digitized and filtered signal data, each channel is actually represented by two components: a real (Q) and imaginary (I) part. The digital filtering on the Echotek module can also be disabled allowing a raw, oscilloscope type view of the signal.

The operation of the Echotek module is controlled by two inputs that are common for all eight channels. They are the CLK and SYNC signals. The digitizing clock paces the Echotek module

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and comes from the BPM Timing Generator Fanout (TGF-II) Module. A phase-lock-loop on the Timing module creates a clock output that has a fractional relationship to the Tevatron RF clock frequency. TeV RF is approximately 52.8 MHz. The Echotek clock is $10/7^{\text{th}}$ or approximately 75.43 MHz. This means that the 52.8 MHz signal is technically under-sampled but the signals-of-interest are modulated onto that RF signal and filtering and signal processing techniques allow the module to extract those signals-of-interest. The digitization process can be gated, singly triggered or triggered for a specified number of samples by the SYNC signal. SYNCs are generated in the TGF-II and normally initiated with respect to the Main Injector BSync (MIBS) or Booster Extraction Sync (BES) event. There are two additional decoders (MDAT & TClk) used to interrupt the VME CPU for notification of a Machine state change and alarms relative to a beam reset. The MIBS decoder or BES to the TGF-II can initiate digitizing sequences and can add fixed delays with a resolution of one-half RfClk period, in order to remove cable delays or to time-in similar actions between the widely separated service buildings around the Main Injector ring. The TGF-II card is capable of additional delay resolutions by changing the PLL count values of the FPGA firmware.

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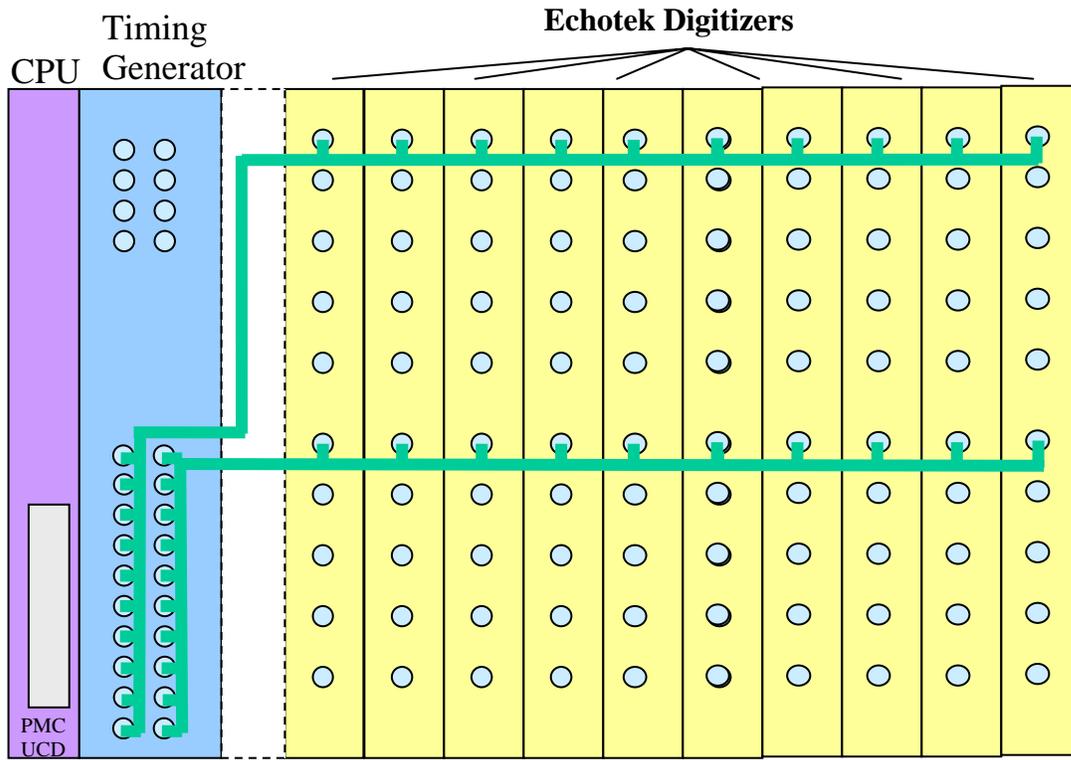


Figure 2. Sub Rack Module, Example Configuration

BPM Requirements

The requirements for this system are based on the system requirements documented in Main Injector BPM Upgrade Requirements Document (Beams Doc #1949). A summary of the functional requirements are:

- User defined turn-by-turn: A measurement of the orbit on every turn (588 53Mhz RF buckets) of every BPM for 2048 turns, performed in wide bandwidth mode.
- Injection and extraction turn-by-turn: A wide bandwidth measurement of the orbit on every turn of every BPM for each batch of the beam injected into the machine. It also provides the capability to measure the extraction turn of at least one portion of the beam extracted from the machine.
- Flash Frame: A single orbit measurement, performed in wide bandwidth mode for each BPM. The flash frame consists of the first turn that has beam for injections, or the last turn that had beam for extractions.
- Average Orbit: A narrow bandwidth measurement that consists of the orbit averaged over the first 512 turns of the flash turn buffer.
- Closed Orbit: A narrow bandwidth measurement collected from all BPMs at a rate of 500Hz.
- Display Frame: A narrow bandwidth measurement triggered by the profile frame TClk (0x7B). Data for this measurement is pulled from the closed orbit buffer.
- Profile Frame: A narrow bandwidth measurement triggered by the profile frame TClk (0x7A). Data is pulled from the closed orbit buffer.

Data Acquisition

Functional Overview

The communication between the front-end processor and the Echotek modules happens through the VME backplane.

Data coming from the BPM are stored into a set of buffers in the sub rack controller. The depth and number of logical buffers that reside on the sub rack controller is defined in the Front-end Software Design Document (Beams Doc #1949). Some of the buffers, most notably the turn by turn data, is first stored in memory on the Echotek boards and then transferred to the sub rack controller on demand, as the processor/backplane does not have the bandwidth to acquire it in real time. The actual physical implementation of the sub rack controller buffers will be described in the front-end software design document.

Echotek Data Converter Module

The Echotek module ECDR-GC814/8-FV2 is the baseline data converter. This module belongs to a general type of modules called Digital Signal Receiver (or Radio) (DSR). These modules have high speed digitizers that convert the analog, usually radio frequency, inputs into digital information very early in the signal processing. This reduces the amount of analog circuitry in

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the system. The subsequent digital circuitry is used to down convert or base band the RF information, removing the high frequency carrier (52.8 MHz in this case) and revealing the information modulated onto that carrier, 48 KHz revolution information, 20 KHz betatron signals etc. The base banded signals are filtered in n stages of digital FIR filters and the output data is stored in a buffer memory on the module. In this Echotek module the 85 MHz, 14 bit Analog-to-Digital converter is followed by a Greychip Digital Down Converter (DDC) chip and then there is a re-programmable FPGA to route the data to onboard memory accessible to the VME bus. The sub rack processors can read out the data memory over the sub rack VME backplane.

Operation of the DAQ software is described in Beams doc #1949, *Main Injector Beam Position Monitor Upgrade Software Specifications for Data Acquisition*. The Echotek boards are configured by initialization files that are loaded during the startup process.

The data sheets for module are in the Appendix as Echotek DSR Module. The module front panel has eight input connectors, a digitizer clock and a synchronization input that can be used as a trigger or a gate. The module signals are described in more detail in the data sheets.

The firmware in the module can be updated by running the driver code software (?) and directing it to the new firmware object file. The system should be not running any other software at this time to avoid interference with the loading process. One Engineering Change Order (ECO) was applied to this module after consultation with Echotek Corp. The SYNC input termination resistor was lowered from 1000 ohms to 50 ohms to match the signal source and to fix a cross talk problem found early in testing.

Timing Generator Fanout (TGF-II) Module

The Timing Generator Fanout (TGF-II) is a double width, 6U VME card that generates timing signals that control and initiate acquisition of the BPM signals. The timing signals are based on inputs from the Main Injector clock system. These signal inputs include the Main Injector RFClk, BSync, TClk, MDat, Recycler BSync and Booster Extraction Sync (BES). The TGF-II is based on the design of the Tevatron TGF and is backwards compatible with a three exceptions. 1) There are ten Clock and Sync outputs instead of eight. 2) The turn counter firmware is 1176 for the Main Injector and 2226 half buckets for Tevatron. 3) the Clock output of the TGF-II is the RFClk times 10/7 for the main Injector rather than 7/5 for Tevatron.

The RFClk is the synchronization time base for the major functionality of the TGF. The RF frequency shifts as the energy of the beam changes and thus frequency values shown are usually approximations. The TGF internally doubles the RFClk to over sample and decode all other timing inputs (MIBS, RRBS, BES, MDat and TCLK) signals.

The BSync base frequency is one seventh of the RF Clock or approximately 7.5 MHz. events are encoded as an eight bit serial byte onto this carrier and can be extracted from it. An important event is the revolution timing mark (0xAA). This event allows synchronization with the pattern of particles circling around the Main Injector ring.

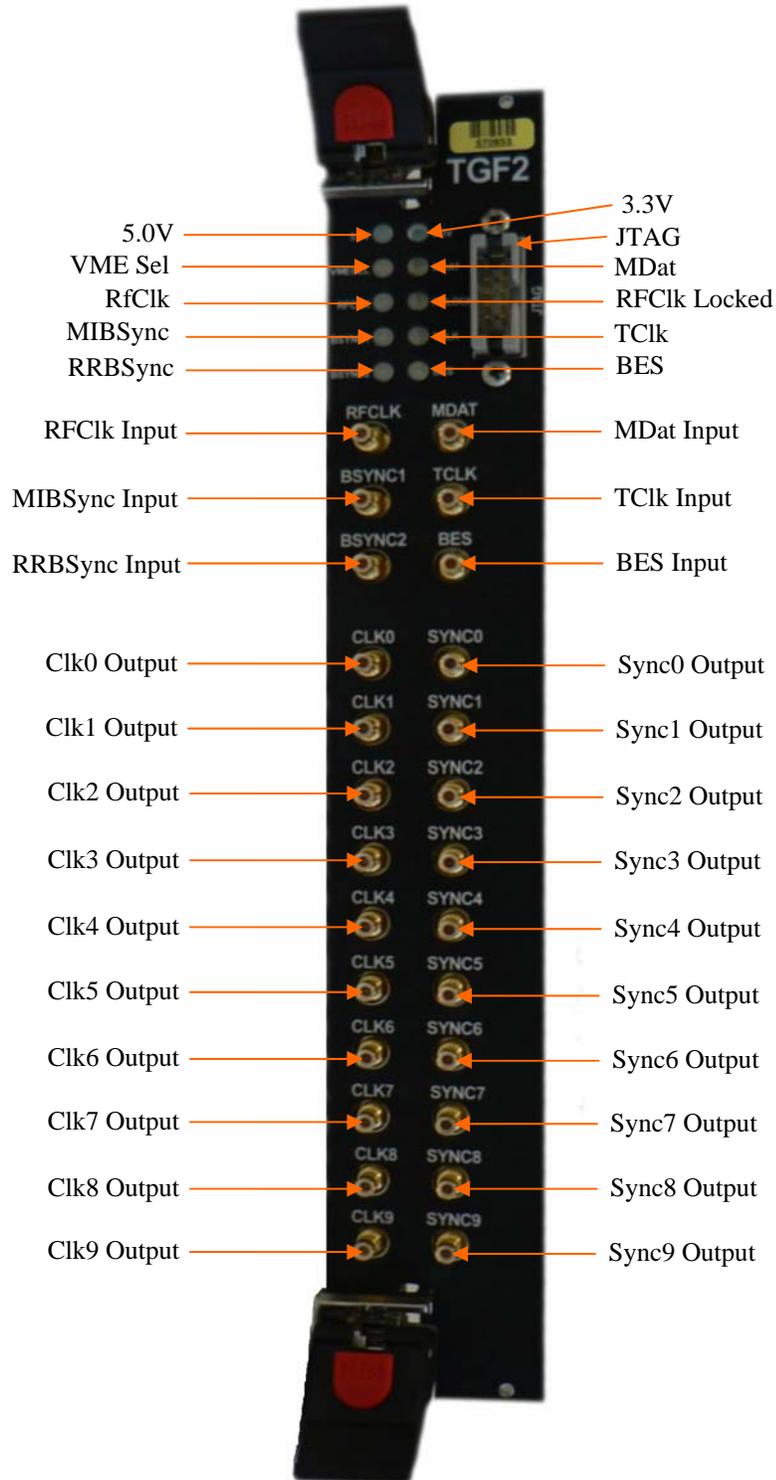
The TClk and MDat signals are encoded similar to BSync but with a 10MHz carrier frequency and from it the TGF-II can extract up to 255 events from each of the input signals. The TGF-II can be programmed to respond to any of up to sixteen selectable TClk events to interrupt the sub rack controller and any of those TClk events can generate up to 32 timer alarm interrupts with 1/2 bucket resolution.

For each Echotek DSR module the TGF-II creates a digitization time base clock that paces the data conversions and filtering on the board. It also supplies a trigger signal for control of the data acquisition. For the Main Injector BPM system, the TGF-II multiplies



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the RF clock frequency by exactly 10/7 to produce the digitization clock. The range of the Main Injector RFClk is approximately 52.8 MHz to 53.1 MHz. This produces range of the digitization rate of 75.43Mhz to 75.86Mhz. The TGF-II module can also generate other multiples of the RF Clock for the digitization clock.



Digitization operations will be triggered by and/or delayed from the BSync revolution timing mark or Booster Extraction Sync (BES) so that the acquired data are related to the particle bunches and measurements in separate service buildings are synchronized to each other as necessary.

Front Panel I/O Description

See **Error! Reference source not found.**

The Timing Generator Fanout Module inputs are:

- RFCLK – Main Injector RF Clock (52.8Mhz -53.1MHz). The RFClk must have signal level greater than 200mv and capable of driving an ac-coupled 50-ohm termination.
- BSync0 – Main Injector Beam Sync is an approximately ~7.5 MHz carrier with a modified Manchester encoding of Tevatron beam specific events. MIBS must be capable of driving 50-ohms with a signal level greater than +1.2v.
- BSync1 – Recycler Beam Sync is an approximately ~7.5 MHz carrier with a modified Manchester encoding of Tevatron beam specific events. RRBS must be capable of driving 50-ohms with a signal level greater than +1.2v.
- TCLK – Main Injector TClk, a 10 MHz carrier modulated by a fixed protocol of bit patterns that can carry commands and data events to electronics across the accelerator complex. TClk must be capable of driving 50-ohms with a signal level greater than +1.2v.
- MDAT – A 10 MHz carrier modulated like TCLK to carry Machine state data and events. TClk must be capable of driving 50-ohms with a signal level greater than +1.2v.
- BES – Booster Extraction Sync, a trigger pulse from the Booster that indicates a beam batch is being extracted to the Main Injector. BES must be capable of driving 50-ohms with a signal level greater than +1.2v.

The Timing Generator Fanout Module outputs are:

- A2D Clock signals [0-9] – the digitization clock to the Echotek modules. These regenerated clock outputs are based on a signal that is phase locked to the RFClk with a frequency of RFClk multiplied by 10/7. Output levels are >700mv into 50-ohms.
- A2D Sync signals [0-9] - the synchronization output for a sequence of digitization. The Sync output signals have a pulse width of ~50ns and are capable of driving a 50-ohm termination.
- An External Trigger Output (Trig0)–Allows an external device to be triggered from an internal firmware trigger condition such as a decoded BSync event. Currently set up to trigger on a Bsync Start event.
- An External Trigger Output (Trig1)–Allows an external device to be triggered from an internal firmware trigger condition such as a decoded BSync event. Currently set up to trigger on a BSync Turn event.

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- VME Interrupts for signaling the sub rack controller.
- Backplane connections that allow the TGF-II to control the Tevatron Filter Boards. These lines will also allow a level of auto-detection on a per sub rack basis so that the TGF-II will 'know' how many Filter boards there are to control.

The A2D Sync signal variations are:

- BSync trigger direct AA (turn marker) detect.
- BSync + programmable delay
- BSync + repeated programmable delay
- BES – Similar to above BSync except it is a direct trigger and bypasses the Manchester decoding section.

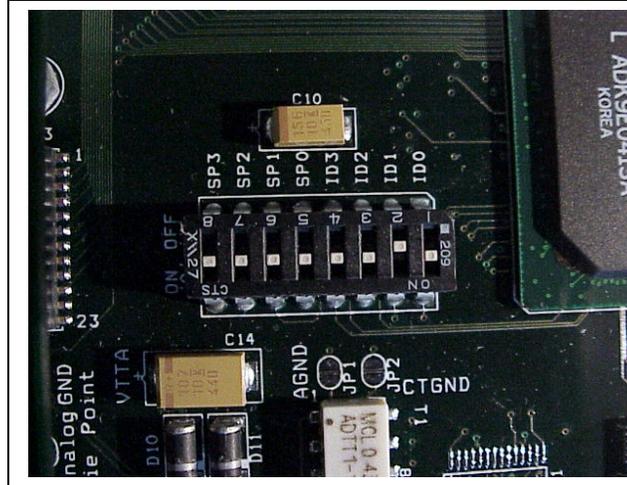
Diagnostic Signal (for Tevatron Filter card)

The TGF-II can create a diagnostic signal called Diagnostic Clock above that is distributed to the Analog Filter Boards Tevatron and can be used to test different parts of the hardware. It is not a calibration signal but is expected to be stable enough to look for long term degradation in individual channels relative to the other channels. The diagnostic signal can be set to a continuous 53Mhz wave or a short burst of 53Mhz pulses via VME writes to TGF-II offset 0x100. Some example waveforms are shown in Beams Doc #1586. From the TGF, the diagnostic signal is distributed to the Filter Boards on a User-Specified bus on the P2/J2 portion of the VME backplane. The signal is approximately 53 MHz which is near the backplane frequency capability so termination of the buss is provided on the TGF-II module and by a dedicated termination module as far away from the TGF-II as possible, usually in slot 20. This termination module was made by replacing the blank PCB portion of a commercial air-dam slot filler module with a PCB containing the necessary resistors. All of the unused slots in the installed sub racks have air-dam modules which are used to evenly distribute the cooling airflow in the sub racks.

TGF VME Base Address Selection

The VME interface section of the TGF-II is capable of 16-bit address and data transfers only. The VME base address is selectable via a four position dip switch labeled ID3 – ID0 as shown below. For the BPM project, only ID1 will be turned off and all the others will be on. This gives a base address of 0x2000 where ID3 – ID0 controls the upper 4-bits of the VME address. See Appendix "A" for a complete register map of the TGF-II module.

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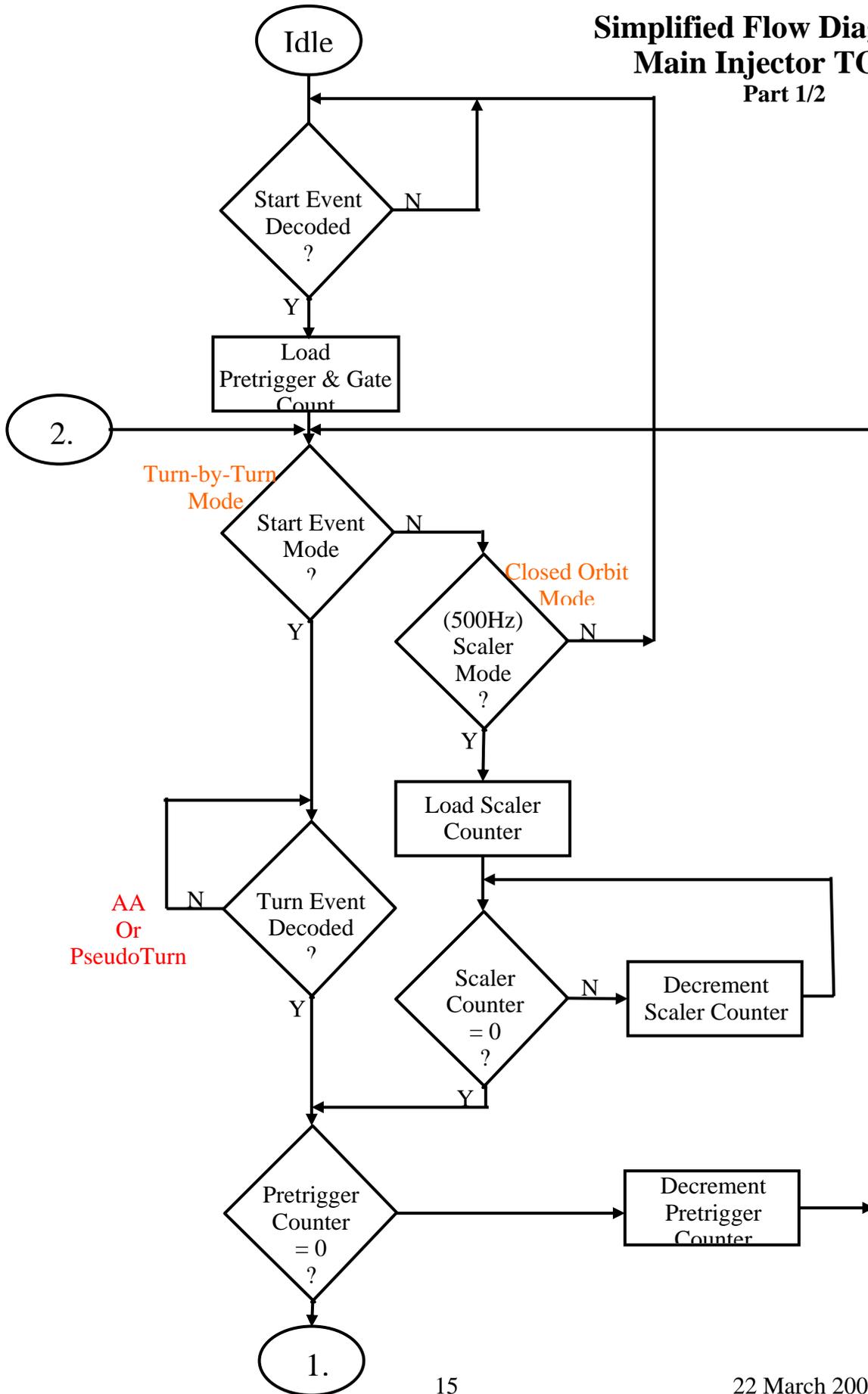


TGF-II Firmware

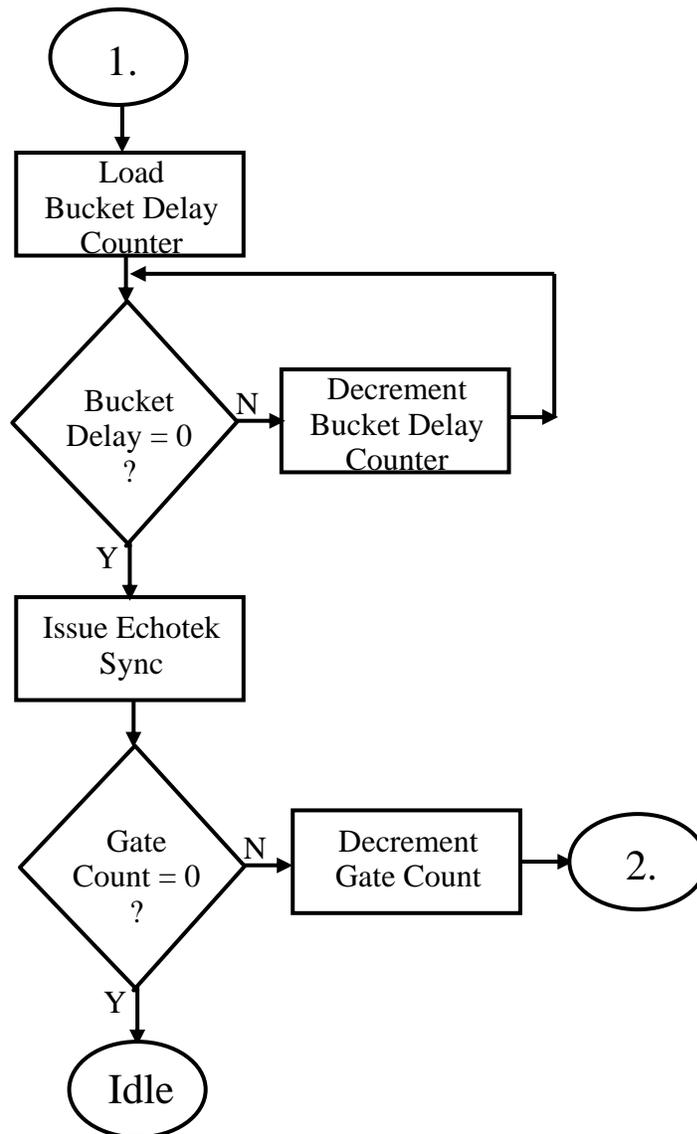
The overall TGF-II firmware will not be changeable remotely. The board will need to be directly connected to the programmer workstation or laptop to change the firmware. However the functional programmability is controlled by the registers indicated in the “TGF-II Register Map” section of this document. These resistors are accessible over the VME bus by the sub rack controller. All registers are 16 bits wide although the effective width is noted. The following simplified flow diagram demonstrates the basic operation of the TGF-II firmware.

TGF-II Flow Diagram of Main Injector

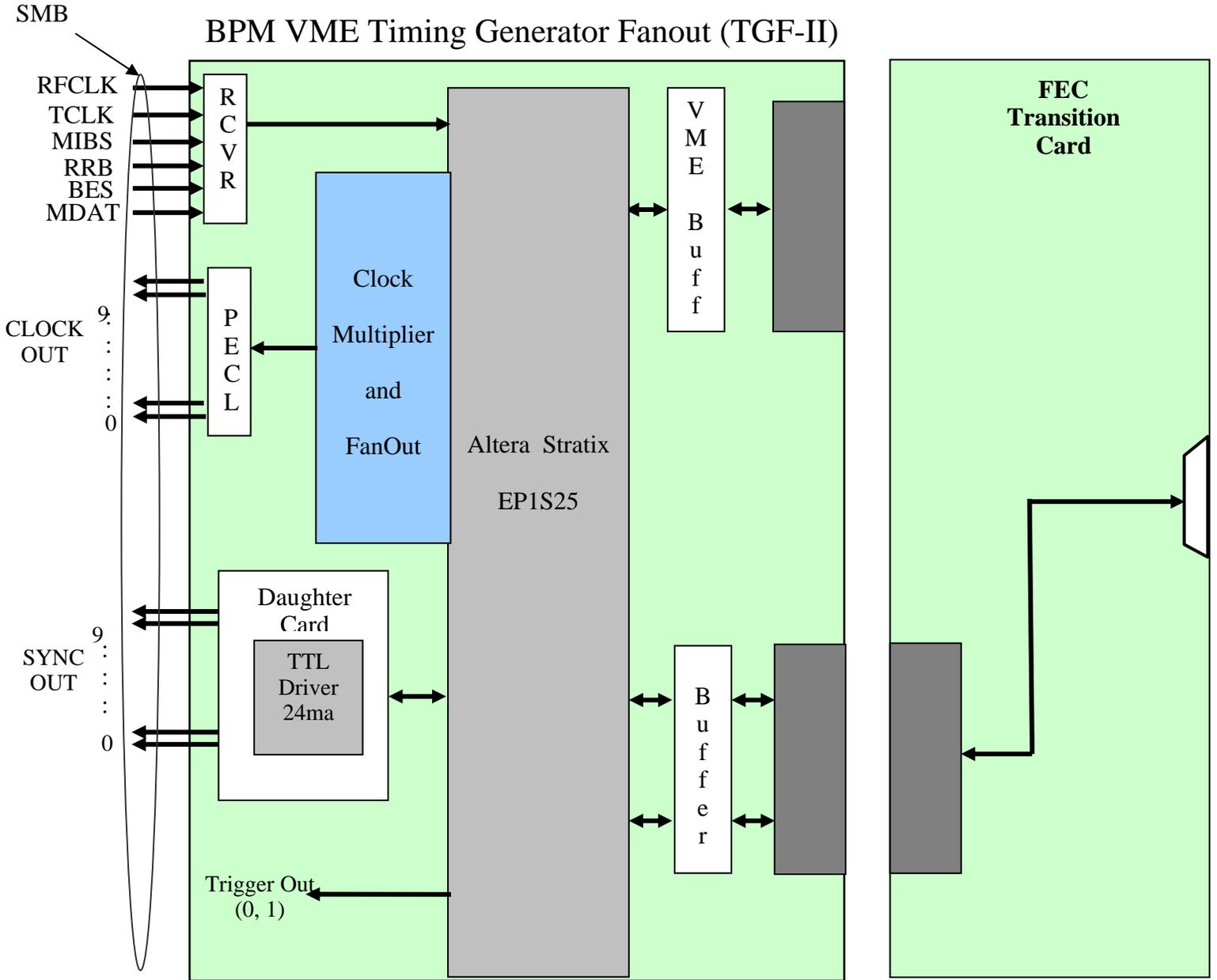
**Simplified Flow Diagram of
Main Injector TGF-II**
Part 1/2



Simplified Flow Diagram of Main Injector TGF-II Part 1/2



TGF-II Simplified Block Diagram



TGF-II Register Map (from Offset = 2000h)

Table 1	REGISTER	MAP	
I/O Address	Register Name	Effective width	
0x00	Acquisition Bucket Delay 0	12-bits	R/W
0x02	Acquisition Bucket Delay 1	12-bits	R/W
0x04	Acquisition Bucket Delay 2	12-bits	R/W
0x06	Acquisition Bucket Delay 3	12-bits	R/W
0x08	Acquisition Bucket Delay 4	12-bits	R/W
0x0A	Acquisition Bucket Delay 5	12-bits	R/W
0x0C	Acquisition Bucket Delay 6	12-bits	R/W
0x0E	Acquisition Bucket Delay 7	12-bits	R/W
0x10	Gate Count 0	16-bits	R/W
0x12	Gate Count 1	16-bits	R/W
0x14	Gate Count 2	16-bits	R/W
0x16	Gate Count 3	16-bits	R/W
0x18	Gate Count 4	16-bits	R/W
0x1A	Gate Count 5	16-bits	R/W
0x1C	Gate Count 6	16-bits	R/W
0x1E	Gate Count 7	16-bits	R/W
0x20	Mdat Type Matched (Last)	8-bits	R
0x22	Mdat Value Matched (Last)	16-bits	R
0x24	Mdat Type Event (interrupt)	8-bits	R/W
0x26	Turn Scaler for Background	16-bits	R/W
0x28	Diagnostics Counter	16-bits	Read Only
0x2A	Diagnostic Counter w/ wait		Wait on read
0x2C			
0x2E	Pre-Trigger Delay All	16-bits	R/W
0x30	Control	See Table 5	R/W
0x32	Status_Register0	See Table 6	Read Only
0x34	BSync Turn Event	8-bits	R/W
0x36	BSync Start Event	See Table 10	R/W
0x38	BSync Clear Timestamp Event	See Table 10	R/W
0x3A	First Turn Timestamp (Wrd0)	Quad Word	Read Only
0x3C	First Turn Timestamp (Wrd1)	Quad Word	Read Only
0x3E	First Turn Timestamp (Wrd2)	Quad Word	Read Only
0x40	First Turn Timestamp (Wrd3)	Quad Word	Read Only
0x42	FirstTurnsCount (Low)	Low+High=32	Read Only
0x44	FirstTurnsCount (High)	Low+High=32	Read Only
0x46	LastTurnsCount (Low)	Low+High=32	Read Only
0x48	LastTurnsCount (High)	Low+High=32	Read Only
0x4A	MissingTurnsCount (Low)	Low+High=32	Read Only

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0x4C	MissingTurnsCount (High)	Low+High=32	Read Only
0x4E	# of ADCSync0Count Low	Low+High=32	Read Only
0x50	# of ADCSync0Count High	Low+High=32	Read Only
0x52	Turns Counter Low	Low+High=32	Read Only
0x54	Turns Counter High	Low+High=32	Read Only
0x56	BSync TimeStamp Event	See Table 10	R/W
0x58	BSync TimeStamp Wrđ0	Quad Word	Read Only
0x5A	BSync TimeStamp Wrđ1	Quad Word	Read Only
0x5C	BSync TimeStamp Wrđ2	Quad Word	Read Only
0x5E	BSync TimeStamp Wrđ3	Quad Word	Read Only
0x60	Irq Vector Reg 1	See Figure 6	R/W
0x62	Irq Vector Reg 2	See Figure 6	R/W
0x64	Last Interrupted TClk Event	8-bits	Read Only
0x66	TClk IRQ #Words Pending	8-bits	
0x68	Switch	16-bits	Read Only
0x6A	Start Event Counter	Note 1	Read Only
0x70	IRQ1 Source Mux	See Table 3.	R/W
0x72	IRQ2 Source Mux	See Table 3.	R/W
0x74	TClk TimeStamp Event	8-bits	R/W
0x76	TClk TimeStamp Wrđ0	Quad Word	Read Only
0x78	TClk TimeStamp Wrđ1	Quad Word	Read Only
0x7A	TClk TimeStamp Wrđ2	Quad Word	Read Only
0x7C	TClk TimeStamp Wrđ3	Quad Word	Read Only
0x7E	Status_Register1	16-bits	Read Only
0x80	TClk Event0	See Table 9.	R/W
0x82	TClk Event1	See Table 9.	R/W
0x84	TClk Event2	See Table 9.	R/W
0x86	TClk Event3	See Table 9.	R/W
0x88	TClk Event4	See Table 9.	R/W
0x8A	TClk Event5	See Table 9.	R/W
0x8C	TClk Event6	See Table 9.	R/W
0x8E	TClk Event7	See Table 9.	R/W
0x90	TClk Event8	See Table 9.	R/W
0x92	TClk Event9	See Table 9.	R/W
0x94	TClk Event10	See Table 9.	R/W
0x96	TClk Event11	See Table 9.	R/W
0x98	TClk Event12	See Table 9.	R/W
0x9A	TClk Event13	See Table 9.	R/W
0x9C	TClk Event14	See Table 9.	R/W
0x9E	TClk Event15	See Table 9.	R/W

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0xA0	BSync_P_Event(00_0F) Found	16-bits	R/W
0xA2	BSync_P_Event(10_1F) Found	16-bits	R/W
0xA4	BSync_P_Event(20_2F) Found	16-bits	R/W
0xA6	BSync_P_Event(30_3F) Found	16-bits	R/W
0xA8	BSync_P_Event(40_4F) Found	16-bits	R/W
0xAA	BSync_P_Event(50_5F) Found	16-bits	R/W
0xAC	BSync_P_Event(60_6F) Found	16-bits	R/W
0xAE	BSync_P_Event(70_7F) Found	16-bits	R/W
0xB0	BSync_P_Event(80_8F) Found	16-bits	R/W
0xB2	BSync_P_Event(90_9F) Found	16-bits	R/W
0xB4	BSync_P_Event(A0_AF) Found	16-bits	R/W
0xB6	BSync_P_Event(B0_BF) Found	16-bits	R/W
0xB8	BSync_P_Event(C0_CF) Found	16-bits	R/W
0xBA	BSync_P_Event(D0_DF) Found	16-bits	R/W
0xBC	BSync_P_Event(E0_EF) Found	16-bits	R/W
0xBE	BSync_P_Event(F0_FF) Found	16-bits	R/W
		16-bits	
0xC0	TClkEvent(00_0F) Found	16-bits	R/W
0xC2	TClkEvent (10_1F) Found	16-bits	R/W
0xC4	TClkEvent (20_2F) Found	16-bits	R/W
0xC6	TClkEvent (30_3F) Found	16-bits	R/W
0xC8	TClkEvent (40_4F) Found	16-bits	R/W
0xCA	TClkEvent (50_5F) Found	16-bits	R/W
0xCC	TClkEvent (60_6F) Found	16-bits	R/W
0xCE	TClkEvent (70_7F) Found	16-bits	R/W
0xD0	TClkEvent (80_8F) Found	16-bits	R/W
0xD2	TClkEvent (90_9F) Found	16-bits	R/W
0xD4	TClkEvent (A0_AF) Found	16-bits	R/W
0xD6	TClkEvent (B0_BF) Found	16-bits	R/W
0xD8	TClkEvent (C0_CF) Found	16-bits	R/W
0xDA	TClkEvent (D0_DF) Found	16-bits	R/W
0xDC	TClkEvent (E0_EF) Found	16-bits	R/W
0xDE	TClkEvent (F0_FF) Found	16-bits	R/W
0xE0	MdatEvent(00_0F) Found	16-bits	R/W
0xE2	MdatEvent (10_1F) Found	16-bits	R/W
0xE4	MdatEvent (20_2F) Found	16-bits	R/W
0xE6	MdatEvent (30_3F) Found	16-bits	R/W
0xE8	MdatEvent (40_4F) Found	16-bits	R/W
0xEA	MdatEvent (50_5F) Found	16-bits	R/W
0xEC	MdatEvent (60_6F) Found	16-bits	R/W
0xEE	MdatEvent (70_7F) Found	16-bits	R/W
0xF0	MdatEvent (80_8F) Found	16-bits	R/W
0xF2	MdatEvent (90_9F) Found	16-bits	R/W
0xF4	MdatEvent (A0_AF) Found	16-bits	R/W

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0xF6	MdatEvent (B0_BF) Found	16-bits	R/W
0xF8	MdatEvent (C0_CF) Found	16-bits	R/W
0xFA	MdatEvent (D0_DF) Found	16-bits	R/W
0xFC	MdatEvent (E0_EF) Found	16-bits	R/W
0xFE	MdatEvent (F0_FF) Found	16-bits	R/W
0X100	Filter Card Control Register	See Table 7	R/W
0X102	Relay Data, Card 0	See Table 8	R/W
0X104	Relay Data, Card 1	See Table 8	R/W
0X106	Relay Data, Card 2	See Table 8	R/W
0X108	Relay Data, Card 3	See Table 8	R/W
0X10A	Relay Data, Card 4	See Table 8	R/W
0X10C	Relay Data, Card 5	See Table 8	R/W
0X10E	Relay Data, Card 6	See Table 8	R/W
0X110	Relay Data, Card 7	See Table 8	R/W
0x112	FEC_Control_0	16-bits	R/W
0x114	FEC_Control_1	16-bits	R/W
0x116	FEC_Dignostic Signal Control	See Table 11.	R/W
0x120	BSync_S_Event(00_0F) Found	16-bits	R/W
0x122	BSync_S_Event(10_1F) Found	16-bits	R/W
0x124	BSync_S_Event(20_2F) Found	16-bits	R/W
0x126	BSync_S_Event(30_3F) Found	16-bits	R/W
0x128	BSync_S_Event(40_4F) Found	16-bits	R/W
0x12A	BSync_S_Event(50_5F) Found	16-bits	R/W
0x12C	BSync_S_Event(60_6F) Found	16-bits	R/W
0x12E	BSync_S_Event(70_7F) Found	16-bits	R/W
0x130	BSync_S_Event(80_8F) Found	16-bits	R/W
0x132	BSync_S_Event(90_9F) Found	16-bits	R/W
0x134	BSync_S_Event(A0_AF) Found	16-bits	R/W
0x136	BSync_S_Event(B0_BF) Found	16-bits	R/W
0x138	BSync_S_Event(C0_CF) Found	16-bits	R/W
0x13A	BSync_S_Event(D0_DF) Found	16-bits	R/W
0x13C	BSync_S_Event(E0_EF) Found	16-bits	R/W
0x13E	BSync_S_Event(F0_FF) Found	16-bits	R/W
0x200	Acquisition Bucket Delay 0	12-bits	R/W
0x202	Acquisition Bucket Delay 1	12-bits	R/W
0x204	Acquisition Bucket Delay 2	12-bits	R/W
0x206	Acquisition Bucket Delay 3	12-bits	R/W
0x208	Acquisition Bucket Delay 4	12-bits	R/W
0x20A	Acquisition Bucket Delay 5	12-bits	R/W
0x20C	Acquisition Bucket Delay 6	12-bits	R/W
0x20E	Acquisition Bucket Delay 7	12-bits	R/W
0x210	Acquisition Bucket Delay 8	12-bits	R/W
0x212	Acquisition Bucket Delay 9	12-bits	R/W

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0x220	Gate Count 0	16-bits	R/W
0x222	Gate Count 1	16-bits	R/W
0x224	Gate Count 2	16-bits	R/W
0x226	Gate Count 3	16-bits	R/W
0x228	Gate Count 4	16-bits	R/W
0x22A	Gate Count 5	16-bits	R/W
0x22C	Gate Count 6	16-bits	R/W
0x22E	Gate Count 7	16-bits	R/W
0x230	Gate Count 8	16-bits	R/W
0x232	Gate Count 9	16-bits	R/W
0x240	Irq Vector Reg 1	See Figure 6	R/W
0x242	Irq Vector Reg 2	See Figure 6	R/W
0x244	Irq Vector Reg 3	See Figure 6	R/W
0x246	Irq Vector Reg 4	See Figure 6	R/W
0x248	Irq Vector Reg 5	See Figure 6	R/W
0x24A	Irq Vector Reg 6	See Figure 6	R/W
0x24C	Irq Vector Reg 7	See Figure 6	R/W
0x24E	Irq Vector Reg 8	See Figure 6	R/W
0x250	IRQ1 Source Mux	See Table 3.	R/W
0x252	IRQ2 Source Mux	See Table 3.	R/W
0x254	IRQ3 Source Mux	See Table 3.	R/W
0x256	IRQ4 Source Mux	See Table 3.	R/W
0x258	IRQ5 Source Mux	See Table 3.	R/W
0x25A	IRQ6 Source Mux	See Table 3.	R/W
0x25C	IRQ7 Source Mux	See Table 3.	R/W
0x25E	IRQ8 Source Mux	See Table 3.	R/W
0x260	TClk IRQ Timer Alarm1	Low 16-bits	R/W
0x262	TClk IRQ Timer Alarm1	High 16-bits	R/W
0x264	TClk IRQ Timer Alarm2	Low 16-bits	R/W
0x266	TClk IRQ Timer Alarm2	High 16-bits	R/W
0x268	TClk IRQ Timer Alarm3	Low 16-bits	R/W
0x26A	TClk IRQ Timer Alarm3	High 16-bits	R/W
0x26C	TClk IRQ Timer Alarm4	Low 16-bits	R/W
0x26E	TClk IRQ Timer Alarm4	High 16-bits	R/W
0x270	TClk IRQ Timer Alarm5	Low 16-bits	R/W
0x272	TClk IRQ Timer Alarm5	High 16-bits	R/W
0x274	TClk IRQ Timer Alarm6	Low 16-bits	R/W
0x276	TClk IRQ Timer Alarm6	High 16-bits	R/W
0x278	TClk IRQ Timer Alarm7	Low 16-bits	R/W
0x27A	TClk IRQ Timer Alarm7	High 16-bits	R/W
0x27C	TClk IRQ Timer Alarm8	Low 16-bits	R/W

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0x27E	TClk IRQ Timer Alarm8	High 16-bits	R/W
0x280	TClk IRQ Timer Alarm9	Low 16-bits	R/W
0x282	TClk IRQ Timer Alarm9	High 16-bits	R/W
0x284	TClk IRQ Timer Alarm10	Low 16-bits	R/W
0x286	TClk IRQ Timer Alarm10	High 16-bits	R/W
0x288	TClk IRQ Timer Alarm11	Low 16-bits	R/W
0x28A	TClk IRQ Timer Alarm11	High 16-bits	R/W
0x28C	TClk IRQ Timer Alarm12	Low 16-bits	R/W
0x28E	TClk IRQ Timer Alarm12	High 16-bits	R/W
0x290	TClk IRQ Timer Alarm13	Low 16-bits	R/W
0x292	TClk IRQ Timer Alarm13	High 16-bits	R/W
0x294	TClk IRQ Timer Alarm14	Low 16-bits	R/W
0x296	TClk IRQ Timer Alarm14	High 16-bits	R/W
0x298	TClk IRQ Timer Alarm15	Low 16-bits	R/W
0x29A	TClk IRQ Timer Alarm15	High 16-bits	R/W
0x29C	TClk IRQ Timer Alarm16	Low 16-bits	R/W
0x29E	TClk IRQ Timer Alarm16	High 16-bits	R/W
0x2A0	TClk IRQ Timer Alarm17	Low 16-bits	R/W
0x2A2	TClk IRQ Timer Alarm17	High 16-bits	R/W
0x2A4	TClk IRQ Timer Alarm18	Low 16-bits	R/W
0x2A6	TClk IRQ Timer Alarm18	High 16-bits	R/W
0x2A8	TClk IRQ Timer Alarm19	Low 16-bits	R/W
0x2AA	TClk IRQ Timer Alarm19	High 16-bits	R/W
0x2AC	TClk IRQ Timer Alarm20	Low 16-bits	R/W
0x2AE	TClk IRQ Timer Alarm20	High 16-bits	R/W
0x2B0	TClk IRQ Timer Alarm21	Low 16-bits	R/W
0x2B2	TClk IRQ Timer Alarm21	High 16-bits	R/W
0x2B4	TClk IRQ Timer Alarm22	Low 16-bits	R/W
0x2B6	TClk IRQ Timer Alarm22	High 16-bits	R/W
0x2B8	TClk IRQ Timer Alarm23	Low 16-bits	R/W
0x2BA	TClk IRQ Timer Alarm23	High 16-bits	R/W
0x2BC	TClk IRQ Timer Alarm24	Low 16-bits	R/W
0x2BE	TClk IRQ Timer Alarm24	High 16-bits	R/W
0x2C0	TClk IRQ Timer Alarm25	Low 16-bits	R/W
0x2C2	TClk IRQ Timer Alarm25	High 16-bits	R/W
0x2C4	TClk IRQ Timer Alarm26	Low 16-bits	R/W
0x2C6	TClk IRQ Timer Alarm26	High 16-bits	R/W
0x2C8	TClk IRQ Timer Alarm27	Low 16-bits	R/W
0x2CA	TClk IRQ Timer Alarm27	High 16-bits	R/W
0x2CC	TClk IRQ Timer Alarm28	Low 16-bits	R/W
0x2CE	TClk IRQ Timer Alarm28	High 16-bits	R/W
0x2D0	TClk IRQ Timer Alarm29	Low 16-bits	R/W
0x2D2	TClk IRQ Timer Alarm29	High 16-bits	R/W
0x2D4	TClk IRQ Timer Alarm30	Low 16-bits	R/W

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0x2D6	TClk IRQ Timer Alarm30	High 16-bits	R/W
0x2D8	TClk IRQ Timer Alarm31	Low 16-bits	R/W
0x2DA	TClk IRQ Timer Alarm31	High 16-bits	R/W
0x2DC	TClk IRQ Timer Alarm32	Low 16-bits	R/W
0x2DE	TClk IRQ Timer Alarm32	High 16-bits	R/W
0x2E0	Alarm Counter when IRQ Issued	Low 16-bits	R Only
0x2E2	Alarm Counter when IRQ Issued	High 16-bits	R Only
0x2E4	TClk Timer Alarm Counter	Low 16-bits	R Only
0x2E6	TClk Timer Alarm Counter	High 16-bits	R Only
	ID ROM		
0X400	x0054, “T”	8-bit	R only
0X402	x0047, “G”	8-bit	R only
0X404	x0046, “F”	8-bit	R only
0X406	x0000, “ “	8-bit	R only
0X408	x0056, “V”	8-bit	R only
0X40A	x0045, “E”	8-bit	R only
0X40C	x0052, “R”	8-bit	R only
0X40E	x0053, “S”	8-bit	R only
0X410	x0049, “I”	8-bit	R only
0X412	x004F, “O”	8-bit	R only
0X414	x004E, “N”	8-bit	R only
0X416	x0000, “ “	8-bit	R only
0X418	x0033, “3”	8-bit	R only
0X41A	x002E, “.”	8-bit	R only
0X41C	x0031, “1”	8-bit	R only
0X41E	x002E, “.”	8-bit	R only
0X420	x0032, “2”	8-bit	R only
0X422	x0020, “ “	8-bit	R only
0X500-0X6FE	Last MDat Values Stored	16-bit	R/W

Note 1 The Start Event Counter located at offset x”6A” counts the number of BSync start events (offset=x”36”). This counter is cleared on BSync Clear Timestamp Event (x”38”).

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Table 2 IRQ SOURCE MUX		I/O	Address
DATA	SOURCE	0x70...0x72	
0x00	Null		
0x01	Start Event		
0x02	Revolution Event		
0x03	MDAT Type Match		
0x04	Turn Scaler Trigger Out		
0x05	TimerAlarm		
0x06	Delay Timer Trigger		
0x07	Delay Timer Terminal Count		
0x08	Turn Counter Trigger		
0x09	Periodic timer (BGFlash rate)		
0x0A	TCIk Event Match	16-bits	R/W

INTERRUPT STATUS/ID REGISTER DETAIL (Eight instances)

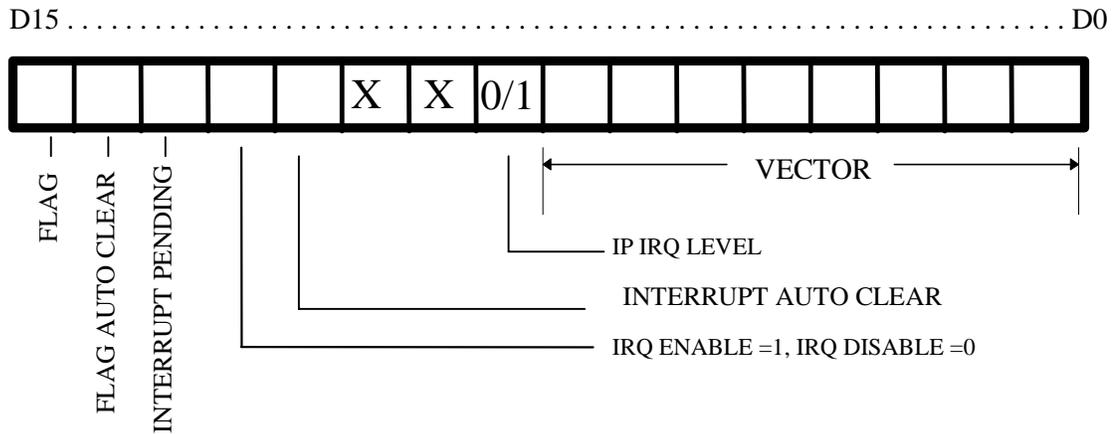


Figure 3

Table 3		CONTROL AND MODE REGISTER	I/O Address 0x30
DATA			
Low Byte			
0xXX01	Control[0]	Enable Pre-Trigger Counter	Zero = Disabled, One = Enabled
0xXX02	Control[1]	Enable Delay Timer	Zero = Disabled, One = Enabled
0xXX04	Control[2]	Reset Alarms	Zero = No action, One = Reset
0xXX08	Control[3]	Not Used	
0xXX10	Control[4]	Trigger Source	Zero = PreTrigger from turn event, One = External, Two = PreTrigger from start event
0xXX20	Control[5]	Trigger Source	
0xXX40	Control[6]	“Start” Source	Zero = Start Event, One = Null, Two = Turn Scaler (periodic)
0xXX80	Control[7]	“Start” Source	
High Byte			
0x01XX	Control[8]	Enable MDat	
0x02XX	Control[9]	Enable TClk	Zero = Disabled, One = Enabled
0x04XX	Control[10]	Enable Beam Sync1 (MI_BS)	Zero = Disabled, One = Enabled
0x08XX	Control[11]	Enable Beam Sync2 (RR_BS)	Zero = Disabled, One = Enabled
0x10XX	Control [12]	Single/Repetitive ADC Sync Out	Zero = Repetitive, One = Single
0x20XX	Control[13]	Enable Beam Extraction Sync (BES)	Zero = Disabled, One = Enabled
0x40XX	Control[14]	Reset TClk IRQ Pending	Zero = No action, One = Reset
0x80XX	Control[15]	Reset TSG	Zero = No action, One = Reset

Control Register Comments:

Control (2)

When equal to ‘1’ the TClkIrq Alarm Timer state machine will be initialized and wait for the next TClk alarm event.

Control (5:4)

When equal to “00”, the pre-trigger counter is selected as the trigger source for the gate count and bucket delay. The pre-trigger counter decrements on each turn event and when it equals zero, the bucket delay is started, when the bucket delay is decremented to zero, the ADCsync signal is issued and then the gate count is decremented on the next turn followed by another ADCSync after the bucket delay, etc until the gate count equals zero.

When equal to “01”, an external trigger input bypasses the pre-trigger counter and immediately starts the bucket delay counter, then issues the ADCsync signal, then

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decrements the gate count every 1113 buckets for the Tevatron (588 buckets for Main Injector).

When equal to “10” , a start event also bypasses the pre-trigger counter and immediately starts the bucket delay, then issues the ADCsync signal, then decrements the gate count every 1113 buckets for the Tevatron (588 buckets for Main Injector).

Control (7:6)

When equal to “00”, the Start Source is the BSync start event register (0x36) is equal the decoded BSync serial input.

When equal to “01”, No Start Source.

When equal to “10”, Start is generated when the turn scaler counter (0x26) is equal to zero. The Turn scaler counter is decremented by the decoded BSync Turn event.

Control (12)

When equal to a zero, an ADC_Sync Out pulse is generated for each event trigger (BSync event or external trigger) repetitively. When equal to a one, an ADC_Sync Out pulse is generated for the first event trigger after writing to the control register. Default is zero for repetitive mode.

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Table 4	STATUS_0 REGISTER BIT DEFINITIONS	I/O Address 0x32
DATA	DESCRIPTION	
Bit-0	Turn Marker	
Bit-1	Start Marker	
Bit-2	TClk Parity Error	
Bit-3	Mdat Parity Error	
Bit-4	BSync Parity Error	
Bit-5		
Bit-6		
Bit-7	Missing Turn Error	
Bit-8	Turn Scaler Enabled	
Bit-9	53MHz present	
Bit-10	BSync Present	
Bit_11	TClk Present	
Bit_12	Mdat Present	
Bit_13	BSync Enabled	
Bit_14	TClk Enabled	
Bit_15	Mdat Enabled	

Table 6	STATUS_1 REGISTER BIT DEFINITIONS	I/O Address 0x7E
DATA	DESCRIPTION	
Bit-0	BSync_P_Enabled	
Bit-1	BSync_S_Enabled	
Bit-2	BES Enabled	
Bit-3	Mdat Enabled	
Bit-4	TClk Enabled	
Bit-5	BSync_P_Present	
Bit-6	BSync_S_Present	
Bit-7	BES_Present	
Bit-8	Mdat_Present	
Bit-9	TClk_Present	
Bit-10	53MHz present	
Bit_11	Turn Marker	
Bit_12	Start Marker	
Bit_13	Turn Scaler Enabled	
Bit_14	Missing Turn Error	
Bit_15		

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Table 7	FilterCard Control Register BIT DEFINITIONS	I/O Address 0x100
DATA	DESCRIPTION	
Bit-0	FilterCard Start/Done Card 0	Note 1
Bit-1	FilterCard Start/Done Card 1	Note 1
Bit-2	FilterCard Start/Done Card 2	Note 1
Bit-3	FilterCard Start/Done Card 3	Note 1
Bit-4	FilterCard Start/Done Card 4	Note 1
Bit-5	FilterCard Start/Done Card 5	Note 1
Bit-6	FilterCard Start/Done Card 6	Note 1
Bit-7	FilterCard Start/Done Card 7	Note 1
Bit-8	FilterCard R/W	Note 2
Bit-9	FilterCard Enable Diagnostic Signal	
Bit-10	Diagnostic Signal Type	Note 3
Bit-11	RelayState0	
Bit-12	RelayState1	
Bit-13	RelayState2	
Bit-14		
Bit-15	FilterCard Global Reset	

Note 1: After loading relay information into the Filter Card Data Registers (0x102 – 0x110) (table 2) and setting a one in the corresponding FilterCard Start/Done 1 register bit will immediately start sending the serialized data to the appropriate Filter/Relay Card. When the transfer of data is complete the start bit will be cleared automatically by the FPGA Firmware.

Note 2: The FilterCard R/W bit (Bit-8) is currently write capable only and read capability will be implemented in the future. Default is zero for writes to Filter Card.

Note 3: The Diagnostic Signal Type can be set to a continuous 53MHz clock when set to a logic zero or a 53 MHz clock pulse train of seven pulses triggered from the BSync turn event when set to a logic one. Default is a continuous 53MHz clock.

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Table 8		FilterCard Data Register			
Ch #	MSB	Data	LSB	Source	Destination
1	xx xx xx xx xx xx xx	00		BPM	Digitizer
1	xx xx xx xx xx xx xx	01		Diagnostic	BPM
1	xx xx xx xx xx xx xx	10		Diagnostic	BPM & Digitizer
1	xx xx xx xx xx xx xx	11		Diagnostic	Digitizer
2	xx xx xx xx xx xx xx	00 xx		BPM	Digitizer
2	xx xx xx xx xx xx xx	01 xx		Diagnostic	BPM
2	xx xx xx xx xx xx xx	10 xx		Diagnostic	BPM & Digitizer
2	xx xx xx xx xx xx xx	11 xx		Diagnostic	Digitizer
3	xx xx xx xx xx xx xx	00 xx xx		BPM	Digitizer
3	xx xx xx xx xx xx xx	01 xx xx		Diagnostic	BPM
3	xx xx xx xx xx xx xx	10 xx xx		Diagnostic	BPM & Digitizer
3	xx xx xx xx xx xx xx	11 xx xx		Diagnostic	Digitizer
4	xx xx xx xx xx xx xx	00 xx xx xx		BPM	Digitizer
4	xx xx xx xx xx xx xx	01 xx xx xx		Diagnostic	BPM
4	xx xx xx xx xx xx xx	10 xx xx xx		Diagnostic	BPM & Digitizer
4	xx xx xx xx xx xx xx	11 xx xx xx		Diagnostic	Digitizer
5	xx xx xx xx xx xx xx	00 xx xx xx xx		BPM	Digitizer
5	xx xx xx xx xx xx xx	01 xx xx xx xx		Diagnostic	BPM
5	xx xx xx xx xx xx xx	10 xx xx xx xx		Diagnostic	BPM & Digitizer
5	xx xx xx xx xx xx xx	11 xx xx xx xx		Diagnostic	Digitizer
6	xx xx xx xx xx xx xx	00 xx xx xx xx xx		BPM	Digitizer
6	xx xx xx xx xx xx xx	01 xx xx xx xx xx		Diagnostic	BPM
6	xx xx xx xx xx xx xx	10 xx xx xx xx xx		Diagnostic	BPM & Digitizer
6	xx xx xx xx xx xx xx	11 xx xx xx xx xx		Diagnostic	Digitizer
7	xx xx xx xx xx xx xx	00 xx xx xx xx xx xx		BPM	Digitizer
7	xx xx xx xx xx xx xx	01 xx xx xx xx xx xx		Diagnostic	BPM
7	xx xx xx xx xx xx xx	10 xx xx xx xx xx xx		Diagnostic	BPM & Digitizer
7	xx xx xx xx xx xx xx	11 xx xx xx xx xx xx		Diagnostic	Digitizer
8	xx xx xx xx xx xx xx	00 xx xx xx xx xx xx		BPM	Digitizer
8	xx xx xx xx xx xx xx	01 xx xx xx xx xx xx		Diagnostic	BPM
8	xx xx xx xx xx xx xx	10 xx xx xx xx xx xx		Diagnostic	BPM & Digitizer
8	xx xx xx xx xx xx xx	11 xx xx xx xx xx xx		Diagnostic	Digitizer

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Table 9	TClk Event Register BIT DEFINITIONS	I/O Address 0x80-0x9E
DATA	DESCRIPTION	
Bit-0	TClk Event bit 0	
Bit-1	TClk Event bit 1	
Bit-2	TClk Event bit 2	
Bit-3	TClk Event bit 3	
Bit-4	TClk Event bit 4	
Bit-5	TClk Event bit 5	
Bit-6	TClk Event bit 6	
Bit-7	TClk Event bit 7	
Bit-8	One = UseAlarm Seq , Zero = No Alarm Seq	Note 1
Bit-9		
Bit-10		
Bit-11		
Bit-12		
Bit-13		
Bit-14		
Bit-15		

Notes: 1) When set to a logic one and the TClk event occurs, start Timer Alarm and generate a VME interrupt to load the Timer Alarm sequence. When Timer Alarm1 times-out a VME interrupt will be generated, followed by Timer Alarm2, Timer Alarm3, etc until the next Timer Alarm value is zero or the Timer Alarm16 has timed-out. Values loaded into the Timer Alarm registers are elapsed time between alarms not total time.

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Table 10	Event Register BIT DEFINITIONS	I/O Address 0x34, 0x36, 0x56
DATA	DESCRIPTION	
Bit-0	Event bit 0	
Bit-1	Event bit 1	
Bit-2	Event bit 2	
Bit-3	Event bit 3	
Bit-4	Event bit 4	
Bit-5	Event bit 5	
Bit-6	Event bit 6	
Bit-7	Event bit 7	
Bit-8	Sync_Sel0	Note 1
Bit-9	Sync_Sel1	Note 1
Bit-10		
Bit-11		
Bit-12		
Bit-13		
Bit-14		
Bit-15		

Notes: 1) When SyncSel = “00” then BSync_P_Event is selected, when SyncSel = “01” then BSync_S_Event is selected and when SyncSel = “10” then BES event is selected.

Table 11	Event Register BIT DEFINITIONS	I/O Address 0x112
DATA	DESCRIPTION	
Bit-0	FEC_Data0	
Bit-1	FEC_Data1	
Bit-2	FEC_Data2	
Bit-3	FEC_Data3	
Bit-4	FEC_Data4	
Bit-5	FEC_Data5	
Bit-6	FEC_Data6	
Bit-7	FEC_Data7	
Bit-8	FEC_Data8	
Bit-9	FEC_Data9	
Bit-10	FEC_Data10	
Bit-11	FEC_Data11	
Bit-12	FEC_Data12	
Bit-13	FEC_Data13	
Bit-14	FEC_Data14	
Bit-15	FEC_Data15	

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Table 12	Event Register BIT DEFINITIONS	I/O Address 0x114
DATA	DESCRIPTION	
Bit-0	FEC_Address(0)	
Bit-1	FEC_Address(1)	
Bit-2	Spare(0)	
Bit-3	Spare(1)	
Bit-4	Spare(2)	
Bit-5	Spare(3)	
Bit-6	Spare(4)	
Bit-7	Spare(5)	
Bit-8	Spare(6)	
Bit-9	Spare(7)	
Bit-10	Spare(8)	
Bit-11	Spare(9)	
Bit-12	Read/Write, Read = '1', Write = '0'	
Bit-13	Not Used	
Bit-14	Not Used	
Bit-15	Not Used	

Table 13	Event Register BIT DEFINITIONS	I/O Address 0x116
DATA	DESCRIPTION	
Bit-0	Diagnostic Signal ½ Bucket Delay bit 0	
Bit-1	Diagnostic Signal ½ Bucket Delay bit 1	
Bit-2	Diagnostic Signal ½ Bucket Delay bit 2	
Bit-3	Diagnostic Signal ½ Bucket Delay bit 3	
Bit-4	Diagnostic Signal ½ Bucket Delay bit 4	
Bit-5	Diagnostic Signal ½ Bucket Delay bit 5	
Bit-6	Diagnostic Signal ½ Bucket Delay bit 6	
Bit-7	Diagnostic Signal ½ Bucket Delay bit 7	
Bit-8	Diagnostic Signal ½ Bucket Delay bit 8	
Bit-9	Diagnostic Signal ½ Bucket Delay bit 9	
Bit-10	Diagnostic Signal ½ Bucket Delay bit 10	
Bit-11	Diagnostic Signal ½ Bucket Delay bit 11	
Bit-12	Enable FEC Diagnostic Signal	
Bit-13	FEC type Diagnostic Signal= PulseTrain/Continuous	
Bit-14	Freq of Diagnostic Signal, 53Mhz = '0', 2.5Mhz='1'	
Bit-15		

- Notes:**
- 1) Diagnostic signal delay is used to generate the diagnostic signal delayed from the decoded BSync start event.
 - 2) The FEC diagnostic signal type is selected to a continuous (53Mhz/2.5Mhz) signal when bit-13 = '0' and a (53Mhz/2.5Mhz) pulse train of 84-pulses when bit-13 = '1'.

Main Injector BPM Hardware Specifications

- 3) The frequency of the diagnostic signal is 53Mhz when bit-14 = '1' and 2.5Mhz when '0'.

TGF-II Schematics, Layouts and drawings

Schematic: Beams Document #

Layout: Beams Document #

Bill of Materials: Beams Document #

Sub Rack

The sub rack is a standard 6U VME64 by Dawn VME Products Corp, see Sub rack Specifications. The 800 watt power supply is built in and provides VME64 standard voltages and the crate has complete fan cooling. There is a crate monitoring micro controller that can report voltages, temperatures and fan speeds. It has minimum control over the power supply such that it can turn the outputs on and off and it can reset the VME bus. It has a serial port and connects to the Accelerator Ethernet network through an Optilogic module that is also used on systems in the Tevatron.

Sub Rack Processor Module

The sub rack controller CPU board is responsible for establishing the communication link between user applications and the Echotek modules. All control and data transferred to/from the BPM modules pass through the sub rack controller.

The processor chosen for the Main Injector BPM system is a Motorola MVME5500 with 512MB of on-board memory. The processor will run the VxWorks embedded operating system which is widely used throughout the lab. The ESS department in the Computing Division has a [MVME 5500 data sheet](#) on its web site. Operation of the TeV BPM DAQ software is described in Beams doc #1949, *Main Injector Beam Position Upgrade Software Specification for Data Acquisition*.

Sub Rack Cables

Interconnection cables are an important facet of this upgrade. The signal cables moving sensor outputs around the electronics must not distort, attenuate or add noise to the signals of interest. Also the signals from the two outputs of each side of a sensor must travel through cables that have the signal delay matched to better than 50 picoseconds. This is approximately one degree of phase shift at 53 MHz. The timing cables also have a similar delay matching specification so that clock and gate delays within a sub rack are uniform. The chosen default cable is double-shielded RG-400. The short jumpers between the TGF-II and the Echotek DSR are RG-316 because of their flexibility requirement. The Cable Specifications are Beams Document #1257.

The connectors chosen for the cables are a mixture of SMA and SMB style connectors which have excellent signal characteristics at 53 MHz. Connections to existing systems use the SMA style. Where the connectors are too close together, the SMB style connectors are used because they snap on and off rather than requiring a nut to be tightened.

Main Injector BPM Hardware Specifications

Cable Specifications

Beams Document #

Sub rack Specifications

Beams Document #

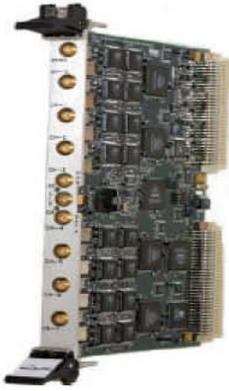
Echotek DSR Module

Data Sheet attached.



**EIGHT CHANNEL
ANALOG TO DIGITAL CONVERTER
WITH DIGITAL RECEIVER**

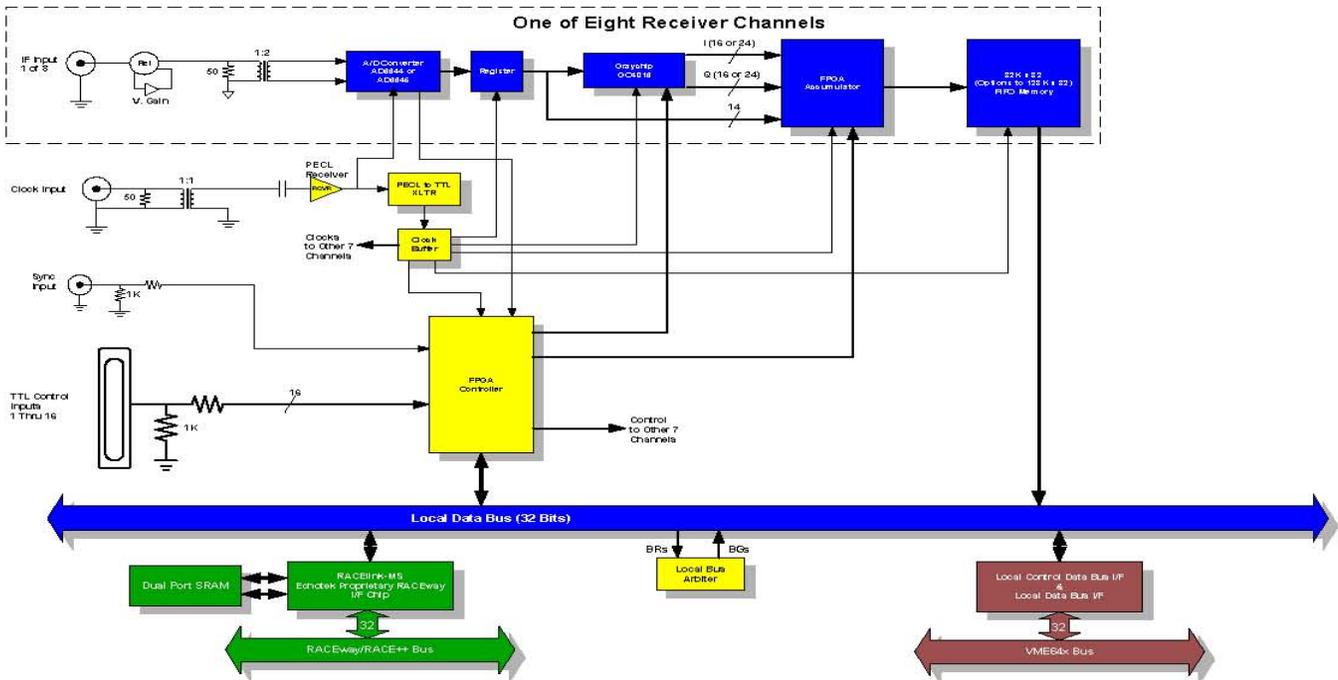
ECDR-GC814



FEATURES

- * 8 IF INPUTS
- * SIMULTANEOUS SAMPLING
- * EIGHT ANALOG TO DIGITAL CONVERTERS (ANALOG DEVICES AD6644, 14 BIT, 65 MSPS, OR AD6645 FOR SAMPLING RATES TO 105 MHz)
- * SFDR > 90 dB FS
- * 8 RECEIVER CHANNELS (GRAYCHIP GC4016)
- * DECIMATION RANGE 8-16K/CHANNEL
- * HEADER INSERTION
- * VME 64X, SINGLE SLOT
- * RACE++™ OUTPUT
- * ALSO AVAILABLE AS TWO OR FOUR CHANNEL MODEL
- * AVAILABLE AS A/D CONVERTER ONLY AS AN 8, 4, OR 2 CHANNEL MODULE
- * VARIABLE GAIN (~ -10 TO +20 dB)

ECDR-GC814 BLOCK DIAGRAM



Main Injector BPM Hardware Specifications

ECHOTEK CORPORATION 555 SPARKMAN DRIVE #400 HUNTSVILLE, AL
35816 PHONE 256 721 1911 FAX 256 721 9266 E-MAIL: sales@echotek.com
ECCR-GC814

This analog to digital converter and digital drop receiver board provides eight channels of 14 bit, 105 MHz analog to digital conversion and digital processing suitable for wideband and narrowband down conversion and filtering in a single 6U VME slot. Data decimation range of each receiver channel is user programmable from 8 to 16384. The receiver section of each channel may be bypassed to output raw A/D data.

Data Inputs

Up to eight analog signals may be input to this board via front panel SMA connectors. Each signal is converted using Analog Devices AD6644, 14 bit, 65 MHz A/D converters or AD6645 for sampling rates to 105 MHz. Direct digitization for IF's > 200 MHz are supported. These high quality analog to digital converters exhibit Spur Free Dynamic Ranges in excess of 90 dB FS.

Clocks

The A/D clock is provided by the user via front panel SMA connector. This clock signal (sine wave into 50 ohms) is buffered and distributed to all eight channels so that all channels are sampled simultaneously.

Other Inputs

The user may also input a sync signal through the front panel and up to 16 bit wide digital word - normally used to insert a header into the data stream or for tagging data.

Receiver Channels

The digitizer outputs from each A/D converter interfaces to the input crossbar switch on the Graychip GC4016 multi-standard quad digital down converter chip. A receiver channel block diagram is shown below for clarity - the Graychip GC4016 contains four such channels that can be combined as mentioned below, only one Graychip 4016 channel or channel combination is output per receiver channel on the ECCR-GC814.

The ECCR-GC814 supports the various channel combination configurations allowed by the Graychip 4016, that is: Sample Accumulator:

A	No channels combined. In this mode, each channel supports decimations from 32 to 16384.
B	Channel pair combinations supports decimations of 16 to 8192 while in this mode
C	Four channel combination resulting in one wideband output channel:
	- supports decimations of 8 to 4096 while in this mode.

The output of the receivers or the A/D converter (in receiver bypass mode) is directed to an FPGA that outputs the sum of a programmed number of samples. The output may be the sum of 1, 2, 4, 8, 16, 32, 64, 128, or 256 raw A/D samples or I's or Q's.

FIFO Buffer

Main Injector BPM Hardware Specifications

Data is output from the sample accumulator to each channel's FIFO buffer. The FIFO buffer is 16K x 32 bits (by default) and may be configured at the factory as large as 128K x 32 bits.

Data Output

Data, raw A/D output, complex receiver data, or either of the quadrature components, is output via the RACE++ interface. The data may also be output via the VME64X interface - but this interface was designed to be used for control in real time and, therefore, is not optimized for high speed data transfer.

Operating Modes

The ECDR-814 supports both CW and pulsed system applications. The board may be controlled in one of two basic operating modes:

Gate Mode - Data acquisition occurs when the gate signal is active. The gate signal may be provided via external front panel input or a software write.

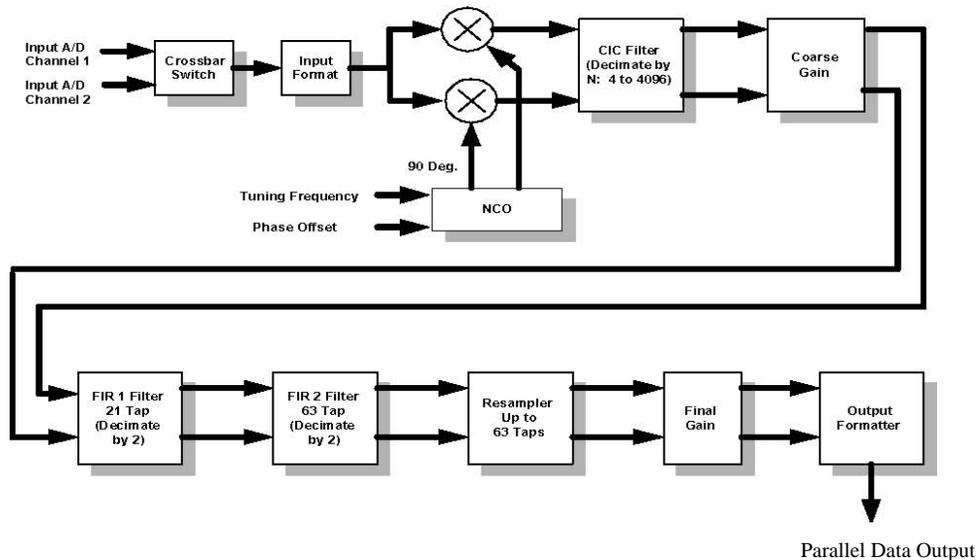
Counted Burst - A preprogrammed number of samples are acquired and processed with each occurrence of an external trigger pulse. This trigger pulse also has a software bit counterpart associated with it.

Set-Up and Control

All set-up and control registers are accessible via the VME interface. Additionally, the RACE++ interface may be programmed by either VME or RACE++ and can be a RACE++ master or slave.

Driver Support

Drivers are supplied for VxWorks Operating Systems.



Ordering Information

Model	Part Number	Ruggedization	Options
ECDR-GC814/8	12-0050/CC334A	Commercial	65 MHz A/D, 16K FIFO
ECDR-GC814/8	12-0050/CC335	Commercial	65 MHz A/D, 128K FIFO
ECDR-GC814/8-80	12-0050/CC450	Commercial	80 MHz A/D, 16K FIFO
ECDR-GC814/8-80	12-0050/CC512	Commercial	80 MHz A/D, 128K FIFO
ECDR-GC814/8-105	12-0050/CC495	Commercial	105 MHz A/D, 16K FIFO
ECDR-GC814/8-105	12-0050/CC496	Commercial	105 MHz A/D, 128K FIFO
ECDR-GC814/4	12-0057/CC339	Commercial	65 MHz A/D, 16K FIFO
ECDR-GC814/4	12-0057/CC337	Commercial	65 MHz A/D, 128K FIFO
ECDR-GC814/4-80	12-0057/CC494	Commercial	80 MHz A/D, 16K FIFO
ECDR-GC814/4-80	12-0057/CC451	Commercial	80 MHz A/D, 128K FIFO
ECDR-GC814/4-105	12-0057/CC477	Commercial	105 MHz A/D, 16K FIFO
ECDR-GC814/4-105	12-0057/CC497	Commercial	105 MHz A/D, 128K FIFO
ECDR-GC814/2	12-0058/CC350	Commercial	65 MHz A/D, 16K FIFO
ECDR-GC814/2	12-0058/CC498	Commercial	65 MHz A/D, 128K FIFO
ECDR-GC814/2-80	12-0058/CC420	Commercial	80 MHz A/D, 16K FIFO
ECDR-GC814/2-80	12-0058/CC340	Commercial	80 MHz A/D, 128K FIFO
ECDR-GC814/2-105	12-0058/CC499	Commercial	105 MHz A/D, 16K FIFO
ECDR-GC814/2-105	12-0058/CC500	Commercial	105 MHz A/D, 128K FIFO
LED OPTION:			
ECDR-GC814/8-DC	12-0107/CC426	Commercial	65 MHz A/D, 16K FIFO
ECDR-GC814/8-DC	12-0107/CC431	Commercial	65 MHz A/D, 128K FIFO

