

# Comparing the Dark Current Kicker and the ILC Damping Ring Kicker Specifications

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# The Specifications

	Rise Time	Width	Peak Voltage	Voltage Jitter	Repetition Rate
Dark Current Kicker	> 1ns	> 10 ns	+/- 3kV	0.1%	3MHz @ 5Hz
Damping Ring Kicker	~1ns	< 10 ns	+/- 10kV	~0.3%	3MHz @ 15kHz

FID Technologies Pulser meets most of the dark current kicker requirements except for jitter. Cost is > \$100k.

Mark Palmer's +/- 1kV version \$67k.  
+/- 10kV version \$250k

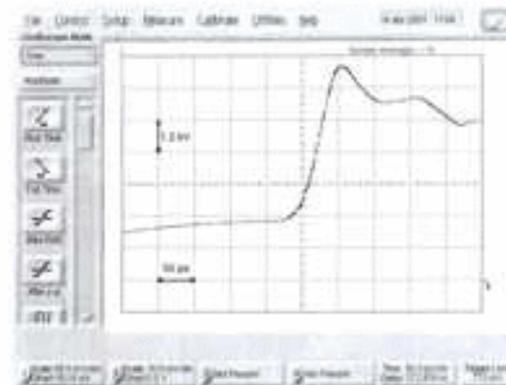
Reliability?

## Ultrafast Pulsers

Up to the recent time it was impossible to form the voltage pulses with a rise time of tens of picoseconds and the amplitude higher than several dozens of volts. The pulsers based on the ultrafast FIDs broke this limit.

The figure below shows the output voltage of the pulser FPG10SP. The snapshot was taken using the Agilent 86100A oscilloscope with the 50 GHz bandwidth. (26 GHz attenuator by Barth Electronics has been used during the measurements).

FPG10SP	
Output voltage at 50 Ohm	5 kV
Rise time	< 50 ps
Pulse width	0.1 - 10 ns
Maximum pulse repetition frequency	10 kHz
Timing jitter	< 20ps
Triggering	5 V, 100 ns
Power supply	100 - 300 V, DC
Dimensions	100x60x40 mm



[Click here to enlarge](#)

# Kicker Design

- Many labs looking into kicker design:
  - SLAC (Krasnykh), ATF (Stefano), Frascati, KEK.
- Known difficulties:
  - Feedthru's unreliable at these voltages.
  - Bandwidth  $\sim$  1GHz.

# What do we want to do?

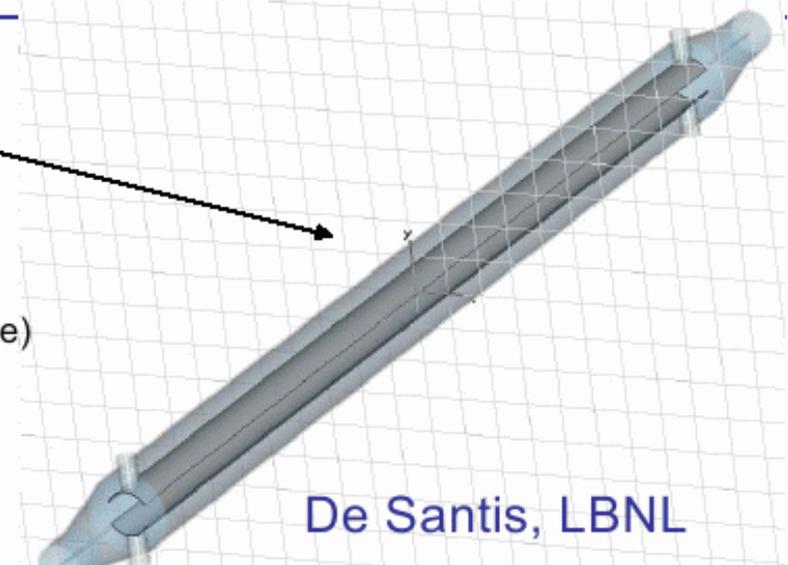
- Build a “Damping Ring Kicker” test kicker at NML?
  - Build a kicker that is capable of taking +/- 10kV peak and 1GHz bw.
  - Modify a design from one/all of the labs.
    - Length is about right 30cm.
- Concentrate on building a prototype kicker on the bench rather than the pulser.
  - Test and install at NML. **Build it and they will come?**



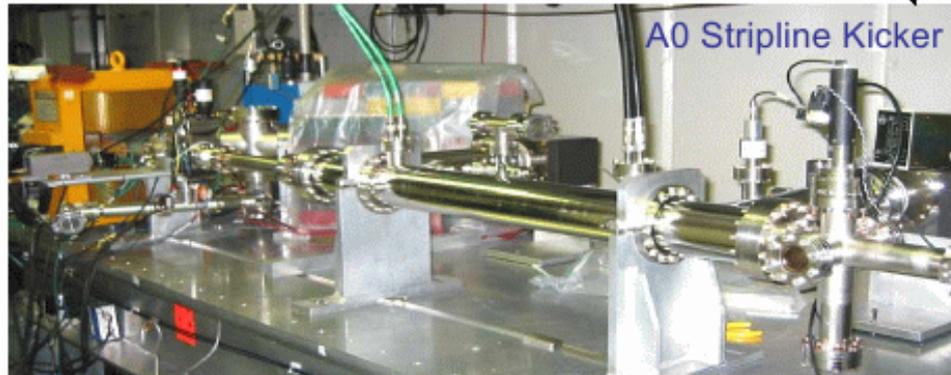
# Fast Kicker Progress

## Americas

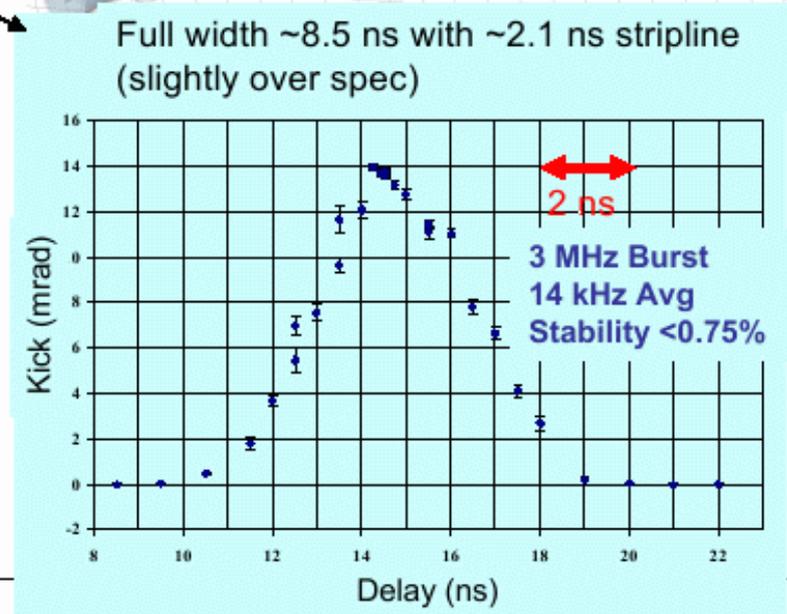
- Structures
  - Ongoing support for extraction kicker at ATF
  - Impedance modeling for ILC design
- Pulser Development
  - $t_{\text{pulse}} < 2t_{\text{bunch}} - 2t_{\text{stripline}} \sim 4.2 \text{ ns}$  at +/-10 kV
  - High availability/reliability for tens of units/ring
  - 3 MHz burst rate, 14 kHz avg rate (lowQ option  $\Rightarrow$  2x rate)
  - Peak stability requirements:  $\sim 0.33\%$  for each pulser
  - Tests of commercially available units from FID Technologies
    - +/-1 kV unit tested at FNAL-A0 (Cornell/UIUC)
    - 5 kV test in Japan
    - $\sim 10 \text{ kV}$  unit under development at FID
  - Ongoing Efforts
    - Inductive-adder technology for high availability
    - DSRD for improved pulse width performance
  - Goal: Downselect by late FY09



De Santis, LBNL



A0 Stripline Kicker

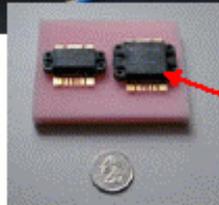
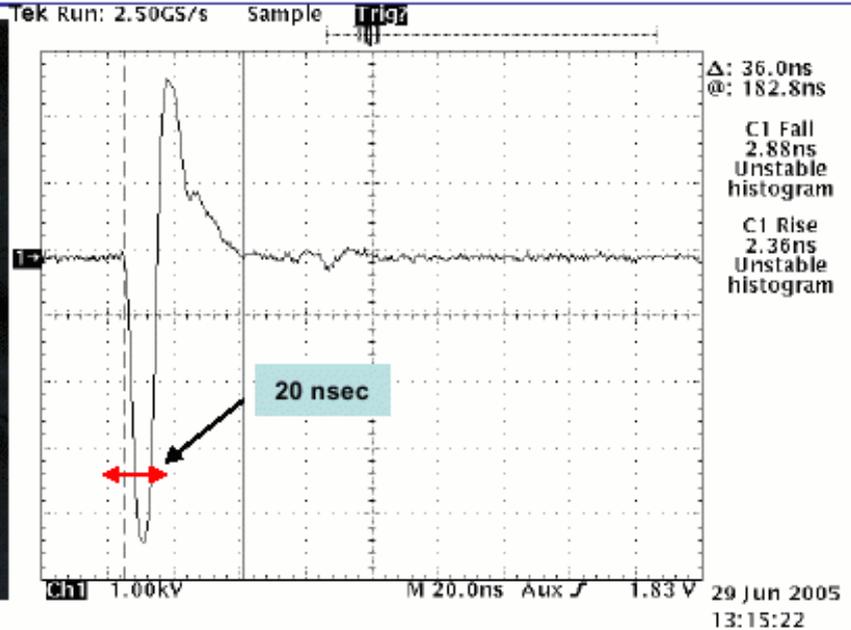
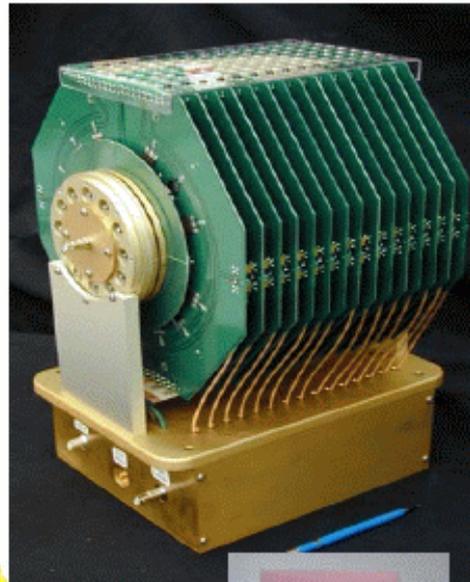


2007 DOE/NSF review  
April 30-May 2, 2007

Global design effort

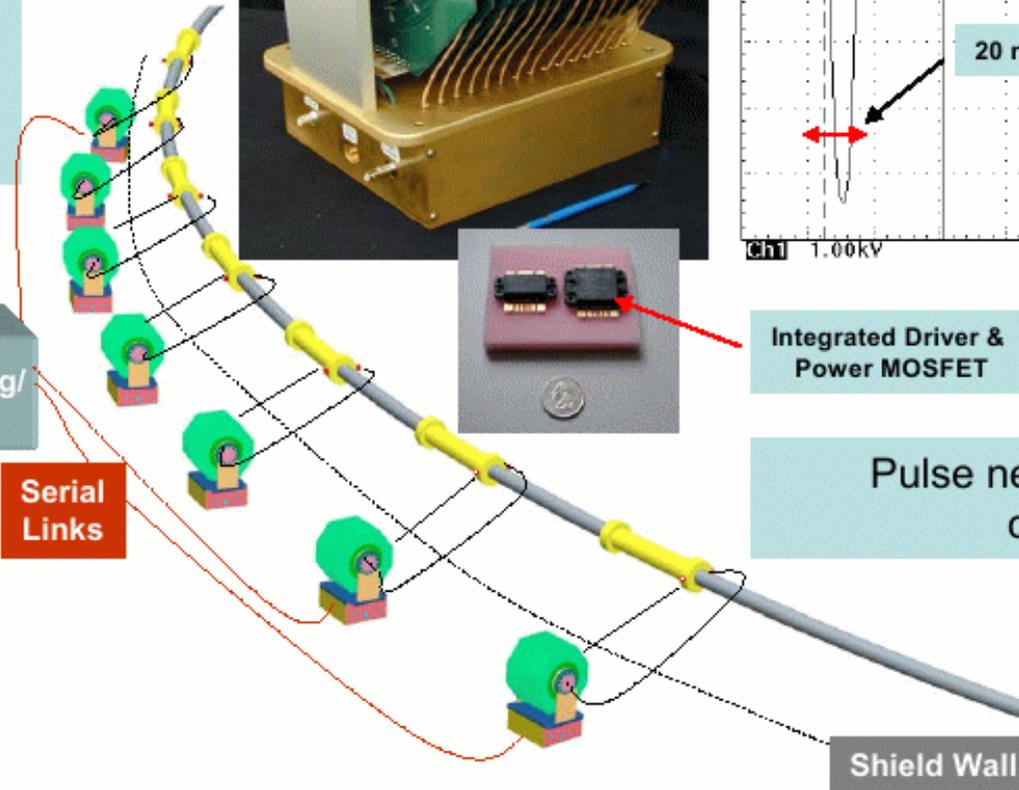
# HA Kicker System Topology

~60 pulsers per ring will be needed in a High Availability topology with auto-failover and access for replacement



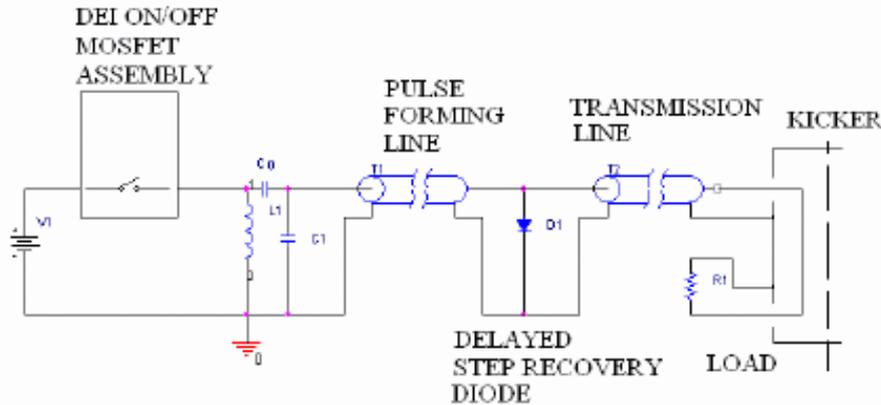
Integrated Driver & Power MOSFET

Pulse needs faster Tr, Tf, tail compensation



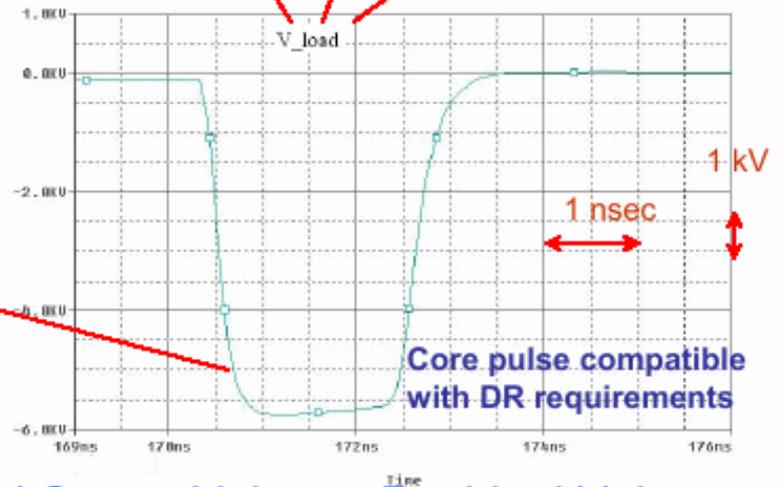
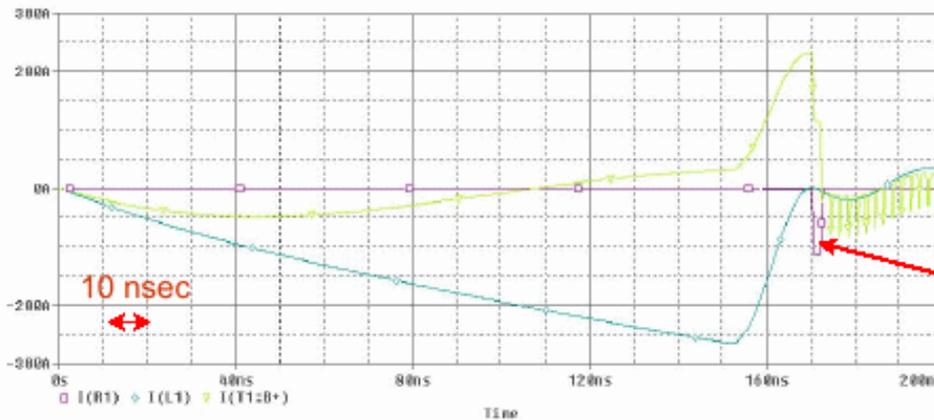
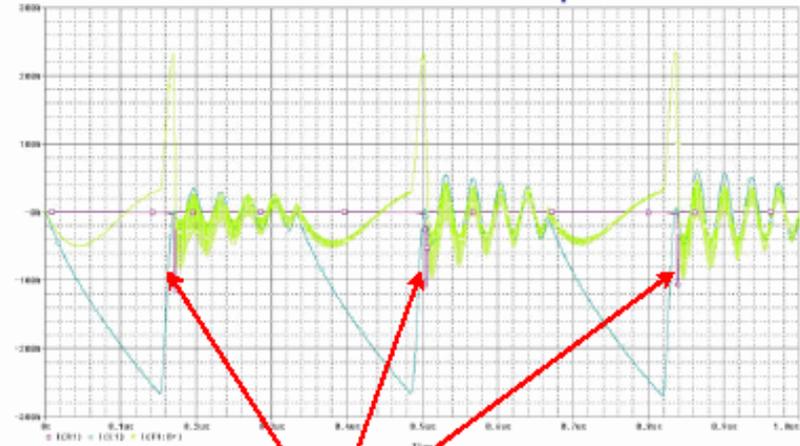
C. Brooksby, E. Cook  
BN/LLNL

# DSRD Detailed Circuit Behavior



$L=40 \text{ nH}$ ,  $C_0=30 \text{ nF}$ ,  $C_1=1.5 \text{ nF}$ ,  
 $t_{on}=150 \text{ nsec}$ ,  $t = 1 \text{ nsec}$

Achieved 3 MHz Rep Rate



Core pulse compatible with DR requirements

Currents vs. time for one cycle

~6kV Output Voltage, Residual Voltage ~ 2%