

PARTIAL DRAFT

Requirements for the Booster LLRF DDS Module

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TABLE OF CONTENTS

I. Introduction 3

II. The Frequency Curve and Booster Phase Lock 3

 II.1 Four Micro-Second Interpolated Frequency Curve 3

 II.2 DDS Frequency Word Scale Factor 3

 II.3 The Injection Frequency Curve..... 3

 II.4 Delay From Trigger 4

 II.5 Ramping the Frequency Back to the Start 4

 II.6 Booster Frequency-Phase Lock 5

III. Phase Control in the LLRF DDS Module..... 8

 III.1 Specification of the Paraphase Function..... 8

 III.2 Three Phase Offset Curves 10

 III.3 Radial Position Control Phase Adjustment..... 10

 III.4 Phase Changes At Transition 11

IV. Booster LLRF DDS IO Signal Specifications..... 15

V. The Four Channel DDS Module..... 17

VI. Diagnostics 17

Requirements for the Booster LLRF DDS Module

January 12, 2007

I. Introduction

This document lists the requirements and specifications for a new LLRF DDS module for the Booster Low Level RF controls. The new module will eliminate the need for the analog phase shift modules in use currently by implementing multiple DDS RF signal synthesizers tied together by a common frequency digital word and manipulated individually by independent phase digital words.

II. The Frequency Curve and Booster Phase Lock

The frequency of the Booster LLRF sweeps from a starting frequency to a final frequency following a pre-defined frequency curve. The frequency curve is defined using time-value pairs. The pairs are generated by an ACNET console application **(WHAT IS THE NAME AND AUTHOR OF THIS APP)**. The time coordinate is an integer number of microseconds from the start of the curve. It is not a delta-time value as used in other curve generating applications.

II.1 Four Micro-Second Interpolated Frequency Curve

The Frequency Curve programmed by the operator can have as many as 1024, 32 Bit time-value pairs, arbitrarily spaced in time. When these points are updated or retrieved from non-volatile memory at initialization, the curve is interpolated into frequency values spaced 4 micro-seconds apart. This Interpolated Frequency Curve may have as many as 10,239 points. When the curve is played out, three more frequency points are interpolated between each pair of points in the curve to produce *frequency updates to the DDS at a rate of 1 micro-second per point*.

II.2 DDS Frequency Word Scale Factor

The scale factor between the 32 Bit values and frequency in Hertz is determined by the DDS component used to produce the final RF sine wave signal, and its reference clock frequency. This scale factor will be fixed upon completion of the DDS circuit design. **CHOOSE A REFERENCE FREQUENCY AND COMPUTE THIS SCALE FACTOR AND LIST IT HERE.**

II.3 The Injection Frequency Curve

Additionally, the initial point of the Frequency Curve, the Injection Frequency, can be adjusted independent from the Frequency Curve itself. This is done by specifying the number curve points to use to ramp from the desired Injection Frequency to the frequency on the 4 micro-second Interpolated Frequency Curve. If the number of injection curve points is specified as the variable n_{INJ} , then the first n_{INJ} points of the 4 micro-second Interpolated Frequency Curve are replaced by this new ramp. The maximum number of injection curve points is designated as n_{INJMAX} . The first n_{INJMAX} number of points of the Interpolated Frequency Curve are always buffered so these can be used in the recalculation of the injection curve points when the Injection Frequency is

readjusted by the operator. Minimum and maximum values for the Injection Frequency and the number of injection points are listed in Table II.1.

The manner in which the new ramp is computed is as follows.

```
/* Psuedo 'C' Type Algorithm */
/*DATA TYPES
INT32 - 32 bit integer number /*originally implemented on an Analog Devices DSP*/
*/
/*VARIABLES
INT32 InjFreq → The injection frequency, the new initial point on the Frequency Curve.
INT32 InjDat[nINJMAX] → The first part of the Frequency Curve buffered so that the
injection curve points can be re-calculated. InjDat[0] is
the first point of the curve.
INT32 FreqCrv[1024] → The Frequency Curve.
INT32 FreqStep → The Frequency Offset Decrement Value.
INT32 nInj → The number of points to modify for the new injection curve.
INT32 Delta → Intermediate variable used below.
*/
/* !! Not shown is the extensive converting between integer and floating point numbers */
FreqStep = (InjFreq - InjDat[0]) / nInj;
Delta = (InjFreq - InjDat[0]); /*The initial frequency offset*/
For (i=0; i<nInj; i++)
{
    FreqCrv[i] = FreqCrv[i] + Delta;
    Delta = Delta - FreqStep;
}
/*end loop*/
```

II.4 Delay From Trigger

A TCLK event triggers the playing out of the Frequency Curve. The operator can specify a delay between this trigger and the playing out of the curve. At the time of the trigger the output frequency will have been set to the initial frequency point of the curve, the Injection Frequency. The Delay from Trigger parameter has a scale factor (and hence resolution) of 40 nano-seconds per Bit.

Minimum and maximum values for this parameter are listed in Table II.1. **THIS HAS CHANGED. THE DELAY IS IMPLEMENTED ON THE CAMAC TRIGGER SIGNAL BEFORE REACHING THE DFS-VCO MODULE**

II.5 Ramping the Frequency Back to the Start

At the end of each Booster cycle the LLRF reference signal frequency is ramped back to the initial Injection Frequency. This is accomplished by playing the curve in reverse, but with a larger step

size to speed things up. The LLRF DDS module typically has only 20 milli-seconds to rewind a 36 milli-second curve to be ready for the next cycle. This Reverse Step Size parameter is adjustable by the operator. Minimum and maximum values for this parameter are listed in Table II.1. **IS IT NECESSARY TO DO THINGS THIS WAY ??**

II.6 Booster Frequency-Phase Lock

The Booster beam bunch frequency throughout the acceleration cycle is predicted by the Frequency Curve and to first order does follow this trajectory. However it is very important that the LLRF reference signal frequency closely match both the frequency and phase of the beam. Therefore a signal phase comparison is made of the LLRF reference signal and the Booster beam bunch frequency as detected with a strip-line pick up in the accelerator. The phase error between these two signals is measured and fed back to the LLRF DDS module. A gain multiplies this error and the DDS frequency is adjusted in real-time by subtracting this product from the current Frequency Curve value before updating the DDS. This correction is made every 1 micro-second update.

This phase error correction is applied only when there is sufficient beam intensity available to make a good phase difference measurement and the Accelerator Phase Lock Enable Bit has been made active by the occurrence of certain TCLK events. **CLARIFY THESE BITS**. Minimum and maximum values for the Phase Error Gain parameter are listed in Table II.1.

PRESCRIBE SPECIFICATIONS FOR THE PHASE ERROR ADC INPUT

Table II.1 Scalar parameters for the LLRF DDS Module

Parameter	Min Value	Max Value	Default Value	Description
Injection Frequency	30 MHz	70 MHz	37.9 MHz	
Number of Injection Points	10	1000	500	
Reverse Step Size	1	10	4	
Phase Error Gain	2	65536	256	
Frequency Table Size	2	1024	--	
Frequency Curve Time Value	--	36000 (micro-second)	--	

Table II.2 Parameters from the current DFS-VCO Code

Program Name	Description	Value
FNPTSMAX	Maximum length of the 4 micro-second interpolated frequency curve	10239
FNPTSMIN	Minimum length of the 4 micro-second interpolated frequency curve	100 (not used ?)
BTFNPTS	Points of Non-volatile memory for frequency curve	40956 (not used ?)
UDRATE	Delta time between frequency curve points. Points are interpolated between each pair of frequency curve points to generate output frequency updates every 1 micro-second.	4 micro-seconds
INJFRQDEF	Injection Frequency Default Value	37.9 MHz
INJFRQMIN	Injection Frequency Minimum	30.0 MHz
INJFRQMAX	Injection Frequency Maximum	70.0 MHz
--info	Curve Delay Resolution	40 nano-seconds
REVSTEPDEF	Reverse Step Size Default Value	4
REVSTEPMIN	Reverse Step Size Minimum	1
REVSTEPMAX	Reverse Step Size Maximum	10
GAINDEF	Phase Error Gain Exponent Default Value (2^y)	8

GAINMIN	Phase Error Gain Exponent Minimum Value (2^y)	1
GAINMAX	Phase Error Gain Exponent Maximum Value (2^y)	16
FSIZEMIN	Frequency Table Size Minimum	2
FSIZEMAX	Frequency Table Size Maximum	1024
FTIMEMAX	Frequency Time Table Maximum	36000

Note: The Phase Error input gain results in a specific full scale frequency adjustment given a full scale Phase Error input. An example using the existing Booster DDS Bit to Hertz conversion is shown below.

Phase Error is digitized by a 12 Bit ADC

Full scale Phase Error Bits = +/- 2048 Bits

Default Phase Error Gain = $2^8 = 256$

Existing Booster DDS Conversion = 0.133877 Hz / Bit

*Full scale frequency adjustment per update = +/- (2048 * 256 * 0.133877) = +/- 70,190 Hz*

*** Every 1.0 micro-second the Phase Error is read, the gain is applied to this error and the frequency correction is applied to the DDS.*

Considering the minimum and maximum Phase Error Gain Exponent listed in the table above {2..16} we can see that we can set the full scale frequency adjustment due to a full scale phase error from

*+/- (2048 * 2 * 0.133877) = +/- 548.7 Hz (resolution of 0.2677 Hz)*

to

*+/- (2048 * 65,536 * 0.133877) = +/- 17,968,667 Hz (resolution of 8,734 Hz)*

III. Phase Control in the LLRF DDS Module

The greatest benefit of the new LLRF DDS Module is derived from the ability to manipulate the phase of each of the four LLRF output signals independently. In the following sections we will describe the various accelerator control functions that manipulate the LLRF phase. The phase offset words that are updated in the LLRF DDS's are the sums of preprogrammed curves and a real-time phase adjustment from the Radial Position Controller (a.k.a the Phase Shift Controller, 0331.00-ED-63397).

Note that the phases of only two of the four LLRF DDS's are adjusted by writing phase words to the DDS's. The phase of the LLRF reference signal used in the acceleration phase lock described in Section II.6 is not manipulated in this manner. Likewise the reference signal produced as the BPM LO signal is not phase adjusted. Again, only the group 'A' and group 'B' reference signals described in the following are phase adjusted.

A block diagram of the frequency and phase controls for the module are illustrated in the block diagrams of Figure III.1 and Figure III.2 found near the end of this section.

NOTE: In the current configuration of the interface between the Booster Low Level RF and High Level RF systems the phase of the 'B' LLRF signal is shifted 180 degrees. A final shift of 180 degrees is applied in the High Level RF system. In the discussion to follow this shift in the group 'B' signal between the LLRF and HLRF systems is not considered, but rather the signal phases at the output of the HLRF system are described. A shift in the group 'B' signals may be accomplished by inverting the most significant bit of the group 'B' phase offset word before it is written to the DDS. By using an XOR gate a control bit could be defined that determines if the group 'B' signals receive the 180 degree shift or not.

III.1 Specification of the Paraphase Function

Booster RF stations are divided into two groups, 'A' and 'B'. At the beginning of the Booster cycle the phase of the RF applied to A stations are 180 degrees out of phase with the B stations. The net RF field applied to the beam is zero in this instance, and hence there is no net acceleration or bunching of the beam. Over the next 600 micro-second interval the phase difference between group 'A' and group 'B' is driven to zero according to a predefined curve.

The Paraphase Curve represents phase offsets from -90 degrees to + 90 degrees. This offset is subtracted from the net group 'A' phase and added to the net group 'B' phase. Hence by ramping the paraphrase curve value from 90 degrees to 0 degrees we accomplish the desired 180 degree to 0 degree phase difference transition between groups 'A' and 'B'.

Table III.1.1 Summary of the paraphase curve parameters.

Time Interval Between Curve Points	1.0 micro-second
Paraphrasing Interval	600 micro-seconds
Number of curve points	600
Phase Range	+/- 90 Degrees
DDS Phase Word Resolution	14 Bits



At the end of the 600 micro-second interval the final value of the paraphase curve is held with offsets being added to this value at desired times during the remainder of the Booster cycle. There are three different offsets that can be summed into the paraphase curve signal. The first is a base offset for the entire interval. The next two are single 14 bit signed values each with a programmable time offset parameter that specifies when in the Booster cycle these offsets are applied. These are the Transition Offset and the Bunch Rotation Offset. Once these offsets are applied they remain in until the end of the Booster cycle.

Table III.2 gives a list of the parameters for this application that are able to be Read and Written by the ACNET control system.

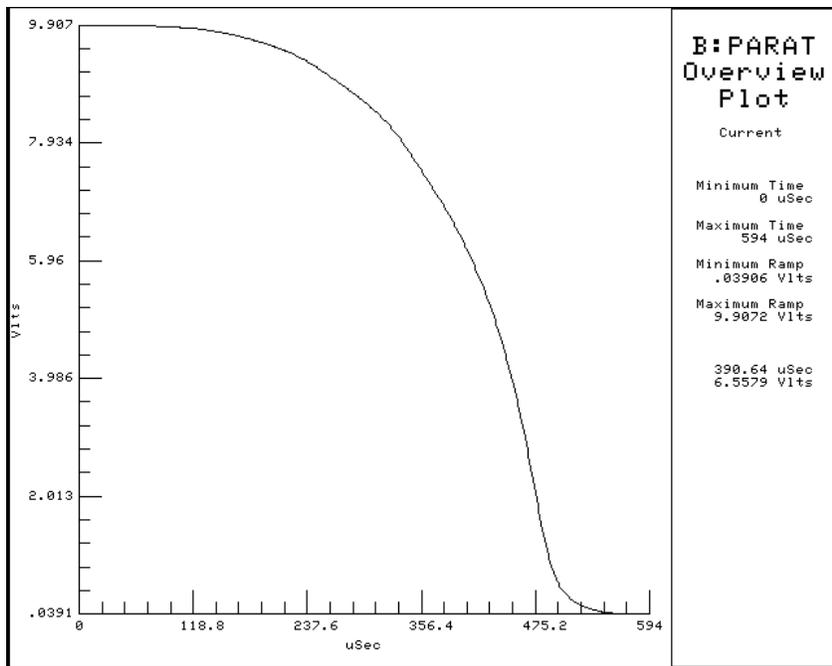


Figure III.1.1 Typical paraphase curve plot.

Table III.1.2 List of parameters that can be Read or Written by ACNET.

Index	Acnet Name	Units	Scale Factor	Parameter Description
0	PARAMM	--	--	Number of values in the base paraphase curve.
1	PC1OFF	Counts	1.221 Volts per Count	C1 Offset: Baseline offset for the paraphase curve.
2	PC2OFF	Counts	1.221 Volts per Count	C2 Offset: Post-Transition offset for the paraphase curve.
3	PBROFF	Counts	1.221 Volts per Count	BR Offset: Beam Rotation offset for the paraphase curve.

4	PC2CNT	Clocks	1.0 micro-seconds per Clock	C2 Count: Apply Offset C2 at this number of 1.0 micro-second clocks from the start of the cycle.
5	PBRCNT	Clocks	1.0 micro-seconds per Clock	BR Count: Apply Offset BR at this number of 1.0 micro-second clocks from the start of the cycle.
6	PhaseCurve1			The Paraphase Curve.

III.2 The Phase Offset Curve and A/B Phase Balance

The LLRF DDS Module also contains a curve that act to offset the phase of the group ‘A’ and ‘B’ RF signals. The Phase Offset Curve acts to offset the phase of both the group ‘A’ and ‘B’ signals equally. A separate Phase A Offset Value (scalar) offsets the phase of group ‘A’ only. Likewise, the Phase B Offset Value offsets the phase of group ‘B’ only.

The Phase Offset curve is delivered to the LLRF DDS Module as up to 512 time/value pairs. It is the job of the LLRF DDS Module to interpolate linearly the 1 micro-second update values from these pairs.

The specification for this curves is given in Table III.2.1.

Table III.2.1 Specification of the Phase Offset Curves.

Time Interval Between Curve Points	1.0 micro-second
Number of curve points	
Phase Range	+/- 90 Degrees
DDS Phase Word Resolution	14 Bits

III.3 Radial Position Control Phase Adjustment

The radial position of the beam is manipulated by varying the phase of both the group ‘A’ and group ‘B’ RF stations. An analog signal out of the Radial Position Controller, PSDRV, is input to the LLRF DDS Module to drive this phase adjustment. This +/- 10 Volts scales to a +/- 90 degree phase change. Unlike the paraphase phase adjustment, this input shifts the phase of group ‘A’ and ‘B’ together in the same direction.

The output of the Radial Position Controller is inverted at and after the accelerator transition. That is the output is multiplied by -1. At the onset of transition a scale factor of the PSDRV voltage is ramped from +1 through 0 to -1 in an adjustable time interval of 10 to 40 microseconds.

Before transition, a **positive (+) voltage** output of the Radial Position Controller indicates that the beam is positioned at a radius that is larger than desired. To correct this condition a **lag in the phase** of groups ‘A’ and ‘B’ RF is called for. Figure III.3.1 shows the effect at the cavity. Given

the timing of the beam batch arrival at the interaction region of the cavity, the beam batch receives less of a kick with the RF phase lagging. With less of a kick and an increasing field in the bending magnets, the radius of the beam orbit will grow smaller.

When the beam is positioned at a radius smaller than desired, before transition, there is a **negative (-) voltage** output of the Radial Position Controller causing a **leading phase shift** of groups 'A' and 'B' RF.

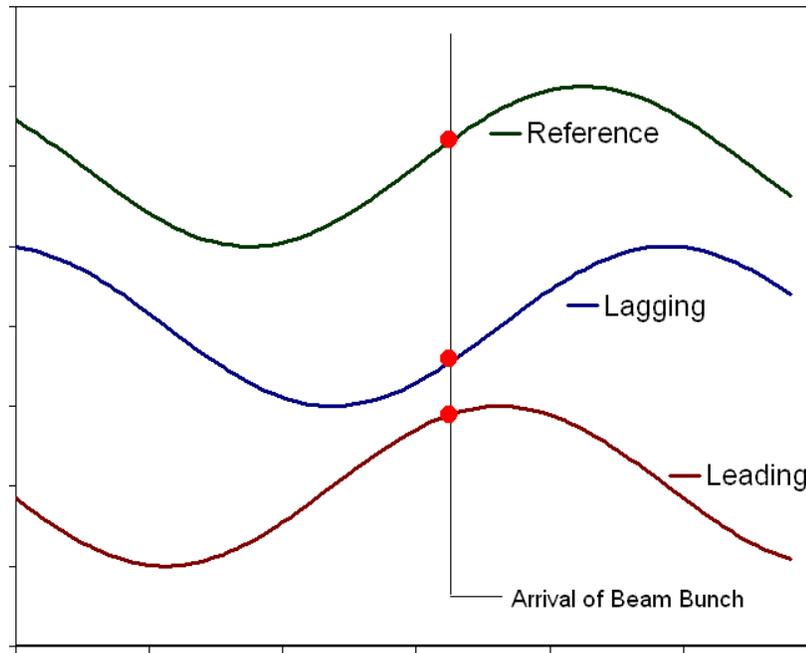


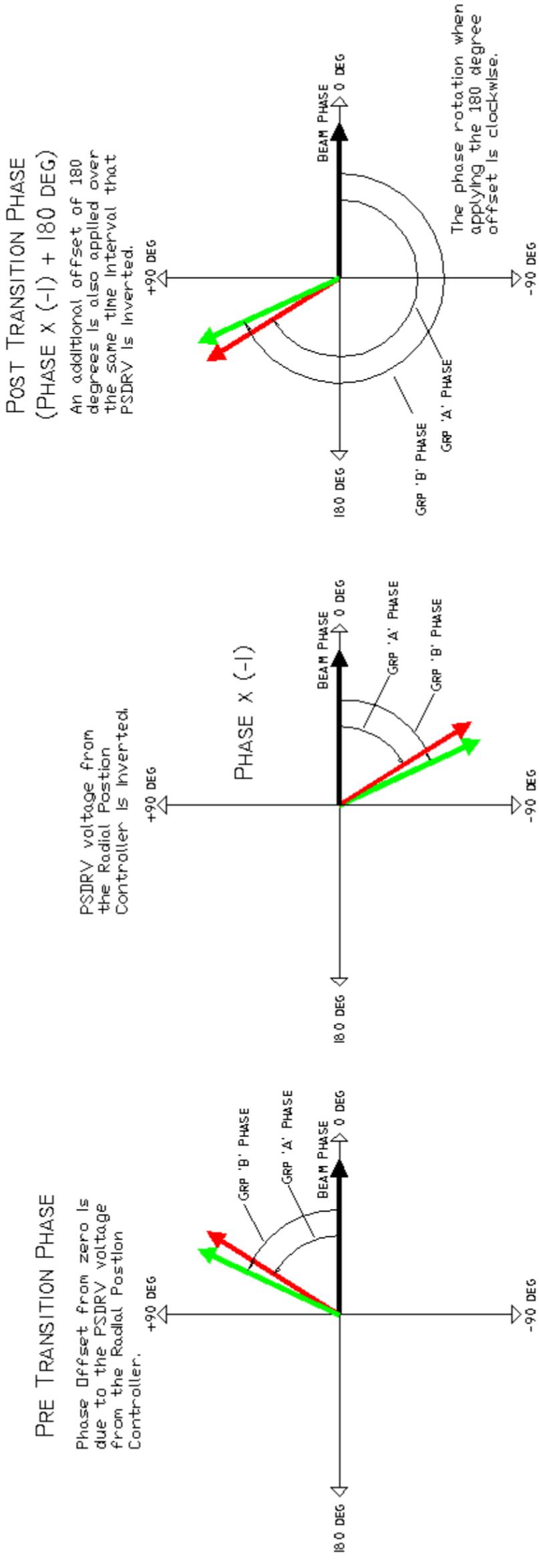
Figure III.3.1 Illustration of leading and lagging RF phase w.r.t. the arrival of a beam bunch (pre-transition).

Prescribe an ADC for digitizing this signal and possibly an operator adjustable gain term.

III.4 Phase Changes At Transition

This section will be revised in the near future.

The RF cavity phase at transition time must be modified. Figure III.4.1 illustrates the manner that the phases change. When triggered at transition, a scale factor of the Radial Position Controller PSDRV voltage is ramped from +1 through 0 to -1 in an adjustable time interval of 10 to 40 microseconds. Simultaneously the phase of the group 'A' and 'B' RF is phase shifted 180 degrees over the same 10 to 40 microsecond interval. The 180 degree phase shift is executed with the phase offset decrementing, that is rotating clockwise. The transition trigger is a TCLK trigger with a settable time delay offset.



III.4.1 Phase manipulation at Booster transition.

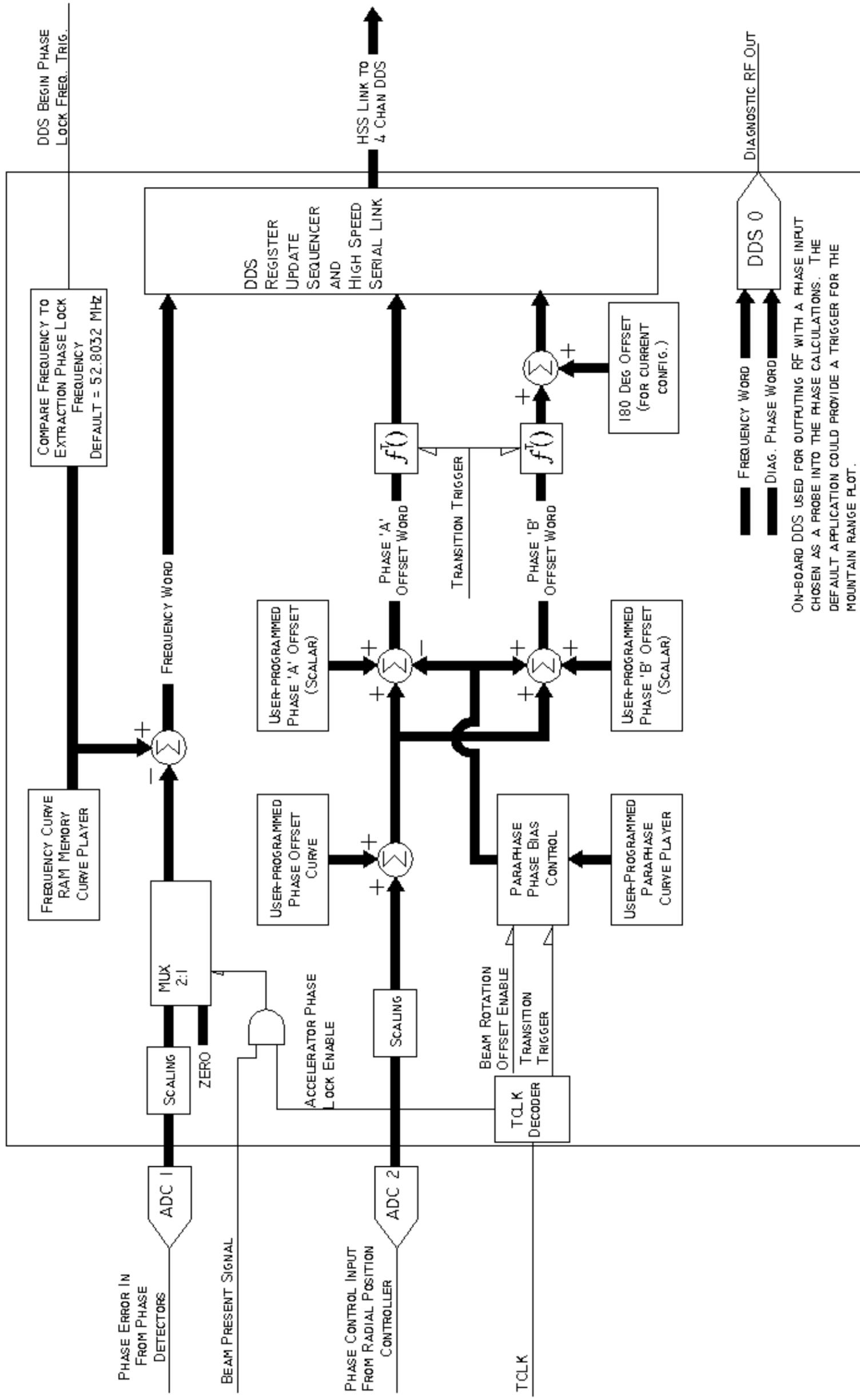


Figure III.1

QUAD DDS MODULE

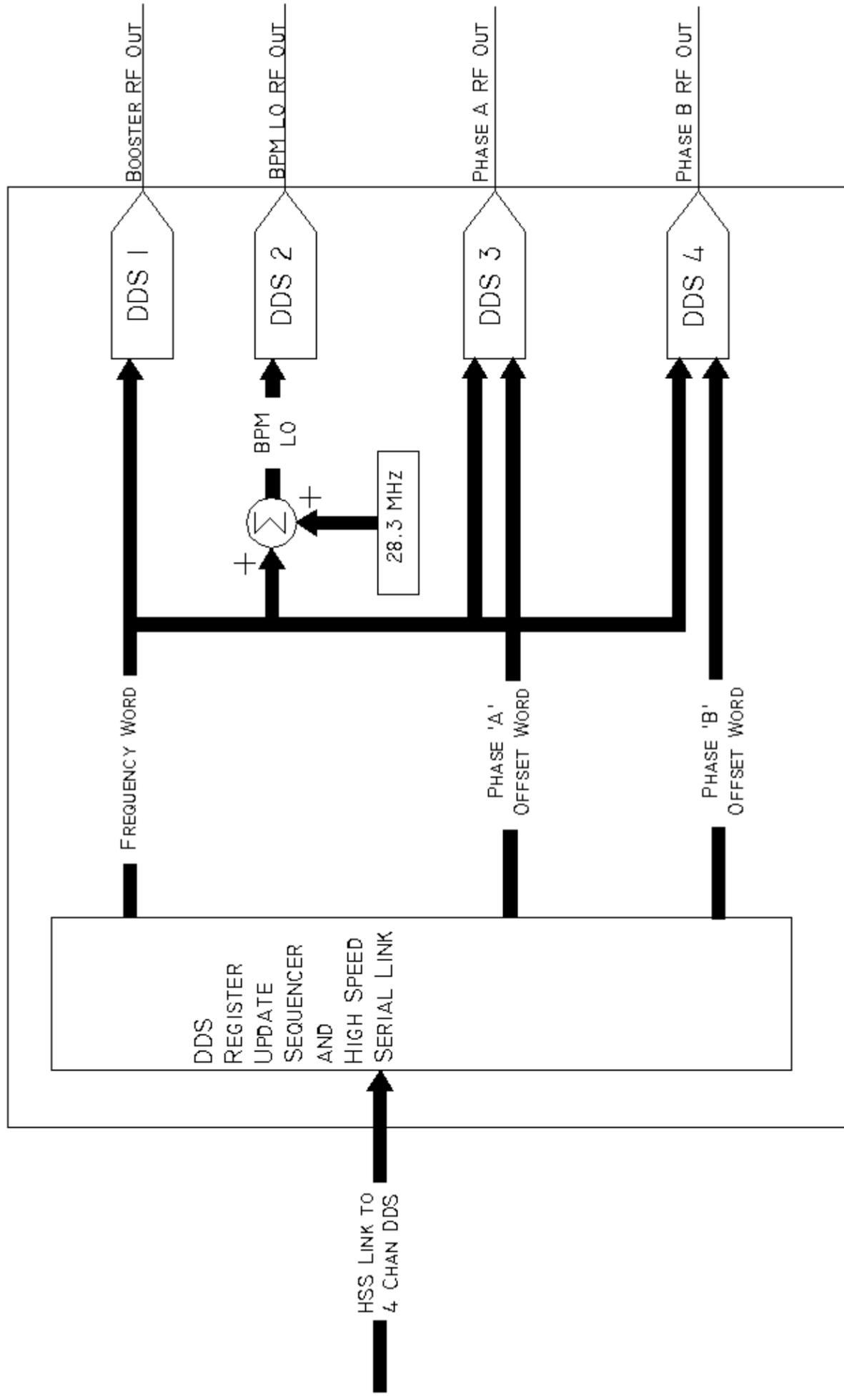


Figure III.2

IV. Booster LLRF DDS IO Signal Specifications

PUT SPECIFICATION OF ADC's AND DAC's HERE

Table IV.1 DDS-VCO Application Inputs and Outputs.

Signal	I/O	Voltage Type	Term. Ohms	Connector	B.W. or Freq. Range	Amplitude Range	Res.	Update Rate
Phase Error from the Phase Controller (Digital)	I	16 bit digital word		VXI Local Bus	4.0 KHz		14 Bit	10 KHz
Phase Error from the Phase Controller (Analog)	I	L.F. Analog	> 500	Lemo Coax	4.0 KHz	+/- 10 V or +/- 1.0 V	14 Bit	10 KHz
Radial Position Control Signal	I	L.F. Analog	> 500	Lemo Coax	< 10 KHz	+/- 10 V or +/- 1.0 V	14 Bit	1.0 MHz
Bias Curve Permit from HLRF	I	Digital	> 500 50 Ohm optional	Lemo Coax		TTL		
Beam Present Indicator	I	Digital	> 500 50 Ohm optional	Lemo Coax		TTL		
Acceleration Phase Lock Enable	I	TClk Trigger	> 500 50 Ohm optional	Lemo Coax		TTL		
Transition Trigger	I	TClk Trigger	> 500 50 Ohm optional	Lemo Coax		TTL		
Beam Rotation Offset Enable	I	TClk Trigger	> 500 50 Ohm optional	Lemo Coax		TTL		
End of Booster Cycle	I	TClk Trigger	> 500 50 Ohm optional	Lemo Coax		TTL		
Begin MI Phase Lock Trigger	O	Digital	50	Lemo Coax		TTL		
HLRF Cavity Bias Curve Out	O	L.F. Analog	1.0K	Lemo Coax	< 100 KHz	+/- 10 V	14 Bit	1.0 MHz
Frequency Curve Monitor Out	O	L.F. Analog	1.0K	Lemo Coax	< 100 KHz	+/- 10 V	14 Bit	1.0 MHz
Booster RF Out	O	DDS RF	50	SMA Coax	37 to 53 MHz	0 to 10 dBm	14 Bit	200 MHz
Booster Phase A RF Out	O	DDS RF	50	SMA Coax	37 to 53 MHz	0 to 10 dBm	14 Bit	200 MHz
Booster Phase B RF Out	O	DDS RF	50	SMA Coax	37 to 53 MHz	0 to 10 dBm	14 Bit	200 MHz
Booster BPM LO Out	O	DDS RF	50	SMA Coax	65.8 to 81.8 MHz	0 to 10 dBm	14 Bit	200 MHz

Table Extended Application Inputs and Outputs.

Signal	I / O	Voltage Type	Term. Ohms	Connector	B.W. or Freq. Range	Amplitude Range	Res.	Update Rate
Delayed Booster DDS-VCO RF #1 <i>Input directly to the Phase Detector IP Module. (Note 1)</i>	I	RF Sinewave	50	BNC Coax Front Panel to IP cable assy.	37 to 53 MHz	0 to 10 dBm		
Delayed Booster DDS-VCO RF #2 <i>Input directly to the Phase Detector IP Module (Note 1)</i>	I	RF Sinewave	50	BNC Coax Front Panel to IP cable assy.	37 to 53 MHz	0 to 10 dBm		
Main Injector RF <i>Input directly to the Phase Detector IP Module (Note 1)</i>	I	RF Sinewave	50	BNC Coax Front Panel to IP cable assy.	52.8 MHz	0 to 10 dBm		
Booster RF from Strip-line Detector <i>Input directly to the Phase Detector IP Module (Note 1)</i>	I	RF Sinewave	50	BNC Coax Front Panel to IP cable assy.	37 to 53 MHz	-20 to 0 dBm		
Radial Position Signal (BPM)	I	Analog	> 500 50 Ohm optional	Lemo Coax	1.0 MHz	+/- 10 V or +/- 1.0 V	14 Bit	10 MHz
BDOT Magnet Current / Field Strength	I	Analog	> 500 50 Ohm optional	Lemo Coax	1.0 MHz	+/- 10 V or +/- 1.0 V	14 Bit	10 MHz
Cogging Radial Position Control Signal	I	Analog	> 500 50 Ohm optional	Lemo Coax	1.0 MHz	+/- 10 V or +/- 1.0 V	14 Bit	10 MHz
Acceleration Phase Error Monitor Out <i>Output directly from the Phase Detector IP Module. (Note 1)</i>	O	L.F. Analog	> 1.0 K	Lemo Coax Front Panel to IP Module cable assy.	4.0 KHz	+/- 10 V	14 Bit	10 KHz
MI Phase Error Monitor Out <i>Output directly from the Phase Detector IP Module. (Note 1)</i>	O	L.F. Analog	> 1.0 K	Lemo Coax Front Panel to IP Module cable assy.	4.0 KHz	+/- 10 V	14 Bit	10 KHz
Radial Position Control Monitor Out	O	L.F. Analog	> 1.0 K	Lemo Coax	< 10 KHz	+/- 10 V	14 Bit	1.0 MHz
Radial Position Error Monitor Out	O	L.F. Analog	> 1.0 K	Lemo Coax	< 10 KHz	+/- 10 V	14 Bit	1.0 MHz
Radial Position Control Disable	O	Digital	50	Lemo Coax		TTL		

Note 1: These Inputs and Outputs are brought directly from the front panel to the IP module via a custom coaxial cable assembly.

V. The Four Channel DDS Module

The Four Channel DDS Module is built separate from the main processor module in order to make the signal generation function of this module available to other processing platforms. The current target for the processing is a CAMAC module. Other possible platforms would be a VME Power PC Crate processor or even the VXI-DSP processor card used currently in the Booster. The candidate processing platform would need to implement the High Speed Serial Link (HSSL) using either a custom or commercial daughter card or another module within its address space.

The candidate DDS component for this application is the Analog Devices part number **AD9958**.

MORE SPECIFICATION TO COME

V.1 Programmable Logic and Memory Requirements for the DDS Module

V.2 High Speed Serial Link Requirements

V.3 DDS Output Analog Filtering and Drive Requirements

VI. Diagnostics

Specify a number of ADC to read out phase curves and frequency curve with a scope.

In addition to the four DDS outputs connected to the processing module via the High Speed Serial Link, there is a need for a DDS channel on board the processor module for use in both booster mountain range plot diagnostics and for probing intermediate phase and frequency calculations within the firmware of the processor module.

The existing system uses a version of the LLRF signal to synchronize the **mountain range plotting** that is shifted in phase just as the group 'A' or group 'B' signals without the application of the phase change at transition. Therefore, this additional DDS output is necessary for this application.