Stacked Transformer Modulator Progress

Greg Saewert

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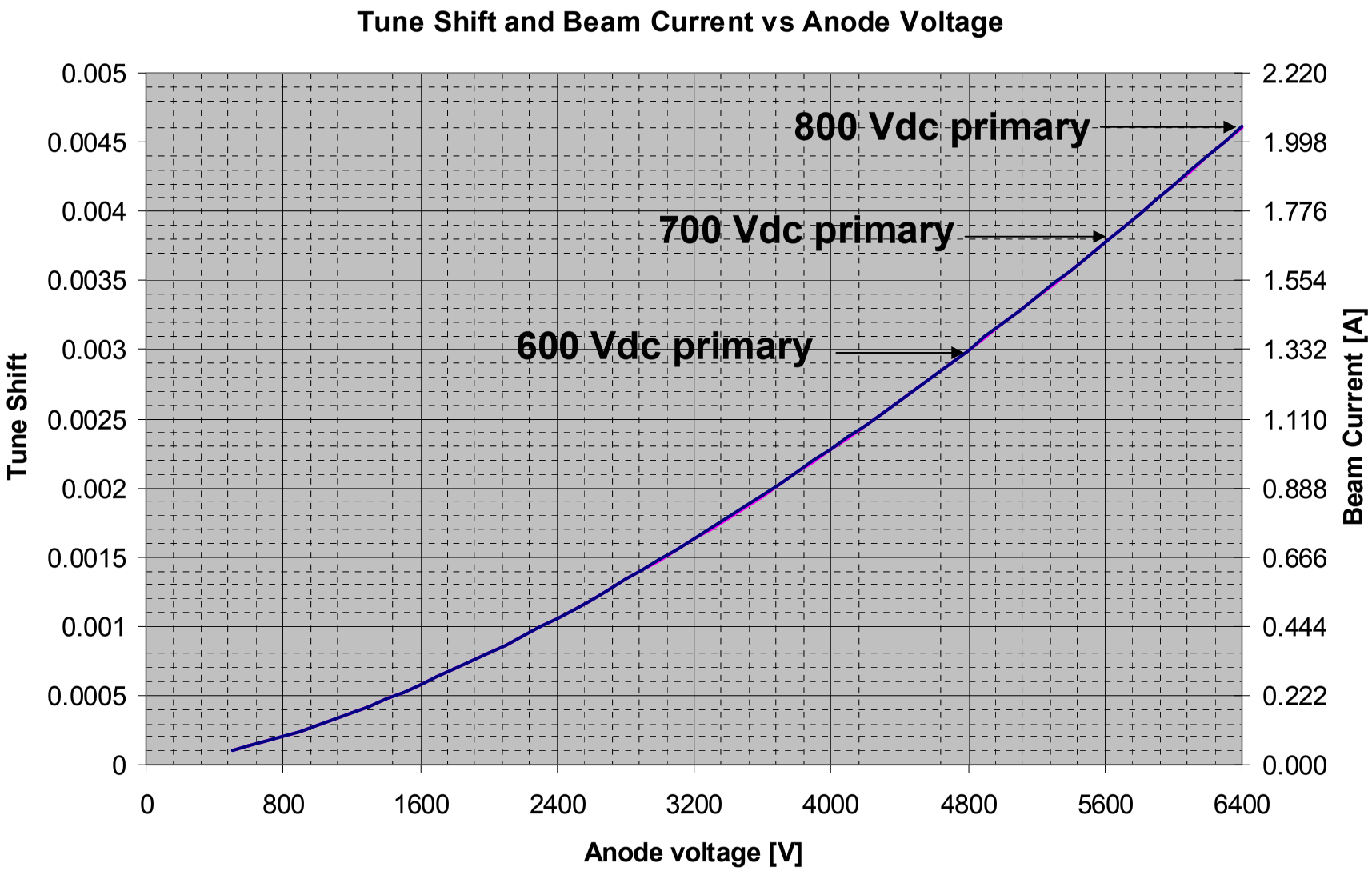
Information presented

- Review specifications.
- Present results of bench tests.
- Show some aspects of the design.
- Highlight work remaining.

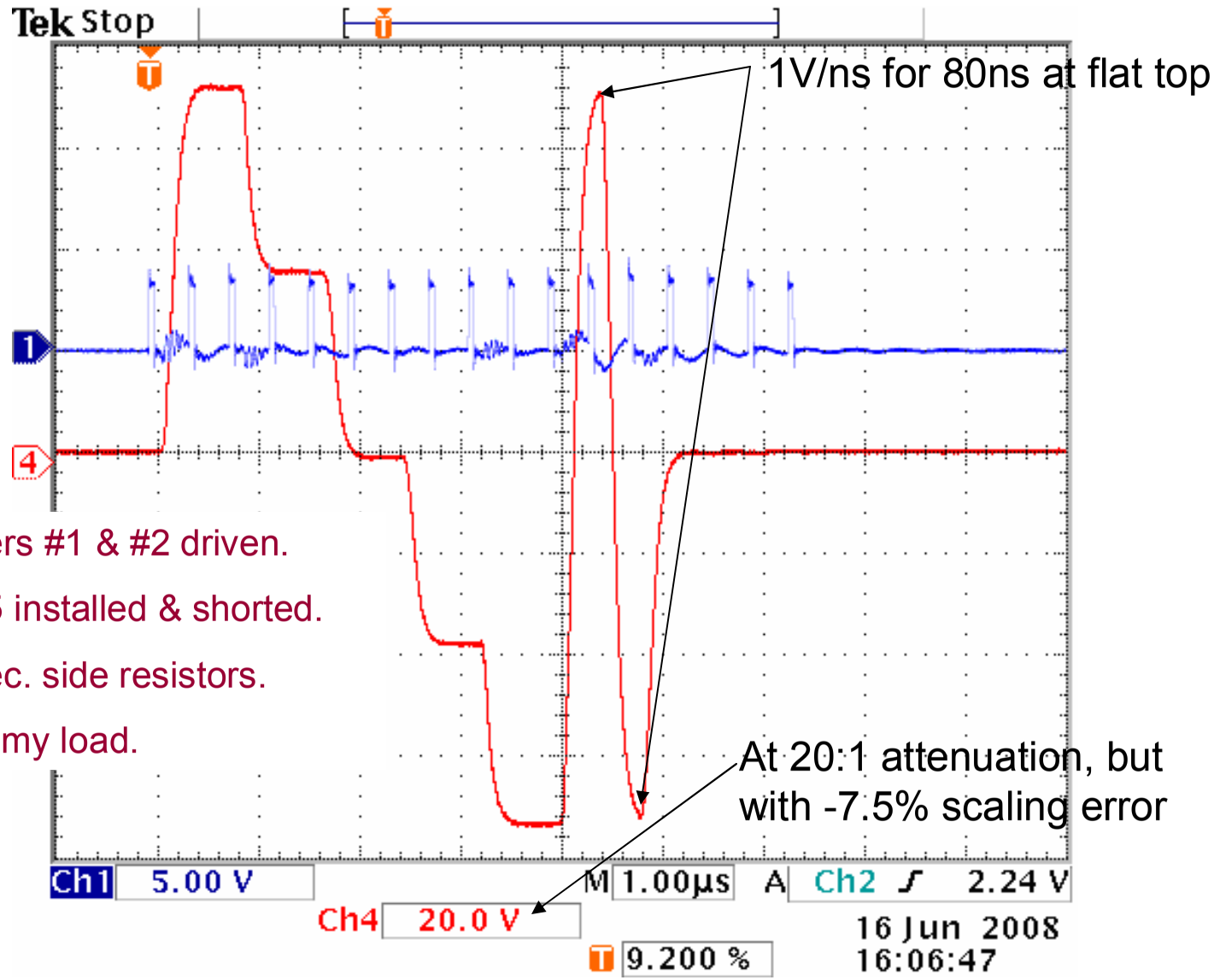
Specs: Design goals

- Output voltage 5 kV min.
- Ability to tune shift all 36 bunches.
- Individually adjustable voltage for 12 bunches that can be repeated 3 times per Tevatron revolution.
- 12 bunch voltage waveform must be capable of being complex.
- Voltage output must be low ripple.
- Voltage flat top for 6 ns can have ?? V/ns flatness. (need not be 0.0 V/ns)

Specs: tune shift vs. anode voltage



Tests: Output plots



Transformers #1 & #2 driven.

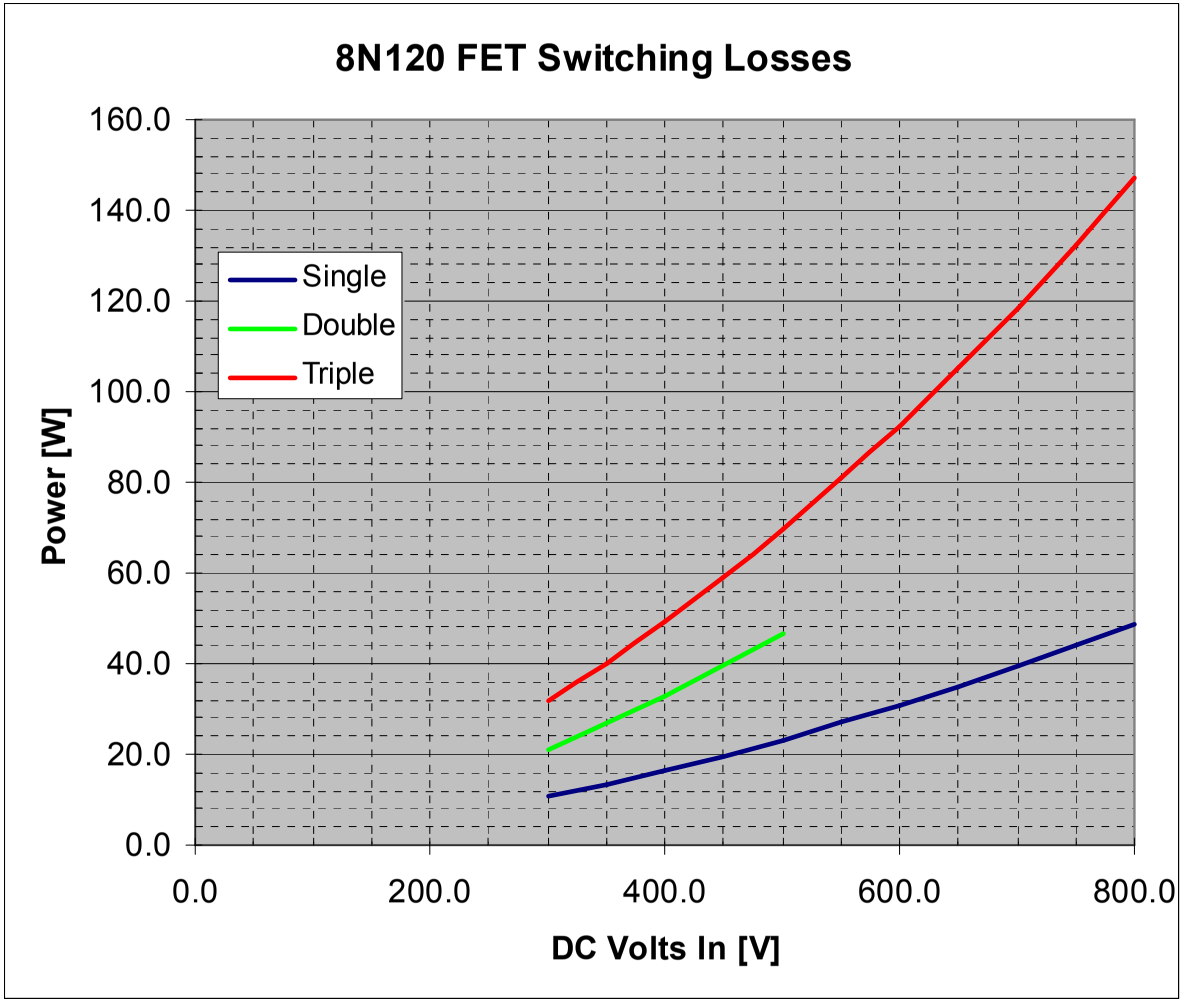
#3, #4 & #5 installed & shorted.

5 x 90 Ω sec. side resistors.

100pF dummy load.

Tests: Switching losses – FETs only

1 Driver board is driven, transformer primary is disconnected.

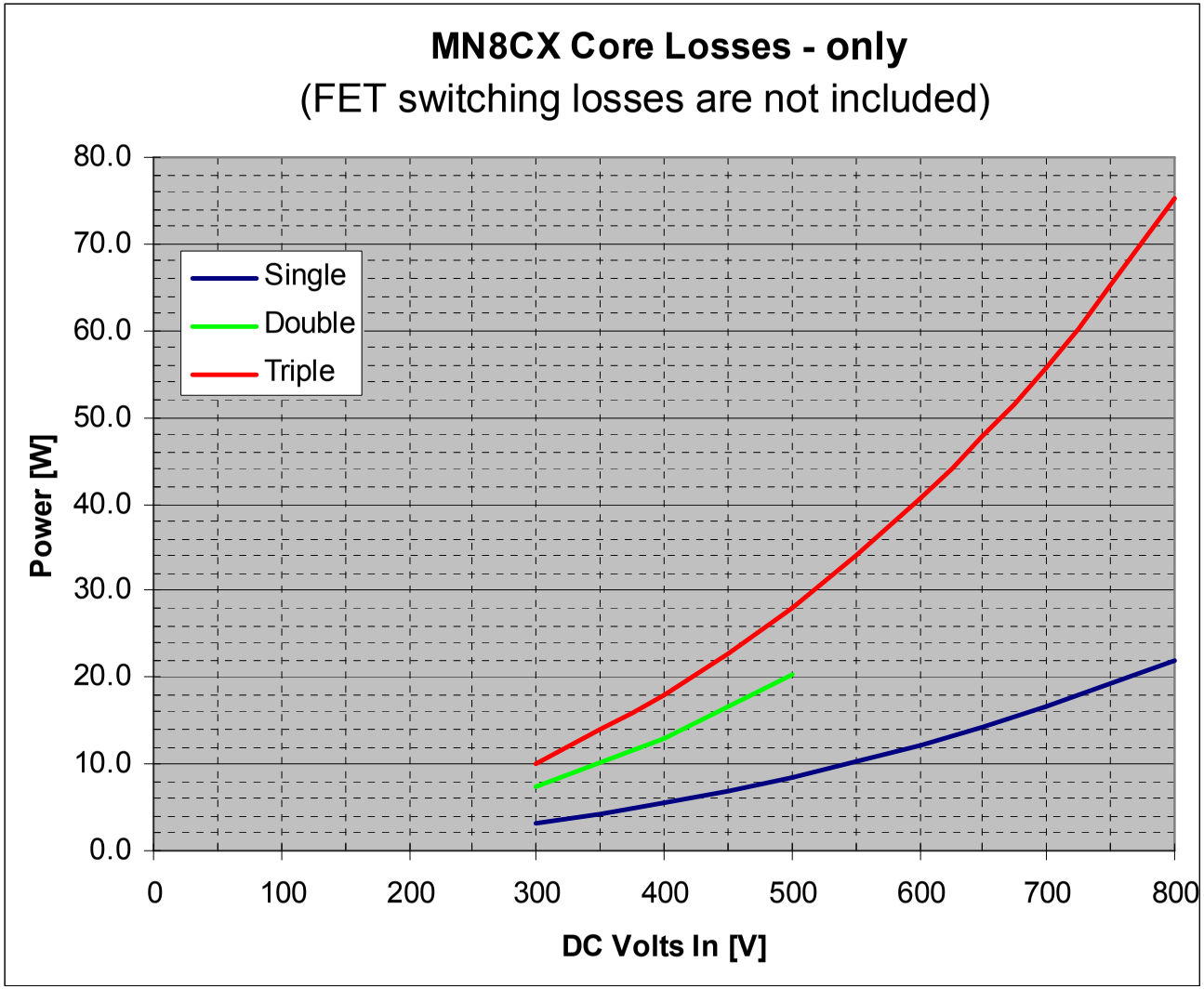


Tests: Switching losses - FETs only (cont.)

- Single, double and triple pulse cycles are within a 7.0μs period.
- All FETs switch equal number of times per cycle.
- Each pulse cycle includes both a positive, negative and return-to-zero voltage swing.
- H-bridge switches at 150 kHz for single pulse cycle, 300 kHz for double and 450 kHz for triple.
- Power dissipation is pulse width independent, as measured.
- FET power dissipation is entirely a result of charging/discharging drain-source capacitance.
- Power is $P_{FET} = .5 \cdot C \cdot V^2 \cdot f$.
- C = 255 pF per switch action.
- Each FET turn-on charges one FET and discharges another.
- Each FET drain-source capacitance is 122 pF.
- 8N120 FET spec: C_{oss} = 59 pF. Capacitance balance includes diode(s) and heat sink parasitics.

Tests: Switching losses - Core

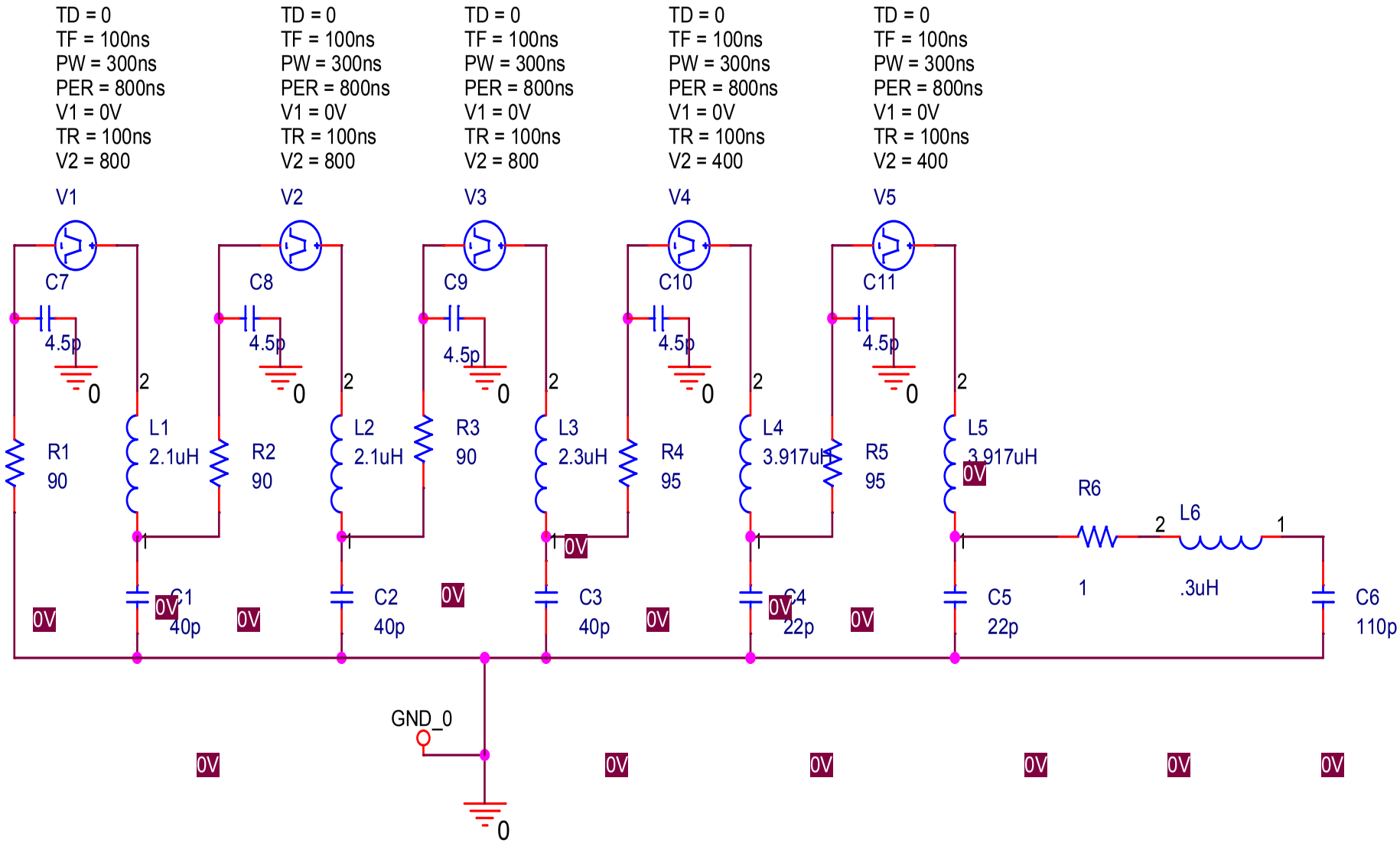
Transformer secondary left open circuit



Tests: Switching losses - Core (cont.)

- What is the FET $I^2 \cdot R$ loss to deliver power to the core? Consider the case of highest power loss:
  - Total dissipated power = FET switching loss + core loss + FET $I^2 \cdot R$ loss.
  - The same current flows through the primary and FET H-bridge.
  - $P_{PS} = P_{sw} + I \cdot V_{pri} + I^2 \cdot R_{ds}$ (Watts).
    - 222 = 147 + I·800 + I2·2.1 (Watts).
    - I = .094A.
    - 222 = 147 + 75 + .04 (Watts average).

Tests: Using measured parasitics



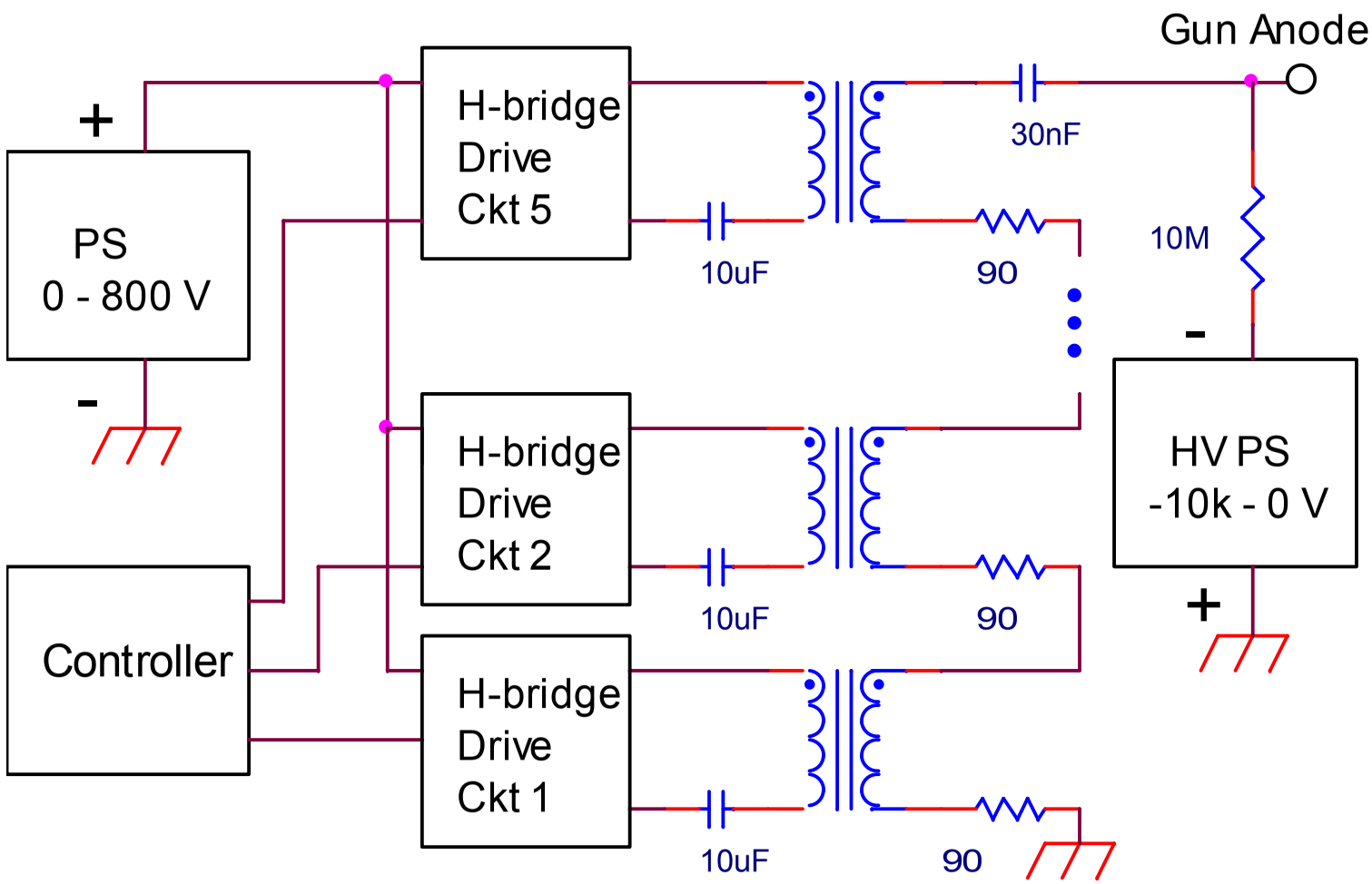
Tests: Using measured parasitics

4	Secondary resistor power dissipation - Vpri = 800V; 3200Vp; 6400Vpp							
5	**Switching rate**	**X1 R**	**X2 R**	**X3 R**	**X4 R**	**X5 R**	**Anode R**	**Total Power**
6	150,000	58.9	53.3	42.5	30.6	24.2	2.0	211.5
7	300,000	117.7	106.6	85.1	61.2	48.4	3.9	422.9
8	450,000	176.6	159.9	127.6	91.8	72.5	5.9	634.4
9								
10	Secondary resistor power dissipation - Vpri = 700V; 2800Vp; 5600Vpp							
11	**Switching rate**	**X1 R**	**X2 R**	**X3 R**	**X4 R**	**X5 R**	**Anode R**	**Total Power**
12	150,000	45.1	40.9	32.6	23.5	18.5	1.5	162.1
13	300,000	90.2	81.7	65.2	46.9	37.1	3.0	324.2
14	450,000	135.4	122.6	97.8	70.4	55.6	4.5	486.2
15								
16	Secondary resistor power dissipation - Vpri = 600V; 2400Vp; 4800Vpp							
17	**Switching rate**	**X1 R**	**X2 R**	**X3 R**	**X4 R**	**X5 R**	**Anode R**	**Total Power**
18	150,000	33.4	30.2	24.1	17.4	13.7	1.1	120.0
19	300,000	66.8	60.5	48.3	34.7	27.4	2.2	239.9
20	450,000	100.2	90.7	72.4	52.1	41.2	3.3	359.9
21								
22	Secondary resistor power dissipation - Vpri = 500V; 2000Vp; 4000Vpp							
23	**Switching rate**	**X1 R**	**X2 R**	**X3 R**	**X4 R**	**X5 R**	**Anode R**	**Total Power**
24	150,000	23.1	20.9	16.7	12.0	9.5	0.8	82.9
25	300,000	46.2	41.8	33.4	24.0	19.0	1.5	165.8
26	450,000	69.2	62.7	50.0	36.0	28.4	2.3	248.7

Tests: Switching losses – secondary resistors

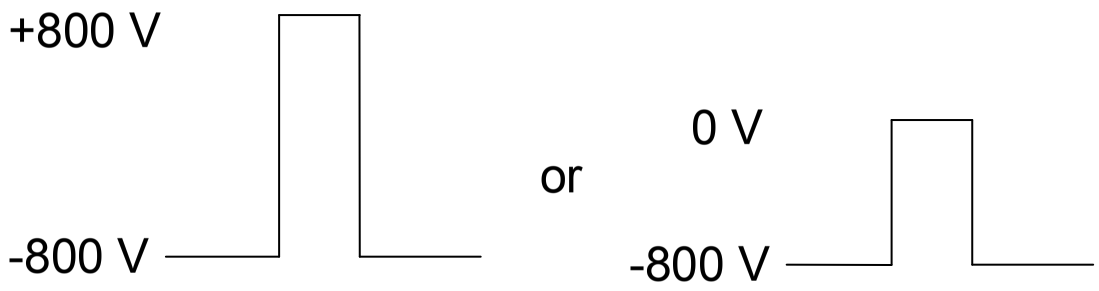
- What are FET I^2R losses delivering power to the secondary side resistors?
  - Modeling estimated 650 W worst case.
    - 800 Vdc primary
    - 450 kHz switch switching rate
    - 3 full cycle waveforms in each of the 3 bunch trains
  - Delivered power is shared by, roughly, four transformers.
    - Modeling reveals progressively lower power dissipation.
    - Parasitics of transformers is slightly different.
  - 650 / 4 = 163 (W) (ave.) delivered by each transformer.
  - 163 (W) / 800 (Vdc) = .20 (A) (ave.) in each H-bridge.
  - $(.20)^2$ (A)·4.2 (Ω) = .17 (W) ave. $I^2 \cdot R$ loss in each H-bridge

Design: Stacked transformer topology



Design: Anticipated drive mode

- New drive mode:



- Features:
  - Slightly less switching per cycle—no automatic step to 0V at the end of each 12-bunch cycle at time slot #17.
  - Allow the primary series capacitor to develop a voltage the automatically average the voltage waveform.
  - We do not attempt to reset the core by the end of each 12-bunch cycle.
  - Perhaps will simplify the waveform generating algorithm.

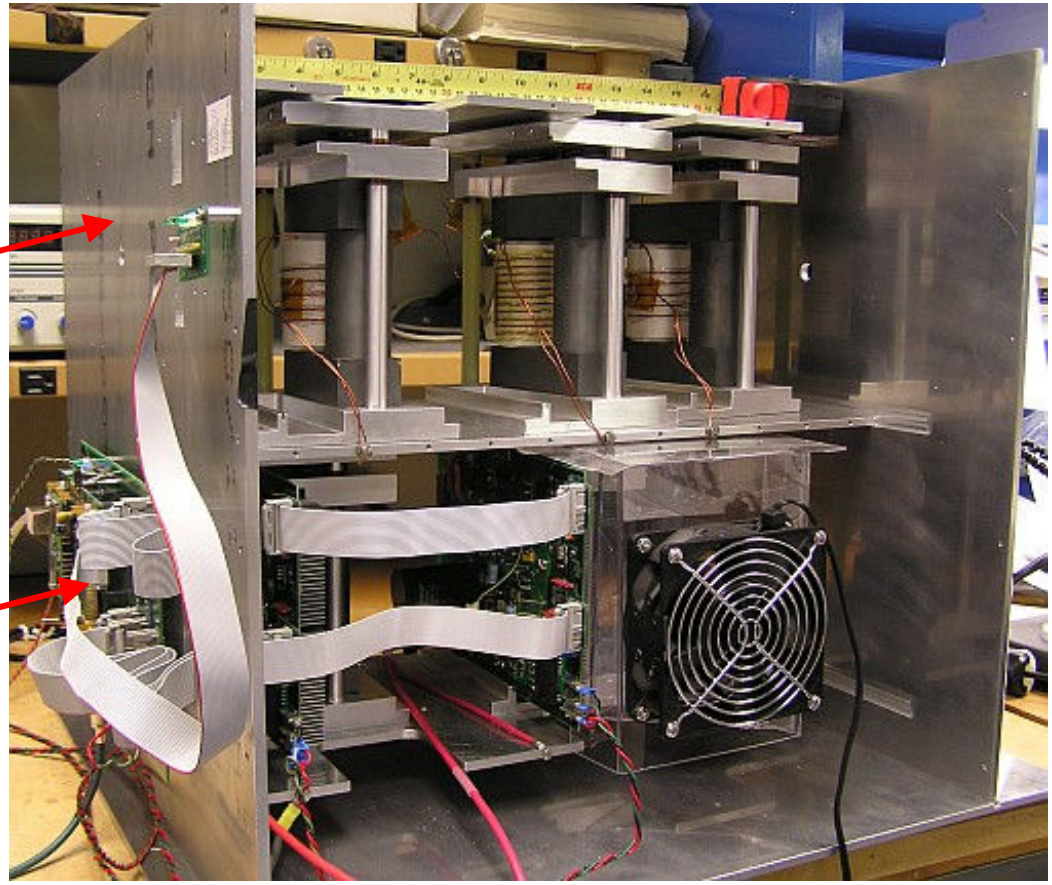
Design: Chassis

300 CFM forced air directed to these areas:

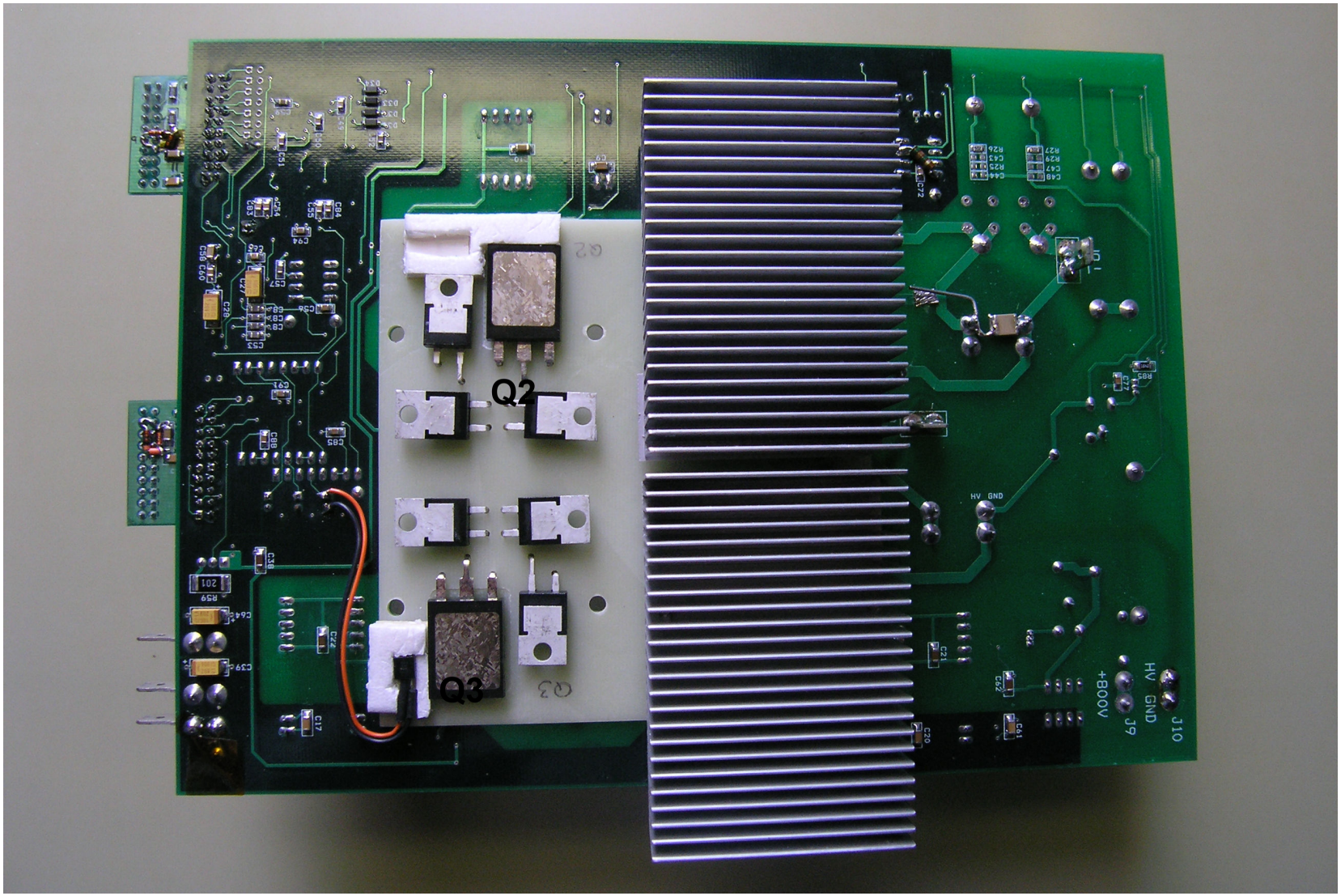
A. FETs. Switching losses total up to ~730 W worst case.
B. Transformer ferrite. Core losses total up to 300 W worst case.
C. Secondary side resistors. Estimated to be 650 W worst case.

Slave controller goes here

Master controller

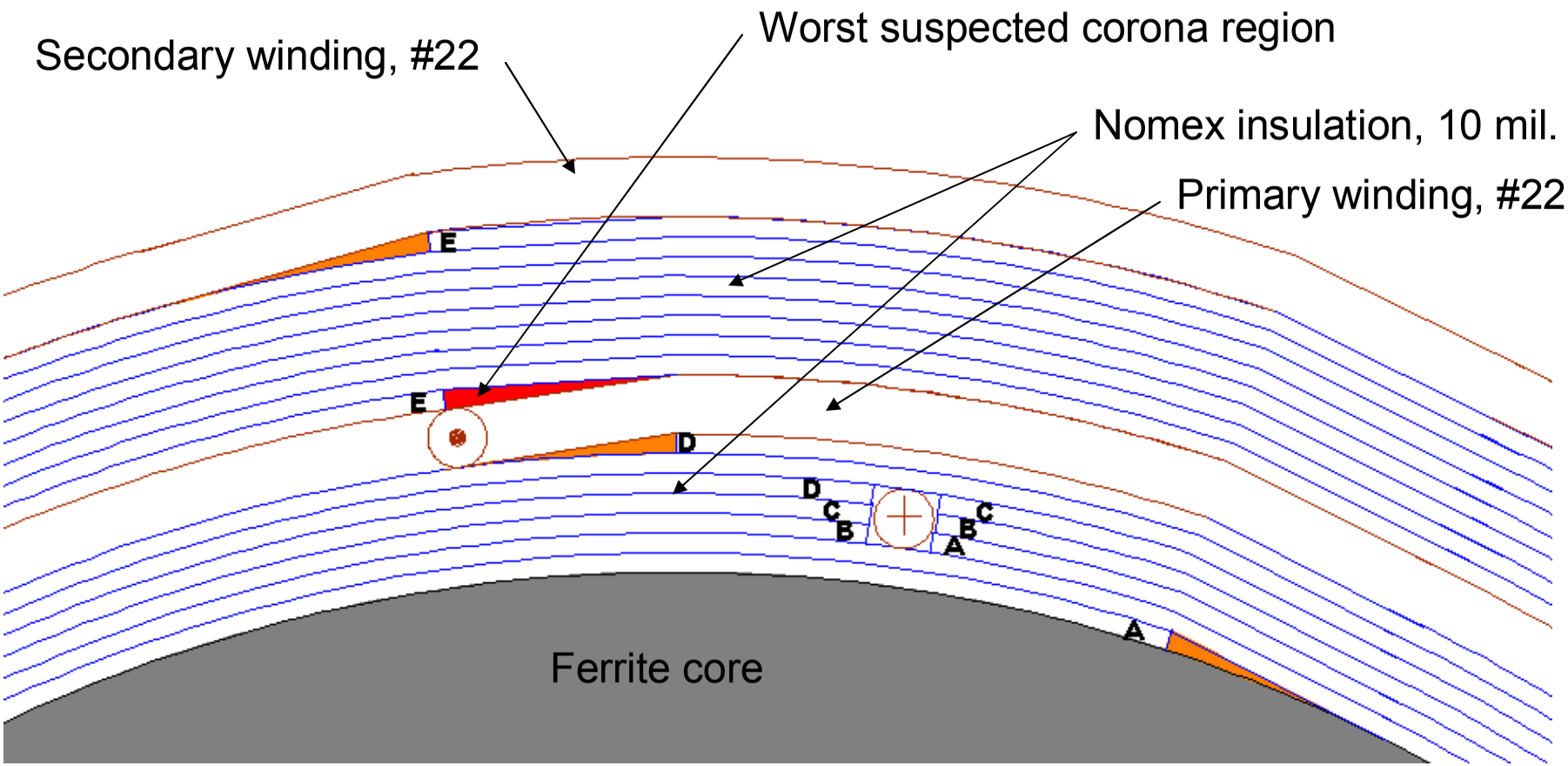


Design: Driver board assembly



Design: Core insulation & winding layering scheme

Corona extinction for 8 Nomex layers was 2900 Vrms.

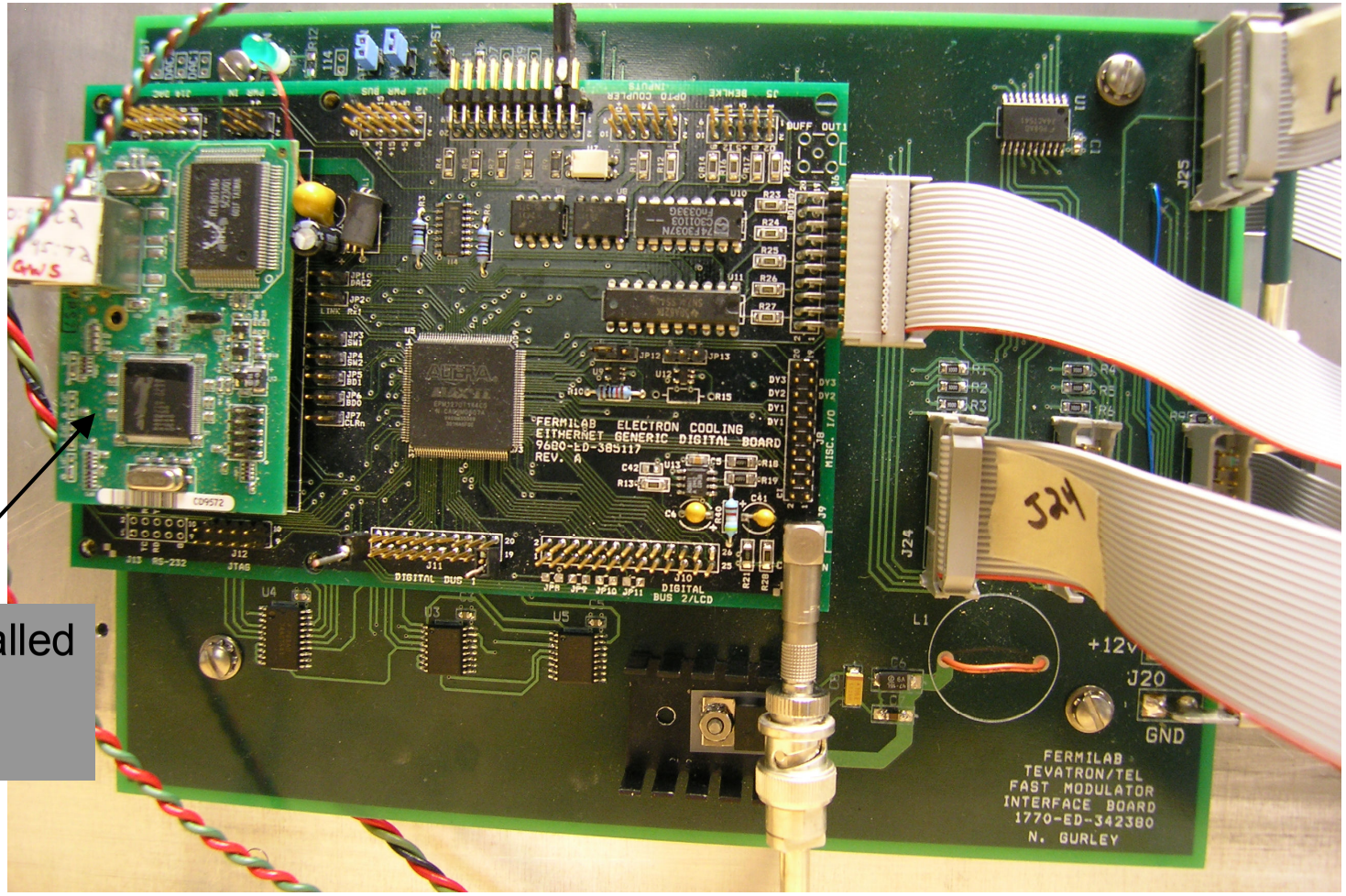


Design: Transformer construction

Transformer S/N	Lpri (mH)	Lleak (μH)	C (pF)	Corona kVrms	Truns Ratio	Nomex Layers
1	2.1	2.13	41.8	1.1	11:11	5
2	2.43	2.09	42.3	1.6	11:11	3
3	2.08	2.28	34	2.5	11:11	6
4	1.52	3.79	25.4	3.15	10:5	8
5	1.52	3.75	22.4	?	10:5	8
PCB corona test between 800 V traces:				1.6		

Design: Controller board

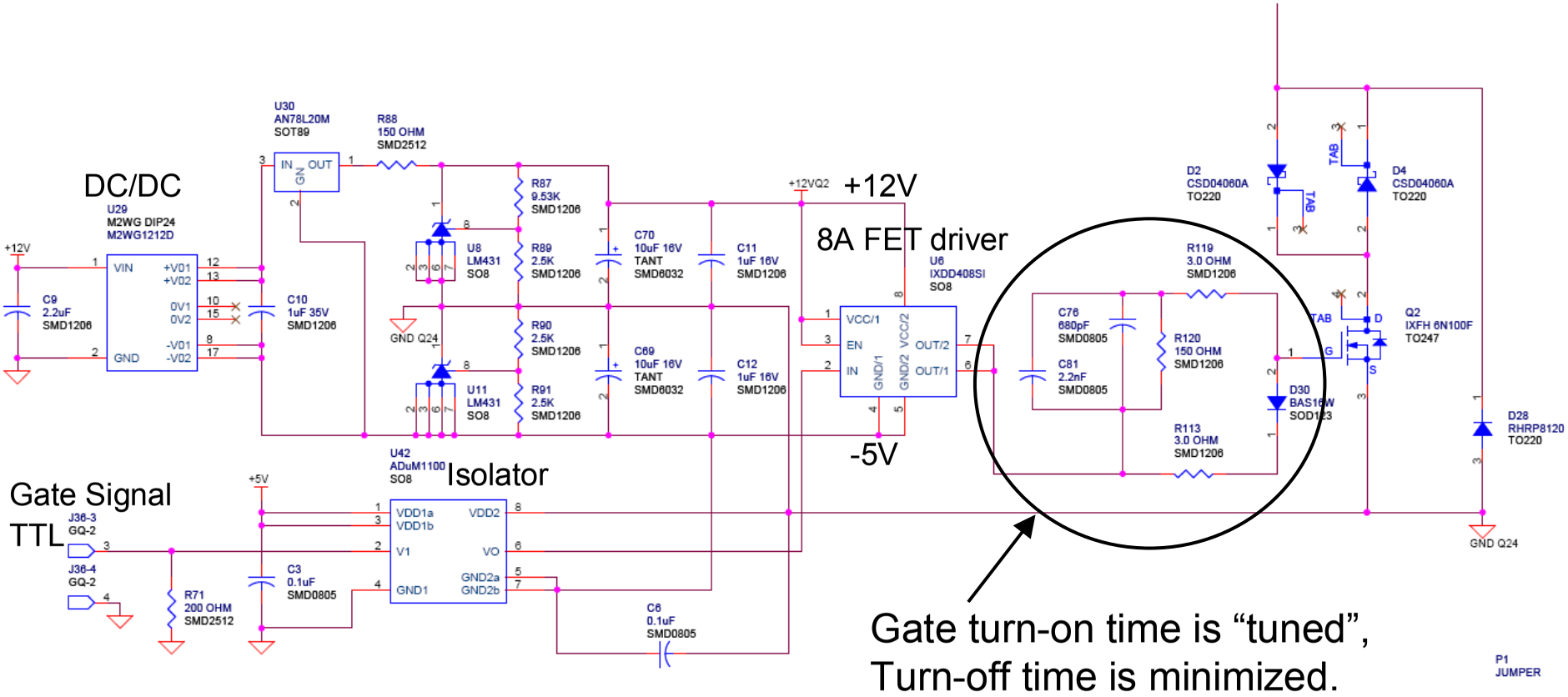
Two required to drive 5 transformers, a master and a slave. The master communicates with the ACNET front end over Ethernet.



CPU only installed on the master controller

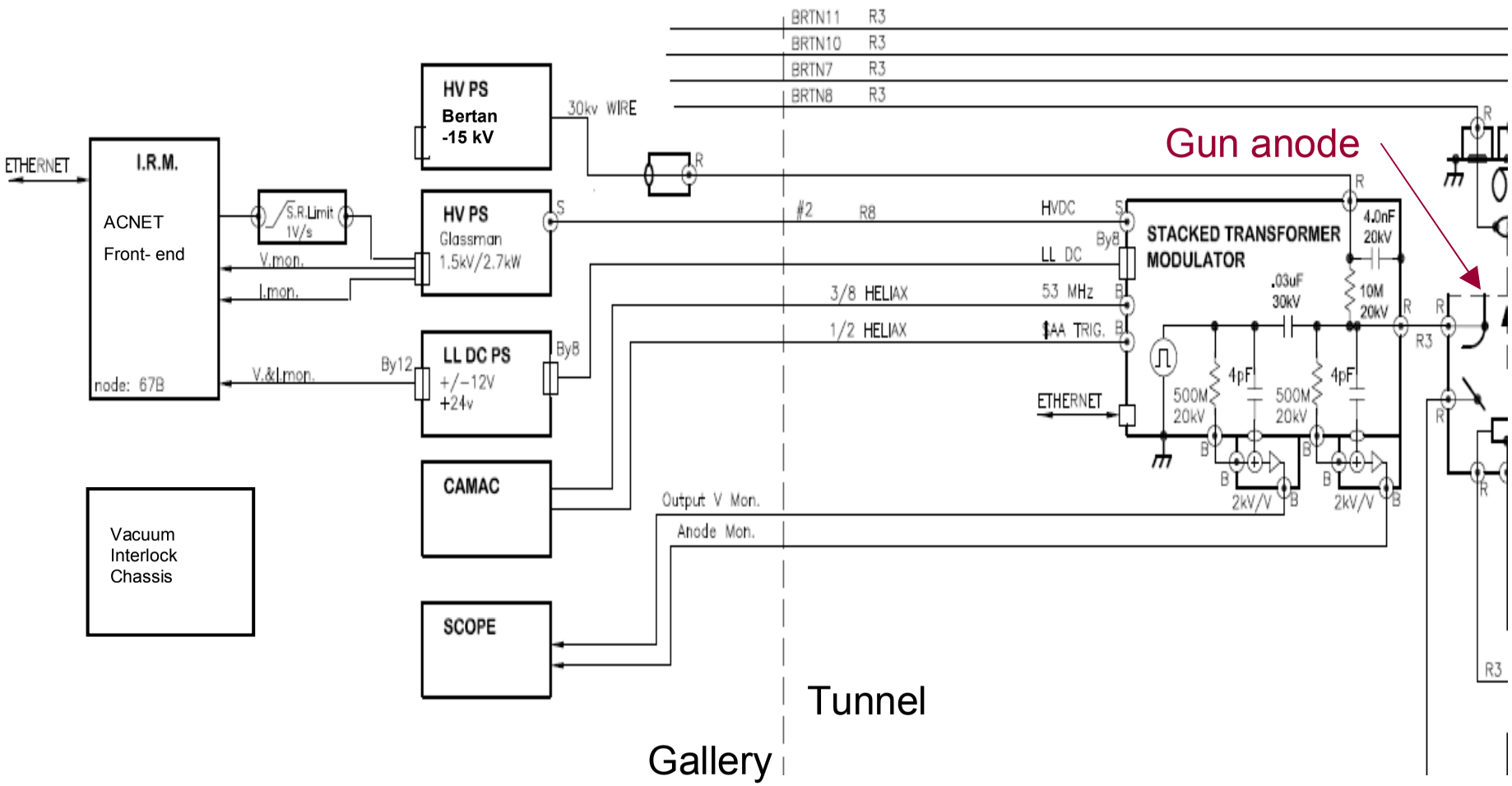
Design: FET gate drive circuit

- Gate driver circuit – typical of 4.
- FET gate drive network “tuned” to limit H-bridge to a 800V / 40ns max slew rate.
- 10-90% rise/fall time is 80ns.
- IXZR8N120 and IXTH3N100P both used and “tuned” for same response.

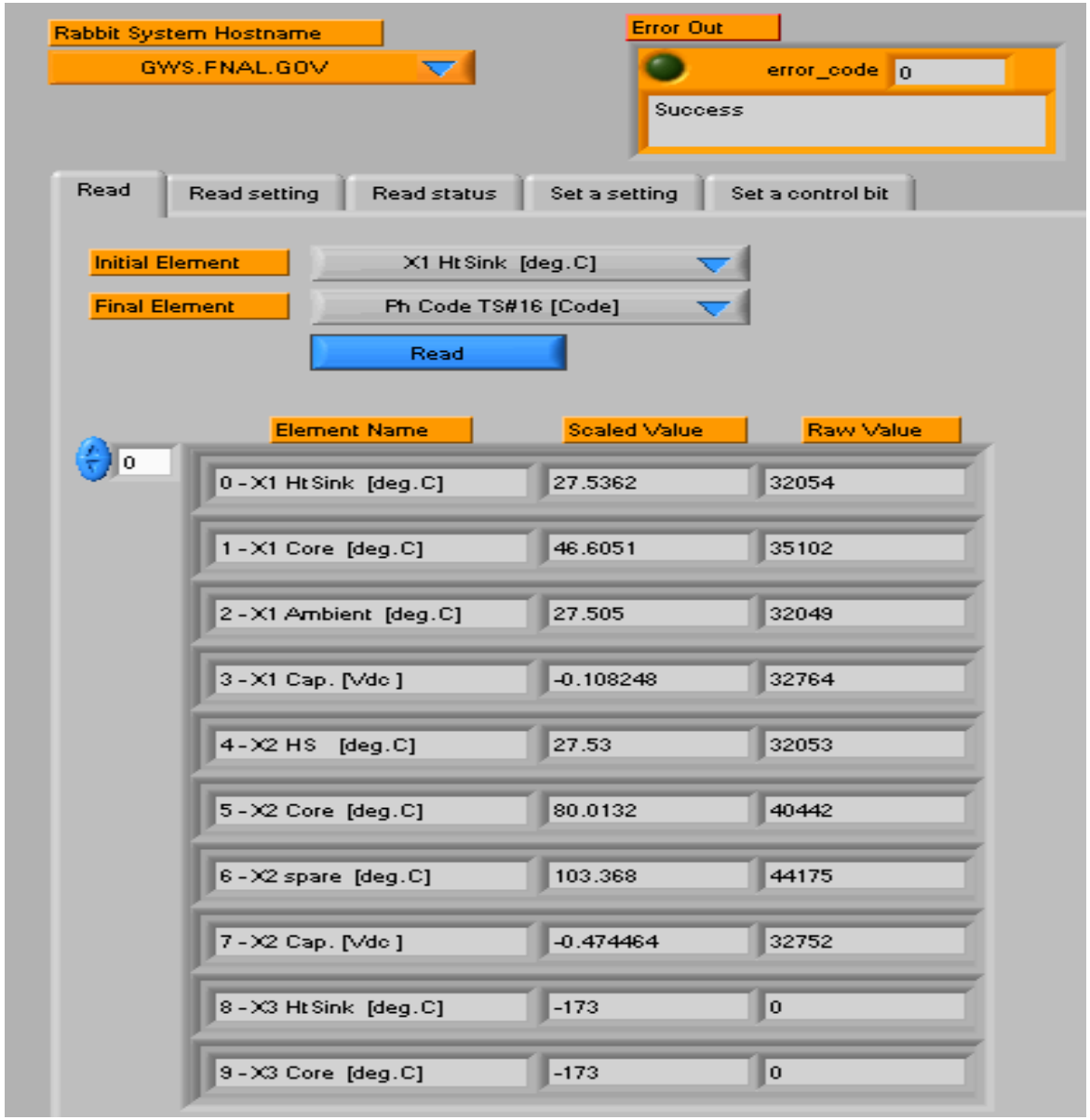


Gate turn-on time is “tuned”,
Turn-off time is minimized.

Design: Modulator system diagram – in TEL2



Design: LabView inerface



Design: LabView inerface

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Work remaining

- Controller
  - Update per new drive mode.
  - Update master for over current protection.
  - Configure the slave controller.
  - Include code to read back primary DC current.
- Chassis
  - Finish dwg's.
  - Machine remaining panels.
  - Finish kludging the primary DC current monitor PCB.
  - Finish assembly and wiring.
  - Debug 3 more driver boards.
- Additional hardware
  - Kludge a slew rate limiter circuit.
  - Kludge a buffer for the offset HV PS. (?)

Conclusion

- Operational testing shows the stacked transformer design topology will to work to enable tune shifting all 36 Tevatron bunches.
- Current design includes 5 transformers capable of producing 6.4 kVpp max.
- Tested performance shows we can run with 800 V primary voltage and switch at 450 kHz.
  - I would prefer not to run at max. voltage and max. switching rate on any one transformer due to FET power dissipation.
- Only corona will limit producing 6.4 kVpp.
- There remains several weeks of work to do, but hoping for August installation.