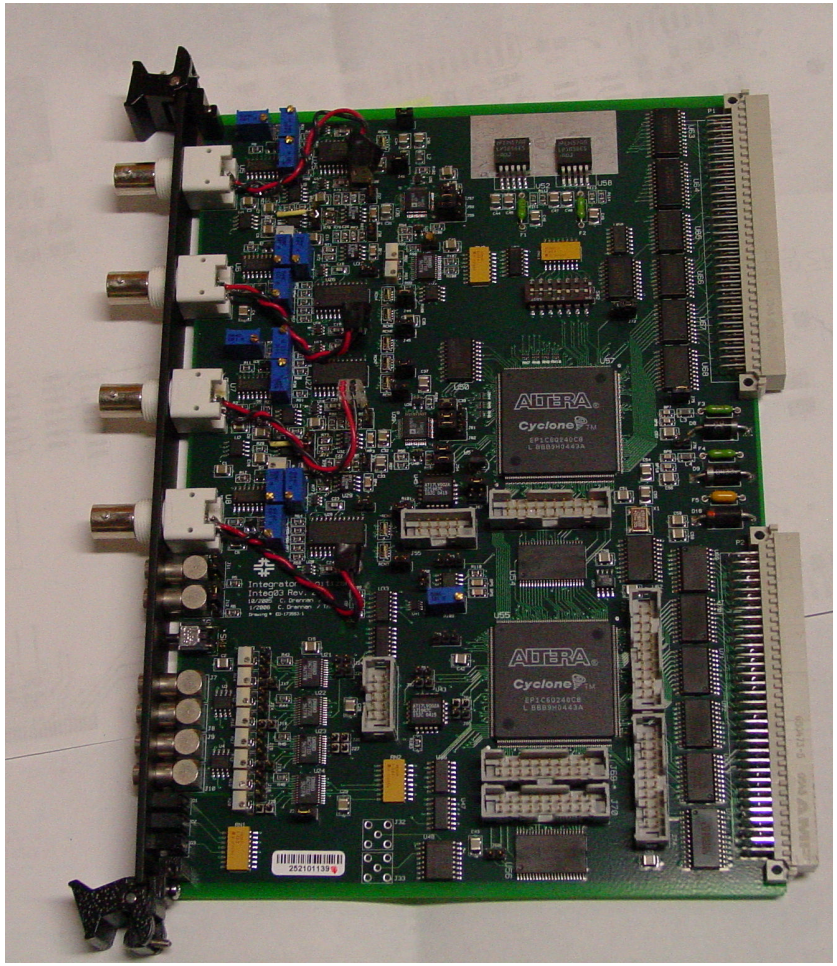
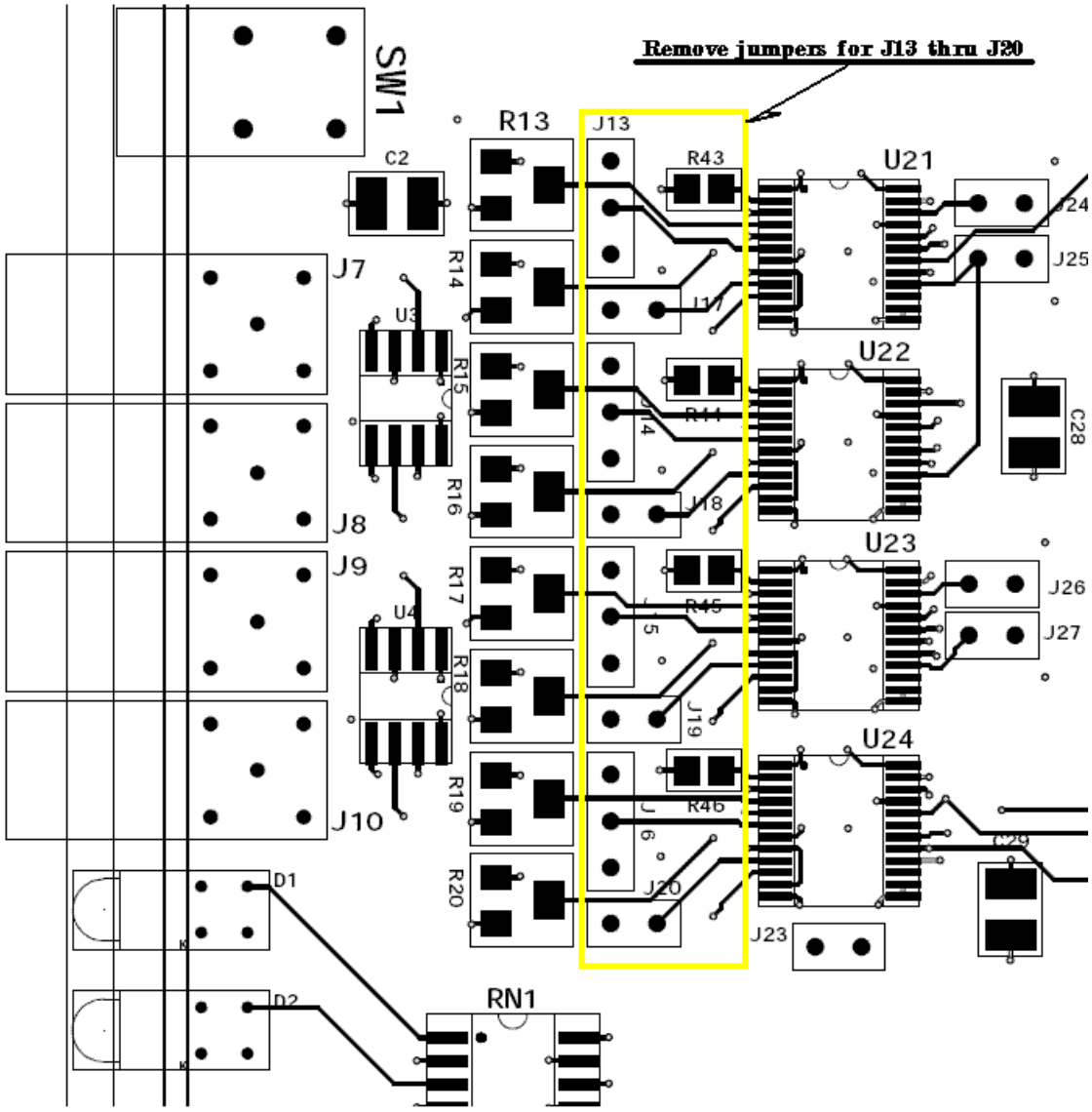
# BLM Integrator Notes -- Converting to the pulse stretcher application.



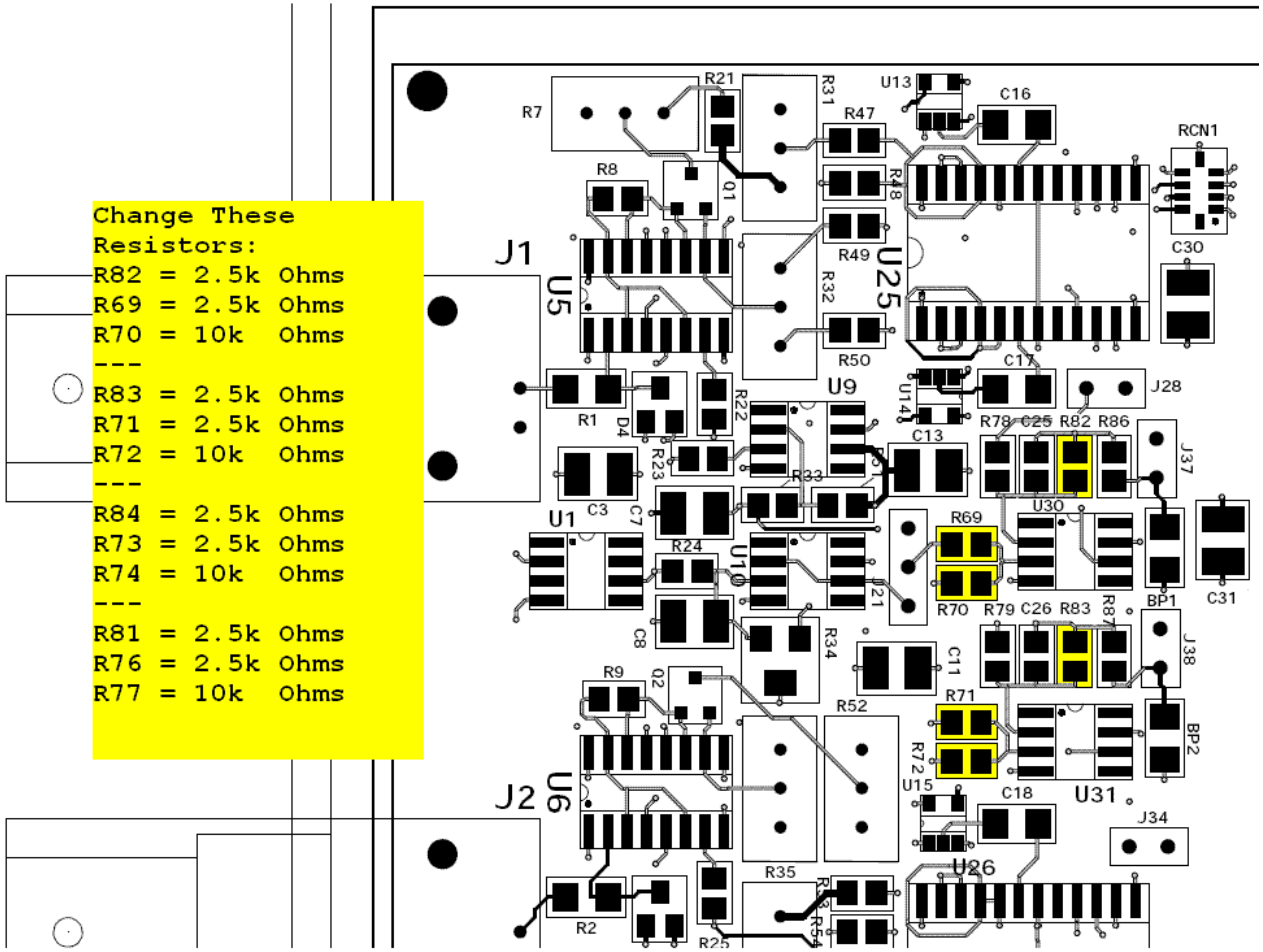
I. **Modifications to the Module.**

1. Remove all Jumpers from the DAC scaling selection pins, J13 thru J20.

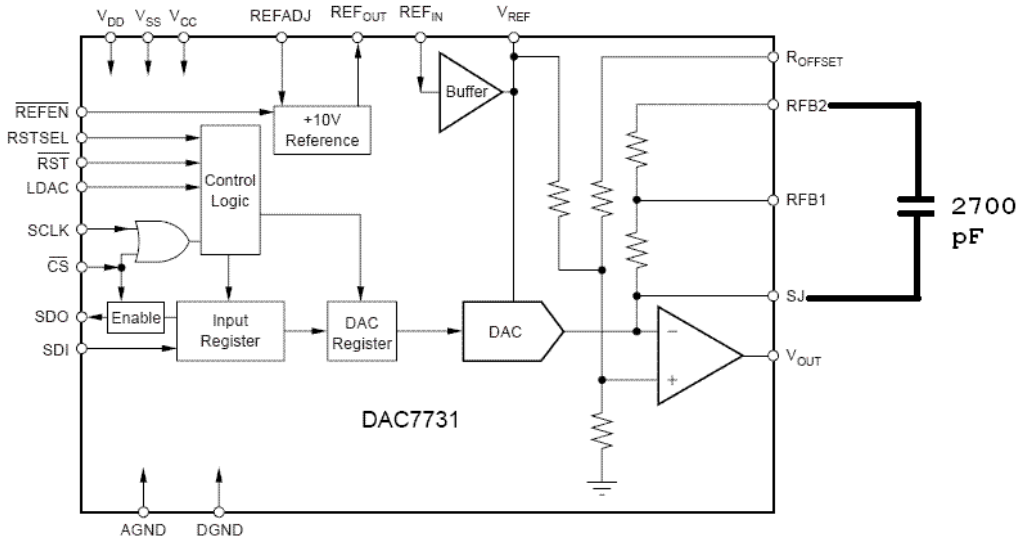


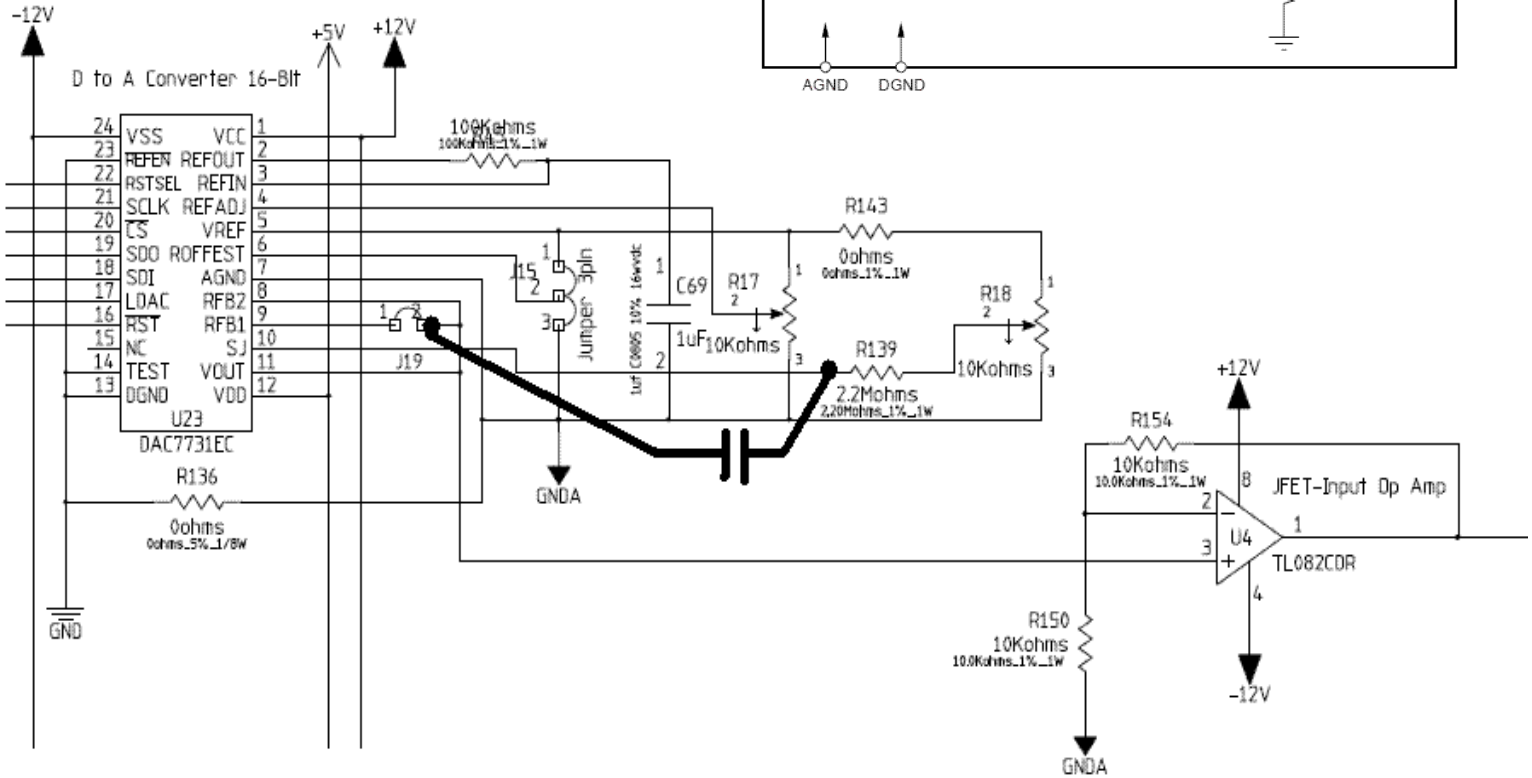
2. The ADC buffer is re-scaled to accept a +/- 10 Volt input. Inversion ( x(-1) ) is accomplished in the FPGA code. Change the following resistors.

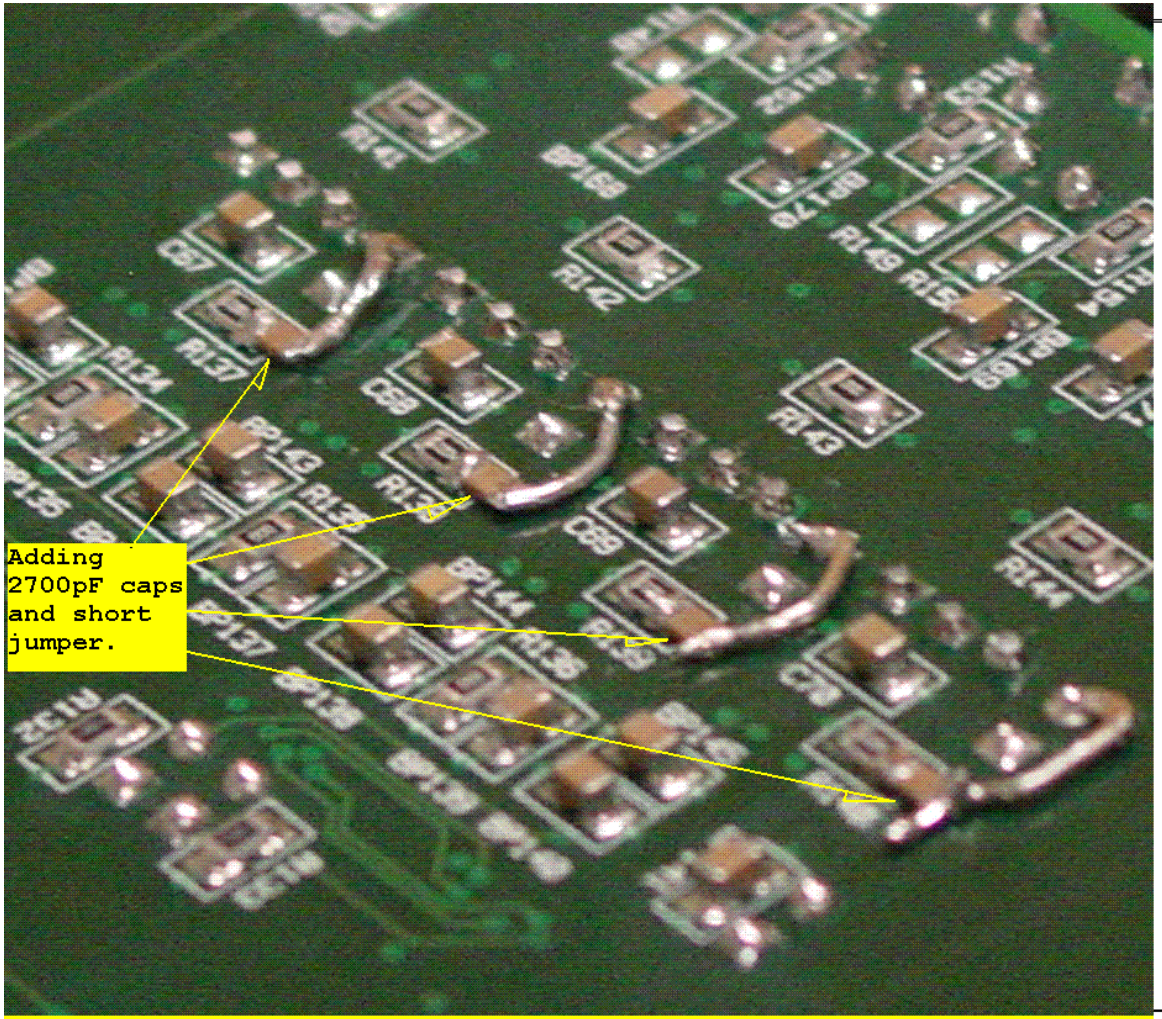
** Previous values for BLM application: R81 thru R84 = 4990, R69 and R73 = 6980, R71 and R76 = 10000, (R70, R72, R74, R77) = 4990.

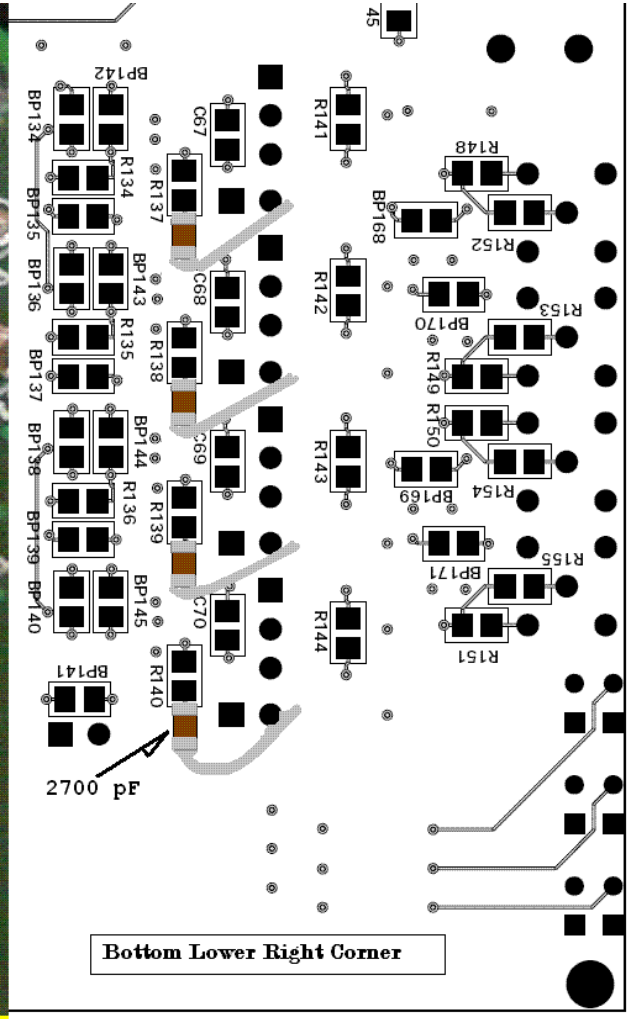


3. Capacitors (2700 pF) are added to the DAC's internal output buffers.

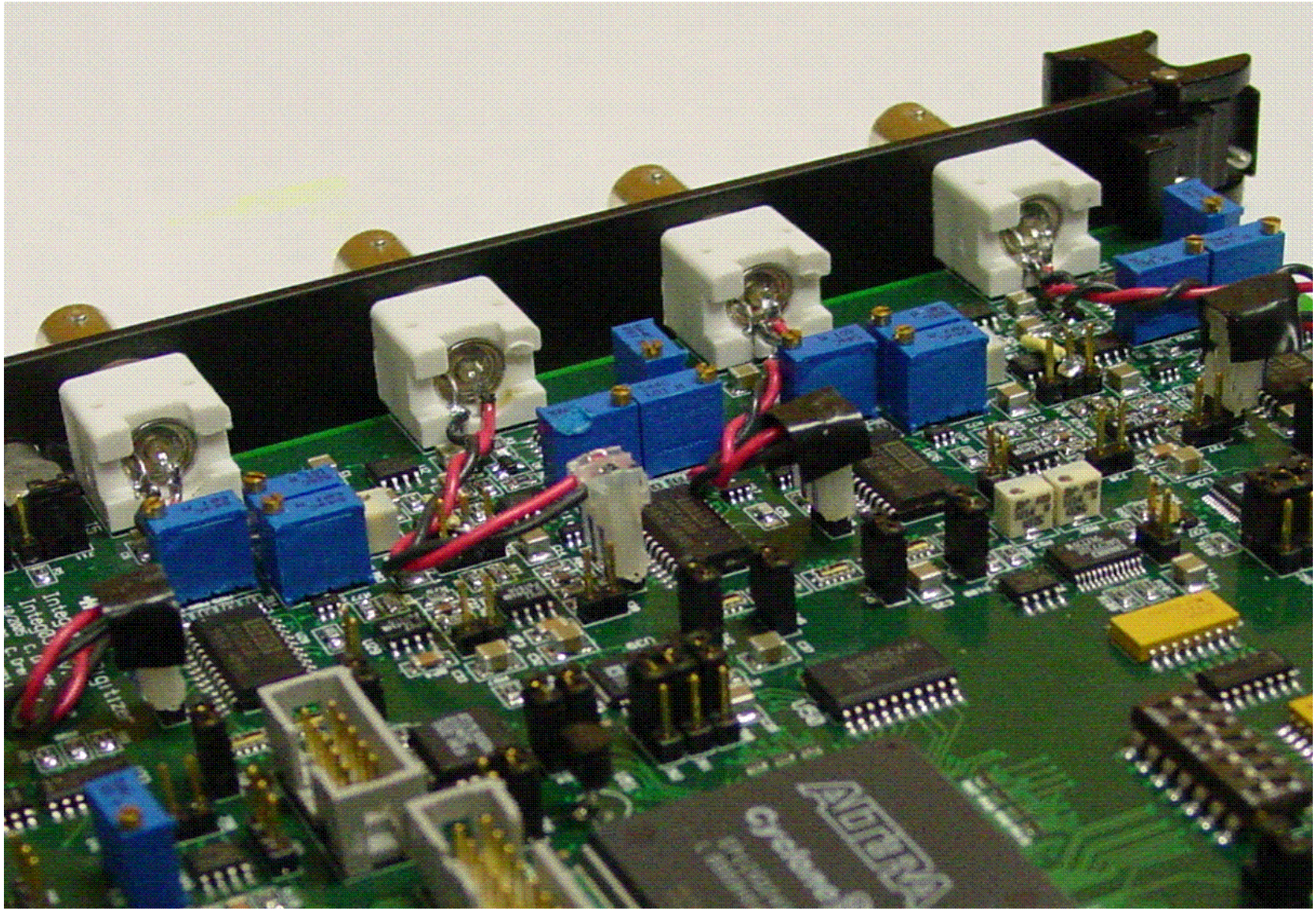


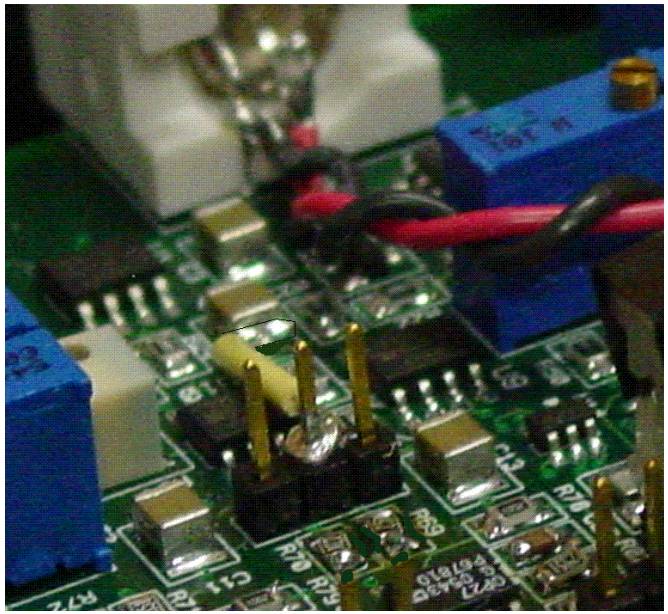

Adding
2700pF caps
and short
jumper.

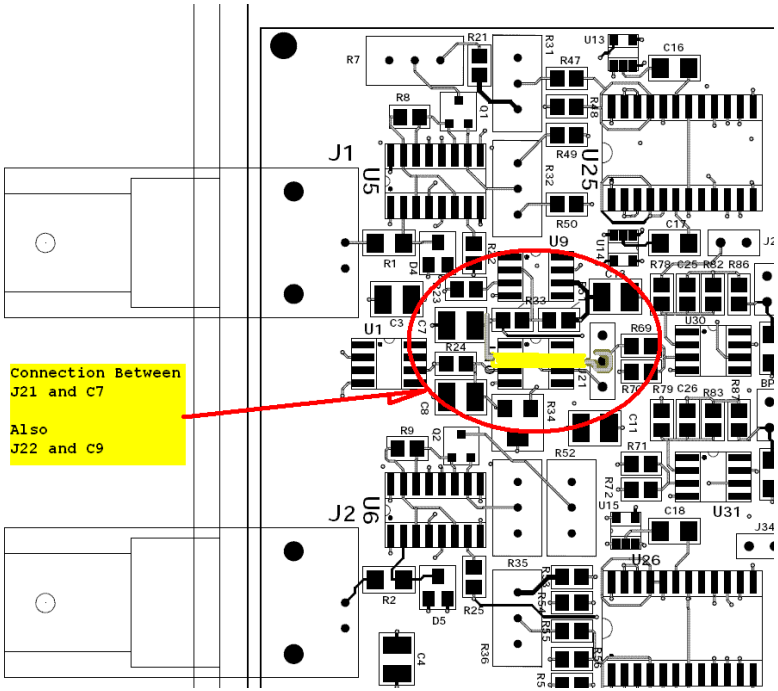

45
R141
R148
BP168
R152
R153
BP170
R149
R150
R154
BP169
R155
BP171
R151
R142
R143
R144
BP142
C67
R134
R137
BP134
BP135
BP136
C68
BP143
R135
R138
BP137
BP138
C69
BP144
R136
R139
BP139
BP140
C70
BP145
R140
BP141
2700 pF
Bottom Lower Right Corner

4. Jumper the input signal from the front panel BNC to the dual pin connections at J28, J29, J30, J31



5. Add jumper between the 2.5 Volt Reference output and the bias connections to the ADC buffer amps.






**Connections between J21/C7 and J22/C9.**

# Signal Connections for MP02

## *Comparator Threshold Input:*

B: TLVL02
CAMAC 052  DAC Voltage Output Module
Crate: $42
Slot: 9
Channel: DAC2

## *Trigger Input:*

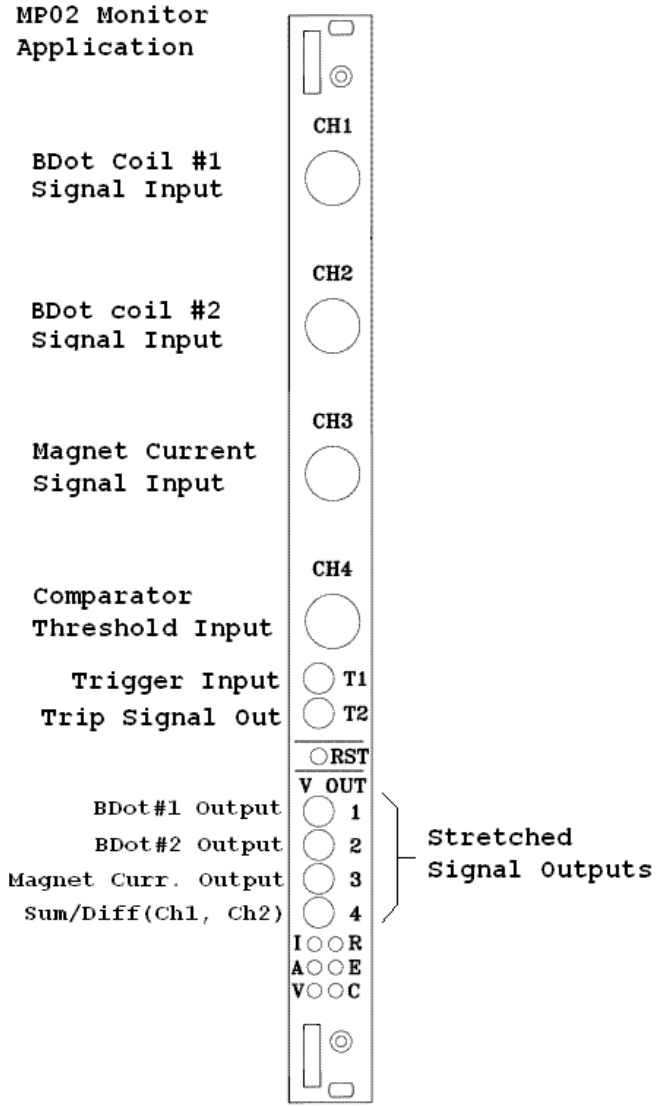
B: TDAQ02
CAMAC 177 Tclk Module
Crate: $41
Slot: 5
Channel: 4

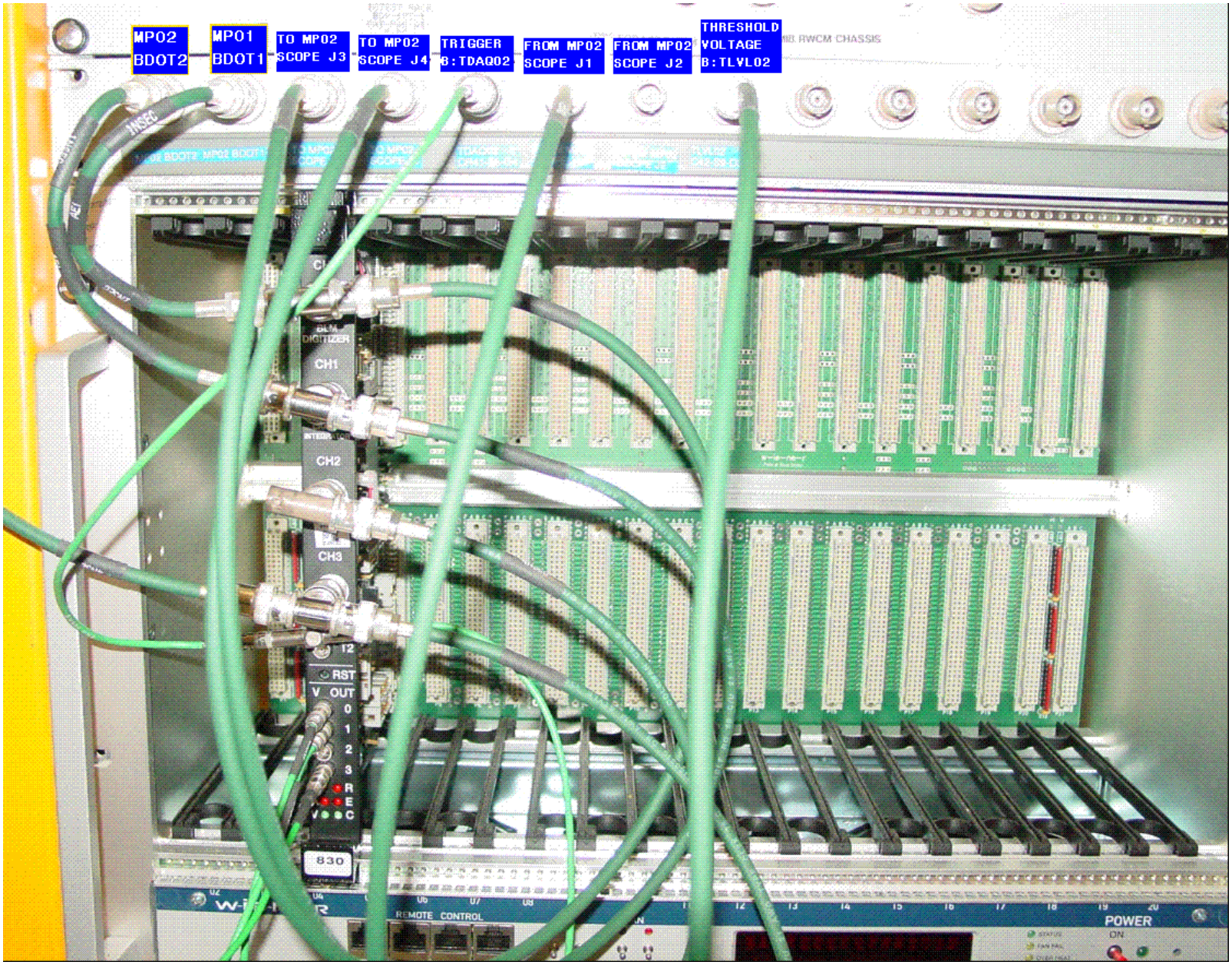
## *Signals Out:*

MADC#11
Crate: $40
Slot: 20

Channel:

| | | |
|---|---|---|
| 24 | B:BDQT1 | “Bdot Coil #1 stretched signal, MP02 (Bdot#1 Output)” |
| 25 | B:BDQT2 | “Bdot Coil #2 stretched signal, MP02 (Bdot#2 Output)” |
| 26 | B:IMP02 | “MP02 Load Current (Magnet Curr.  Output)” |
| 27 | B:DBDT12 | “Difference Between Bdot #1 and Bdot #2, MP02 (Sum/Diff)” |
| 28 | B:BDTTRP | “Difference beyond Threshold (sparking), MP02 (Trip Signal Out)” |






Crate Hookup in rack G01-RR6-3

II. Bill of Material 8/12/2008

The initial requirement for parts for 5 BLM to PS modification is the following

| Part Number - Part Description | Boards | Units/Brd | Total Units |
|---|---|---|---|
| RR12P2.55KDCT-ND - RES 2.55K OHM 1/10W .5% 0805 SMD | 5 | 8 | 40 |
| RR12P10.2KDCT-ND - RES 10.2K OHM 1/10W .5% 0805 SMD | 5 | 4 | 20 |
| PCC272BNCT-ND - CAP 2700PF 50V CERM CHIP 0805 | 5 | 4 | 20 |
| CE100F22-2 – 2 POSITION PCB PIN CONNECTORS | 5 | 4 | 20 |

III. FPGA Notes

1. SW5, SW6, SW7 are the front most dip switches near the VME J1 connector. These can be used to set different modes of operation. With [sw7,sw6,sw5] = 111 we can set the board into pulse stretcher mode.

2. Pulse stretcher mode sets the following

```
WHEN B"111" =>    -- "Reserved" (VME Bus Control, Test Enabled)
        Intg_CLK    = 20us_CLK;
        Run_Intg    = GND;
        Use_Const   = GND;
        Test_Enabled   = VCC;
        Use_Alt_ControlBus = VCC;
        INJ_TBT_TRIGx  = INJ_TBT_TRIG2;
        STDY_TBT_TRIGx = STDY_TBT_TRIG2;
        BypassInteg = VCC;  --<-- new signal
        Alt_GetADC  = 4us_CLK;    --<-- new signal

END CASE;
```

3. Added the Bypass integrator signal to control the integrator switches in the pulse stretcher mode.