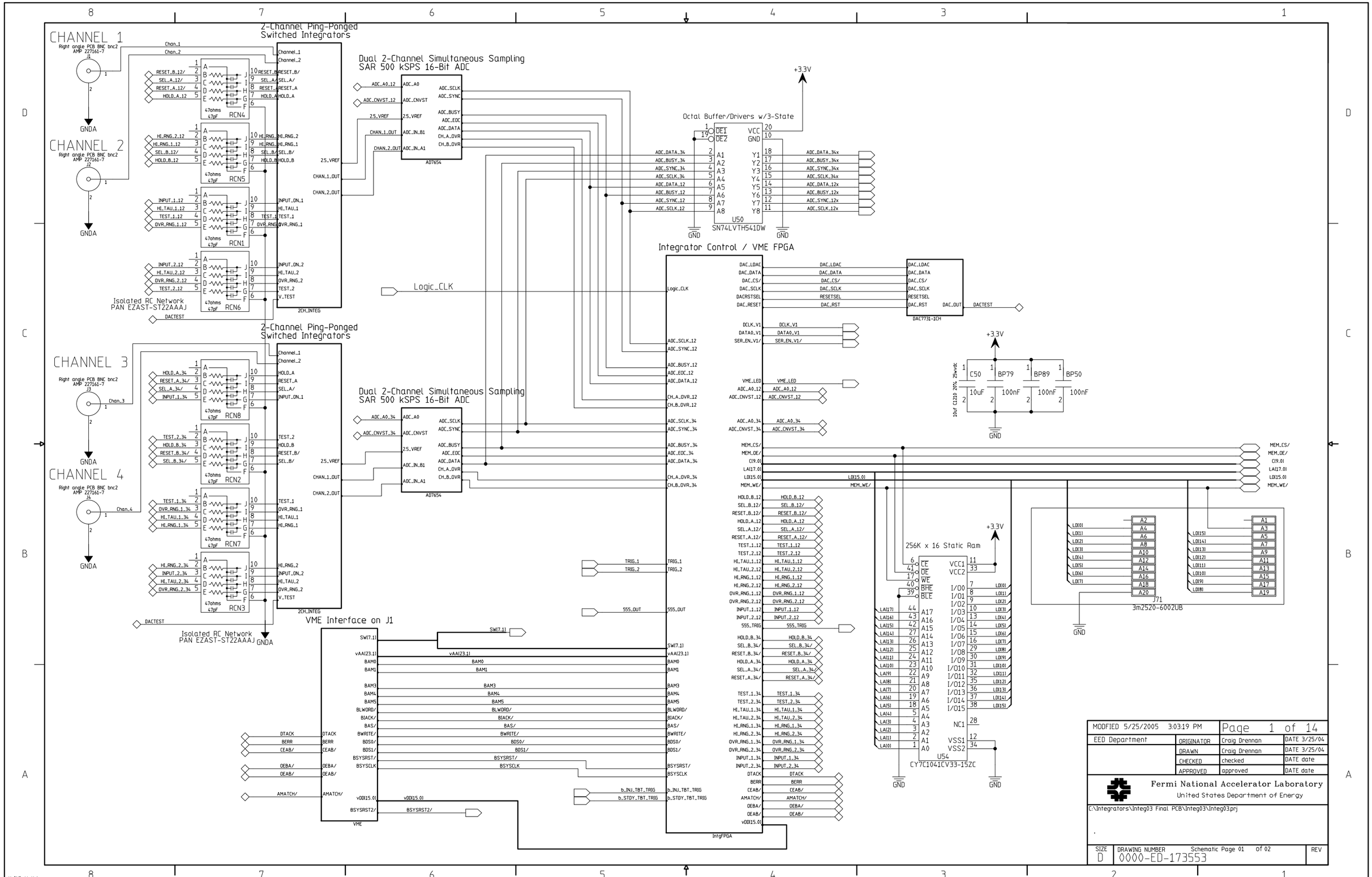

CHANNEL 1
Right angle PCB BNC bnc2
AMP 227161-7
J1
CHANNEL 2
J2
CHANNEL 3
J3
CHANNEL 4
J4
GNDA
2-Channel Ping-Ponged
Switched Integrators
Dual 2-Channel Simultaneous Sampling
SAR 500 kSPS 16-Bit ADC
AD7654
Isolated RC Network
PAN EZAST-ST22AAAJ
2CH_INTEG
Logic_CLK
Octal Buffer/Drivers w/3-State
U50
SN74LVTH541DW
+3.3V
GND
Integrator Control / VME FPGA
DAC7731-1CH
C50
BP79
BP89
BP50
10uF
100nF
256K x 16 Static Ram
U54
CY7C1041CV33-15ZC
J71
3m2520-6002UB
VME Interface on J1
VME
IntgFPGA
MODFIED 5/25/2005 3:03:19 PM
Page 1 of 14
EED Department
ORIGINATOR Craig Drennan DATE 3/25/04
DRAWN Craig Drennan DATE 3/25/04
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
C:\Integrators\Integ03 Final PCB\Integ03\Integ03.prj
SIZE D
DRAWING NUMBER 0000-ED-173553
Schematic Page 01 of 02
REV
H=8ND; V=4LA

BLM Control Bus FPGA

BLM Control Bus Connections on J2

Logic_CLK2
DCLK_V1
DATA0_V1
SER_EN_V1/
ADC_SCLK_12x
ADC_BUSY_12x
ADC_SYNC_12x
ADC_DATA_12x
PB_SW
ADC_SCLK_34x
ADC_BUSY_34x
ADC_SYNC_34x
ADC_DATA_34x
C[9.0]
MEM_CS/
MEM_OE/
LA[17.0]
LD[15.0]
MEM_WE/
SW[7.1]
BSYSRST2/
b_MAKE_MEAS
TRIG_1
TRIG_2
555_OUT
RECEIVE
DD[7.0]
AA[12.0]
b_Fast_LATCH0
b_Slow_LATCH1
b_VSlow_LATCH2
b_WR/
b_MEMRD/
b_MREQ/
b_GLOBAL_OSC
b_AIP
b_RESET_DC
b_RESET_SM
b_CPU_DETECT
b_Update
b_AbortCS5
b_AbortCS4
b_AbortCS3
b_AbortCS2
b_AbortCS1
b_AbortCS0
b_SPARE2
b_SPARE3
ENA_BUS_WR/
ENA_BUS_RD/
ABORT_CS/
ABORT0x/
ABORT1x/
ABORT2x/
ABORT3x/
ABORT4x/
CHAN_OK_OUT
ERROR
b_INJ_TBT_TRIG
b_STDY_TBT_TRIG
Logic_CLK
CtrlFPGA
CtrlBus

LED1
LED2
LED3
LED4
CNTRL_LED
DIG_OUT_1
DIG_OUT_2
VME_LED
CNTRL_LED
555_TRIG
TRANSMIT
PB_SW
TRIG_1
TRIG_2
RECEIVE
555_OUT
Board_10

MEMC_CS/
MEMC_OE/
LCA[17.0]
LCD[15.0]
MEMC_WE/
TRANSMIT
DD[7.0]
ENA_BUS_RD/
ENA_BUS_WR/
ABORT_CS/
ABORT0x/
ABORT1x/
ABORT2x/
ABORT3x/
ABORT4x/
DAC_SCLK_12
DAC_CS_12/
DAC_DATA_12
DAC_LDAC_12
DAC_SCLK_34
DAC_CS_34/
DAC_DATA_34
DAC_LDAC_34
WDTimer
CHAN_OK_OUT3/
ERROR

DAC7731
DAC_SCLK
DAC_CS/
DAC_DATA
DAC_LDAC

R128
10Kohms
Hex Inverter Buf/Driv w/O-C
U33
SN7406D
Out

Pin-Selectable Watchdog Timer
U41
MAX6373KA-T
VCC
WDO
SET2
SET1
WDI
GND
NC
SET0

256K x 16 Static Ram
U56
CY7C1041CV33-15ZC
CE
OE
WE
BHE
BLE
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
I/O9
I/O10
I/O11
I/O12
I/O13
I/O14
I/O15
NC1
VSS1
VSS2
VCC1
VCC2
+3.3V
GND

J70
J69
J68
3m2520-6002UB

C76
10uF
BP244
100nF
BP51
100nF
10uF C1210 20% 25wvdc

MODFIED 5/25/2005 3:03:19 PM		Page 2 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03.prj

SIZE D | DRAWING NUMBER 0000-ED-173553 | Schematic Page 02 of 02 | REV

H=8ND, V=4LA

Channel_1
R1 200ohms 200ohms_1%_.25W Res Thick Film 1206
-12V
+12V
D4 BAV199-PHILIPS
INPUT_ON_1
NO CMOS Analog SPST Switch
U5 MAX313CSE
IN1 IN2 COM1 COM2 NO1 NO2 V- V+ GND VL NO4 NO3 COM4 COM3 IN4 IN3
14.7Kohms R8 14.7Kohms_1%_.1W
HI_TAU_1
TEST_1
OVR_RNG_1
GNDA
V_TEST
R22 200Kohms 200Kohms_1%_.1W
Q1 MMBF4117
R21 20Kohms 20.0Kohms_1%_.1W
-2.5_VREF
R7 10Kohms 10Kohms Top Adj 25 turns 10% Bourns-3296-W-1-103
R32 100ohms 100ohms Top Adj 25 turns 10%
2.5_VREF
R31 10Kohms 10Kohms Top Adj 25 turns 10% Bourns-3296-W-1-103
R47 12.4Kohms 12.4Kohms_1%_.1W
R48 10ohms 10ohms_1%_.1W
SEL_B/
HOLD_B
RESET_B/
SEL_A/
HOLD_A
RESET_A
HI_RNG_1
+5V_ANALOG
MAX4514CUK-T
U14 U13 U16 U15
IN GND NO COM V+
NO Analog SPST Switch
0uf C1206 10% 25wvdc
0F C17 0F C16 0F C19 0F C18
Dual Switched Integrator
CAP IN SW-IN COM RESET HOLD SELECT SW-OUT SW-COM V+ V- OUT GND
U25 U26 ACF2101BU
R50 R49 R57 R54 0ohms 0ohms_1%_.1W
INTG_1_OUT
INTG_2_OUT
C63 C64 680pF 680pF C0805 5% 50wvdc
J28 J29
C25 C26 6pF 6pF C0805 5% 50wvdc
R82 R83 4.99Kohms 4.99Kohms_1%_.1W
OP AMP
U30 U31 OP-27GS
IN- IN+ BALa BALb V+ V- OUT
10Kohms R78 R79 10.0Kohms_1%_.1W
VBIAS
R69 R71 10Kohms 10.0Kohms_1%_.1W
R70 R72 4.99Kohms 4.99Kohms_1%_.1W
R86 R87 15ohms 15ohms_1%_.1W
BP1 BP2
10nF .01uf C1206 10% 50wvdc
J37 J38
CHAN_1_OUT
CHAN_2_OUT
Channel_2
R2 200ohms 200ohms_1%_.25W Res Thick Film 1206
D5 BAV199-PHILIPS
INPUT_ON_2
U6 MAX313CSE
R9 14.7Kohms 14.7Kohms_1%_.1W
HI_TAU_2
R25 200Kohms 200Kohms_1%_.1W
TEST_2
OVR_RNG_2
Q2 MMBF4117
R53 20Kohms 20.0Kohms_1%_.1W
R52 10Kohms 10Kohms Top Adj 25 turns 10% Bourns-3296-W-1-103
R35 100ohms 100ohms Top Adj 25 turns 10%
R36 10Kohms 10Kohms Top Adj 25 turns 10% Bourns-3296-W-1-103
R55 12.4Kohms 12.4Kohms_1%_.1W
R56 10ohms 10ohms_1%_.1W
HI_RNG_2
J34
R57 R54 0ohms 0ohms_1%_.1W
+5V
L1 Fair-Rite 2512066007Y0 Z=60ohms, DCR=0.2ohms, L1206
BP128 BP109 BP155 BP129 BP119 BP127 BP126 BP152 C34
100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 10uF
Precision Voltage Ref. 2.500V
U1 ADR291 Vin Vout GND
C3 10uF 10uf C1210 20% 25vdc
BP172 100nF
C7 10uF BP154 100nF
2.5_VREF
20Kohms R33 20.0Kohms_1%_.1W
R51 20Kohms 20.0Kohms_1%_.1W
R23 10Kohms 10.0Kohms_1%_.1W
U9 OP177FS TRIMa TRIMb
Ultraprecision OP AMP
-2.5_VREF
C13 10uF
R24 20Kohms 20.0Kohms_1%_.1W
C8 10uF
R34 10Kohms
U10 OP177FS
J21 Jumper 3pin
VBIAS
J43 J49 J44 J45
GND
C11 BP112 BP113 BP147 BP146 BP165 BP164
C30 BP123 BP161 BP120 BP150 BP153 BP122 BP111 BP160
10uF 100nF
HGND, V=4LA

MODIFIED 5/25/2005 2:45:33 PM		Page 9 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03prj

SIZE D | DRAWING NUMBER 0000-ED-173553 Schematic Page 01 of 01 | REV

Channel_1
R3
200ohms
200ohms 1% 25W
Res Thick Film 1206
-12V
+12V
D6
BAV199-PHILIPS
INPUT_ON_1
NO CMOS Analog SPST Switch
U7
MAX313CSE
14.7Kohms
R11
14.7Kohms_1%_1W
HI_TAU_1
V_TEST
R27
200Kohms
200Kohms_1%_1W
TEST_1
OVR_RNG_1
GNDA
R26
20Kohms
20Kohms_1%_1W
R10
10Kohms
10Kohms Top Adj 25 turns 10%
Bourns-3296-W-1-103
-2.5_VREF
2.5_VREF
R37
Bourns-3296-W-1-103
10Kohms Top Adj 25 turns 10%
R58
12.4Kohms
12.4Kohms_1%_1W
R59
10Kohms
10ohms
10ohms_1%_1W
MMBF4117
Q3
R38
100ohms
100ohms Top Adj 25 turns 10%
HI_RNG_1
MAX4514CUK-T
U18
NO Analog SPST Switch
0uf C1206 10% 25wvdc
0F C21
Dual Switched Integrator
R61
0ohms
0ohms_1%_1W
ACF2101BU
U27
+5V_ANALOG
INTG_1_OUT
C65
680pF
680pF C0805 5% 50wvdc
J30
10Kohms
R80
10Kohms_1%_1W
R73
10Kohms
10Kohms_1%_1W
VBIAS
R74
4.99Kohms
4.99Kohms_1%_1W
6pF
C27
6pf C0805 5% 50wvdc
R84
4.99Kohms
4.99Kohms_1%_1W
OP AMP
U32
OP-27GS
R88
15ohms
15ohms_1%_1W
BP3
J39
10nF
.01uf C1206 10% 50wvdc
CHAN_1_OUT
SEL_B/
HOLD_B
RESET_B/
SEL_A/
HOLD_A
RESET_A
U17
R60
0ohms
0ohms_1%_1W
INTG_1_OUT
U27
ACF2101BU
Dual Switched Integrator
Channel_2
R4
200ohms
200ohms 1% 25W
Res Thick Film 1206
D7
BAV199-PHILIPS
INPUT_ON_2
NO CMOS Analog SPST Switch
U8
MAX313CSE
14.7Kohms
R12
14.7Kohms_1%_1W
HI_TAU_2
R30
V_TEST
200Kohms
200Kohms_1%_1W
TEST_2
OVR_RNG_2
GNDA
R64
20Kohms
20Kohms_1%_1W
R63
10Kohms
10Kohms Top Adj 25 turns 10%
Bourns-3296-W-1-103
-2.5_VREF
2.5_VREF
R42
Bourns-3296-W-1-103
10Kohms Top Adj 25 turns 10%
R66
12.4Kohms
12.4Kohms_1%_1W
R67
10Kohms
10ohms
10ohms_1%_1W
MMBF4117
Q4
R41
100ohms
100ohms Top Adj 25 turns 10%
HI_RNG_2
MAX4514CUK-T
U20
NO Analog SPST Switch
0uf C1206 10% 25wvdc
0F C24
Dual Switched Integrator
R68
0ohms
0ohms_1%_1W
ACF2101BU
U28
+5V_ANALOG
INTG_2_OUT
C66
680pF
680pF C0805 5% 50wvdc
J31
10Kohms
R75
10Kohms_1%_1W
R76
10Kohms
10Kohms_1%_1W
VBIAS
R77
4.99Kohms
4.99Kohms_1%_1W
6pF
C22
6pf C0805 5% 50wvdc
R81
4.99Kohms
4.99Kohms_1%_1W
OP AMP
U29
OP-27GS
R85
15ohms
15ohms_1%_1W
BP4
J35
10nF
.01uf C1206 10% 50wvdc
CHAN_2_OUT
U19
R65
0ohms
0ohms_1%_1W
INTG_2_OUT
U28
ACF2101BU
Dual Switched Integrator
+5V
L2
Fair-Rite 2512066007Y0
Z=60ohms, DCR=0.2ohms, L1206
BP159
BP133
BP132
BP110
BP131
BP121
BP156
BP130
C36
100nF
10uF
Precision Voltage Ref. 2.500V
U2
ADR291
Vin
Vout
C5
10uF
BP173
100nF
C9
10uF
BP158
100nF
2.5_VREF
R62
20Kohms
20.0Kohms_1%_1W
R39
20Kohms
20.0Kohms_1%_1W
R28
10Kohms
10.0Kohms_1%_1W
U11
OP177FS
Ultraprecision OP AMP
-2.5_VREF
C14
10uF
J36
J46
J47
J48
J112
GND
J22
VBIAS
Jumper 3pin
R29
20Kohms
20.0Kohms_1%_1W
C10
10uF
R40
10Kohms
U12
OP177FS
Ultraprecision OP AMP
C12
BP115
BP166
BP148
BP116
BP167
BP149
C33
BP124
BP162
BP114
BP125
BP157
BP151
BP163
BP117
10uf C1210 20% 25wvdc
HGND, V=4LA

MODIFIED 5/25/2005 2:45:33 PM		Page 8 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03prj

SIZE D | DRAWING NUMBER 0000-ED-173553 | Schematic Page 01 of 01 | REV

AMP 650473-5
Conn 96pin VME RA PCB Male
3 x 32 Standard Size DIN 41612, Type C, Right Angle Pin Assy, PCB, Male.

P1

Octal Buffer/Drivers w/3-State
U65
SN74LVTH541DW

D-Type Latch, Octal, W/3-State
U61
SN74LVTH573DW
SN74LVTH573DW so20w

U66
SN74LVTH573DW
SN74LVTH573DW so20w

U67
SN74LVTH573DW
SN74LVTH573DW so20w

U68
SN74LVTH573DW
SN74LVTH573DW so20w

SN74LVTH543DW
U63
Octal Registered Transceiver

SN74LVTH543DW
U64
Octal Registered Transceiver

Quad 2-Input Positive-NAND Buf
U60
SN74S38D

Quad 2-Input Positive-NAND Buf
U60
SN74S38D

7 Position Dip Switch SMD
SW2
CTS-204-7ST

Bourns 4816P-T01-103

Jumper 3pin
J72

Fair-Rite 2512066007Y0
F5 3a
F4 1 AMP
F3 1 AMP

D10 1N5908
D9 1N6277
D8 1N6277

J76
J75

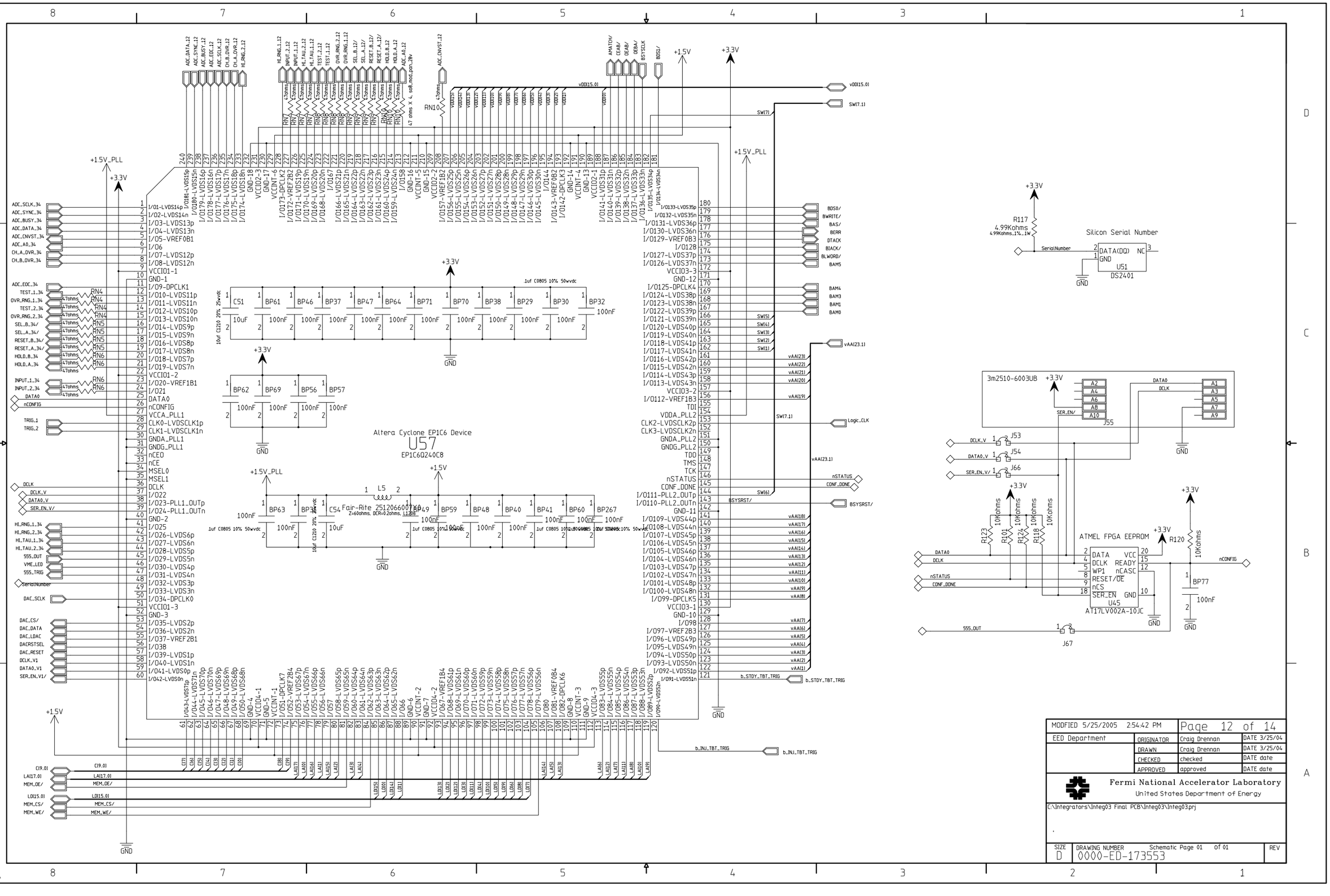
MODIFIED 5/25/2005 2:48:14 PM		Page 13 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03.prj

SIZE	DRAWING NUMBER	REV
D	0000-ED-173553 Schematic Page 01 of 01	

H=8ND; V=4LA



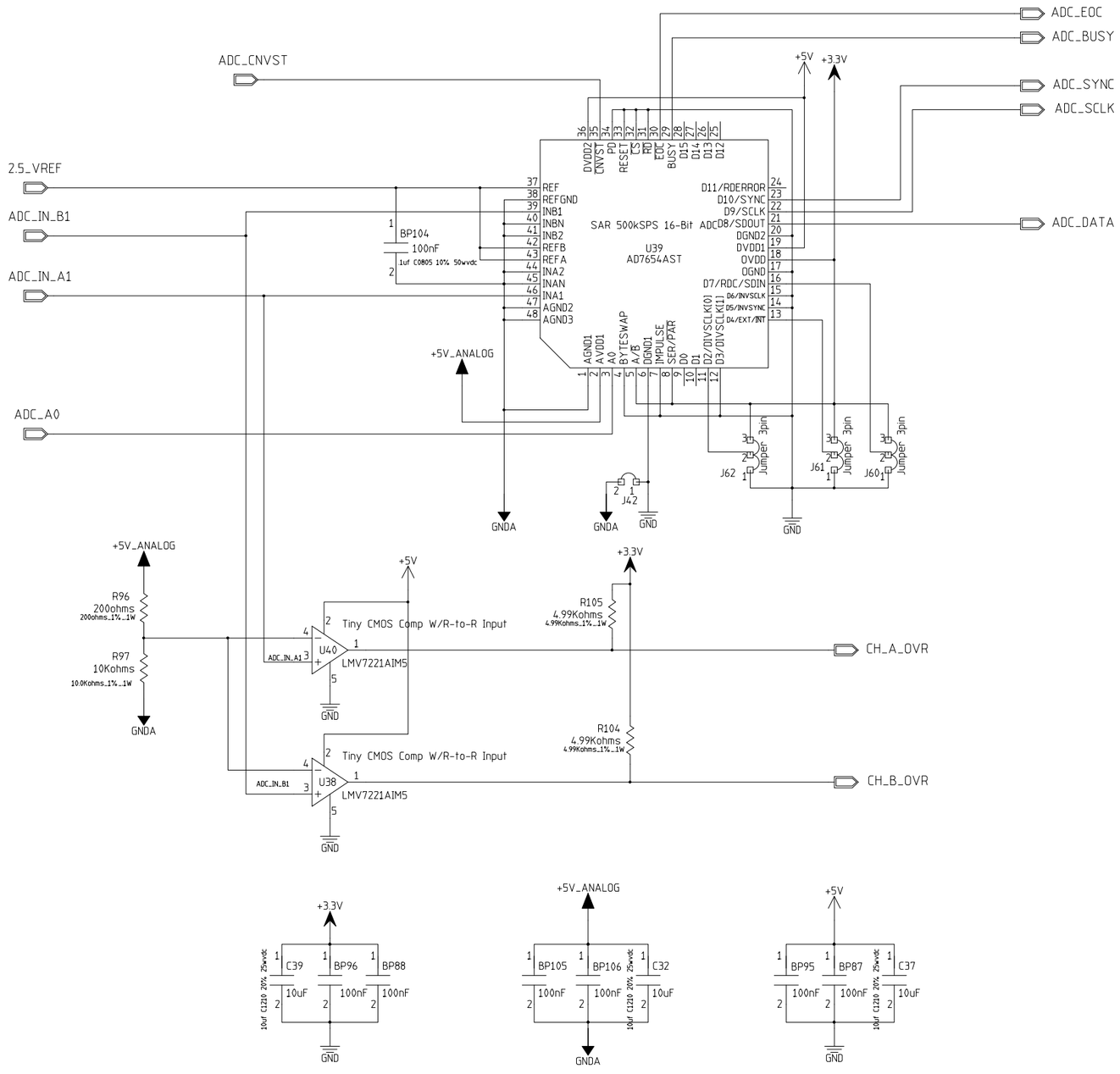
MODIFIED 5/25/2005 2:54:42 PM		Page 12 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03.prj

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	0000-ED-173553		

H=8ND; V=4LA



MODFIED 5/25/2005 2:46:47 PM		Page 11 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

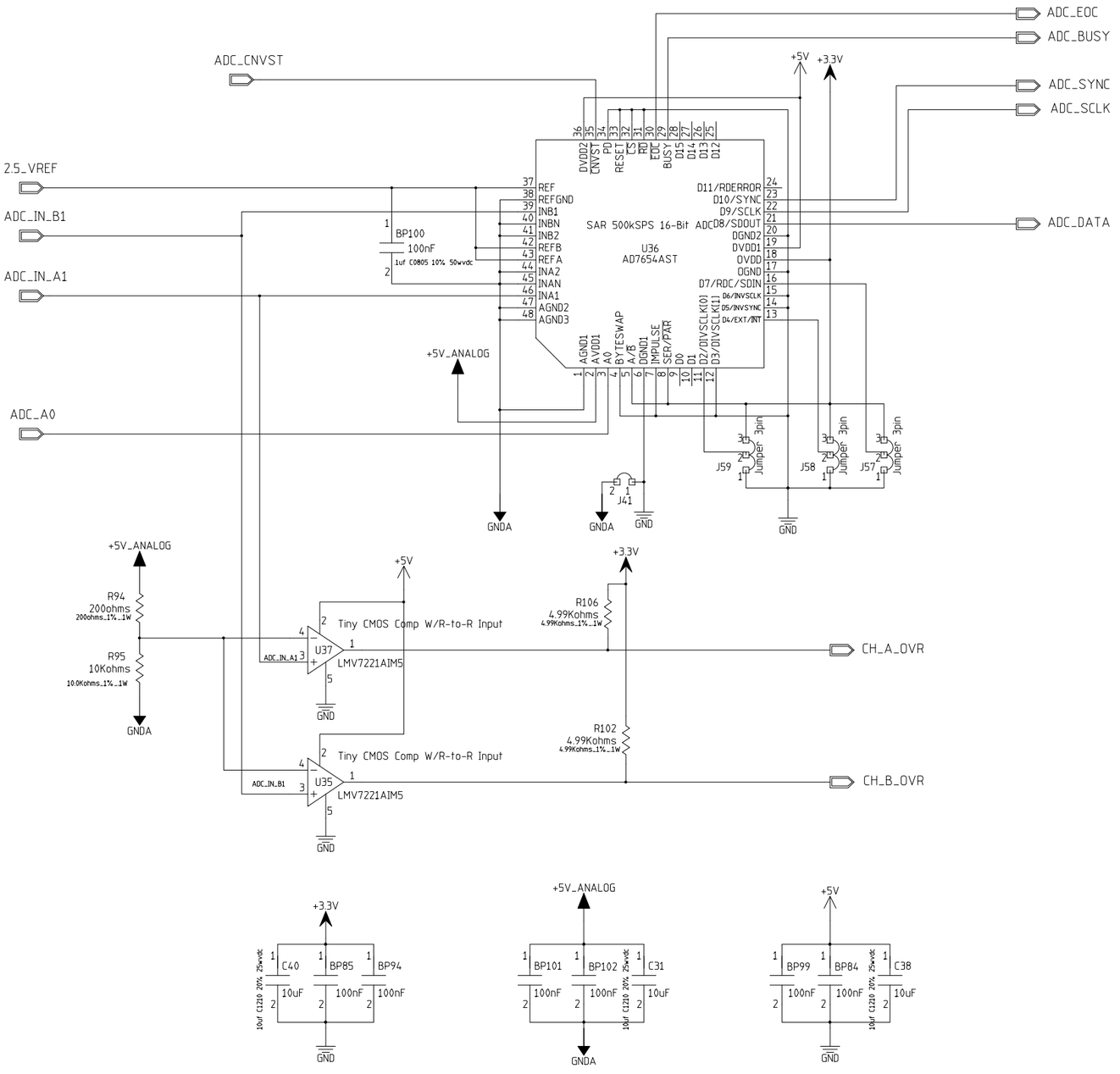
Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03.prj

.

SIZE	DRAWING NUMBER	REV
D	0000-ED-173553 Schematic Page 01 of 01	

H=8ND; V=4LA



MODFIED 5/25/2005 2:46:47 PM		Page 10 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

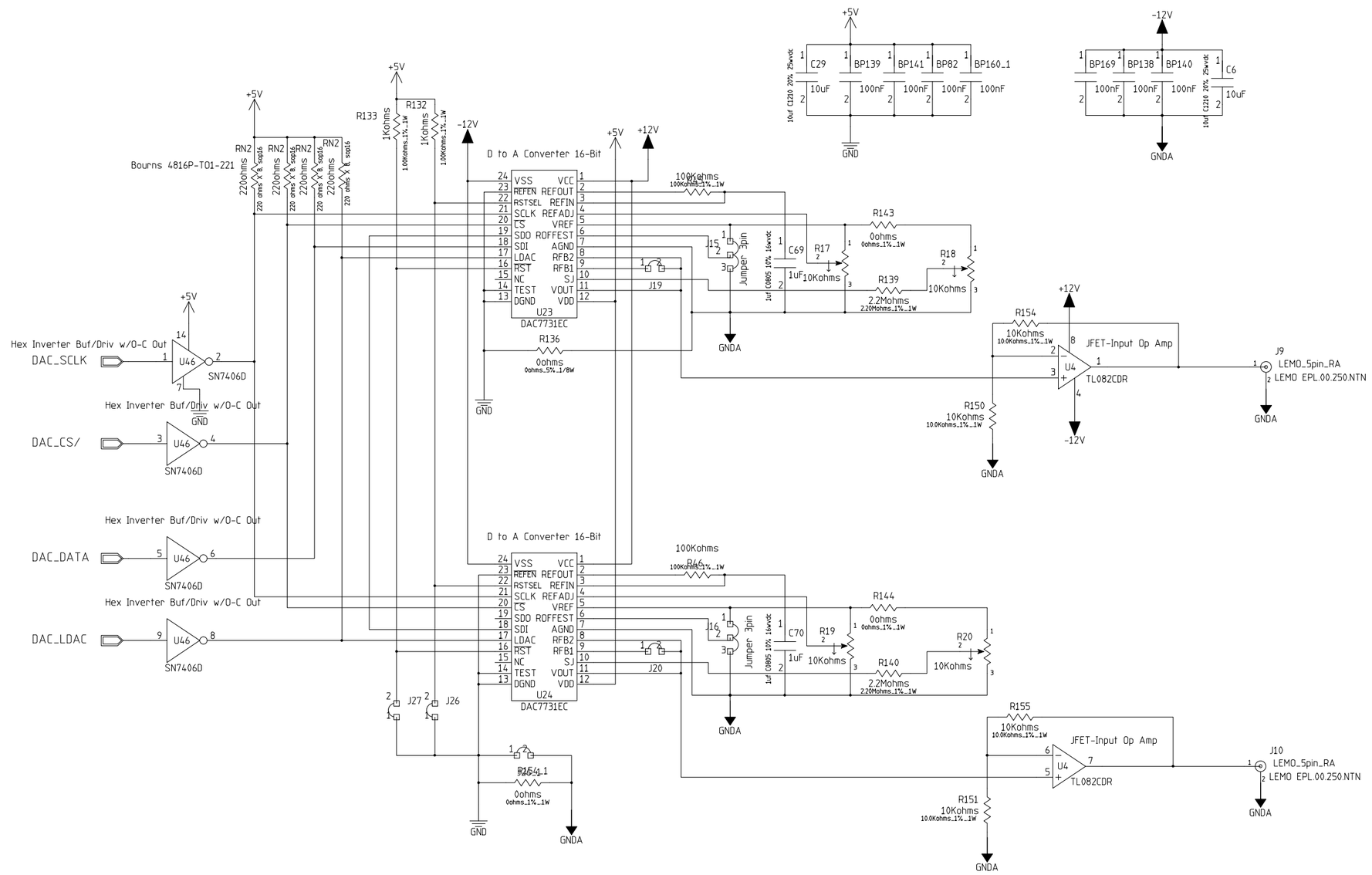
Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03.prj

.

SIZE	DRAWING NUMBER	REV
D	0000-ED-173553 Schematic Page 01 of 01	

H=8ND; V=4LA



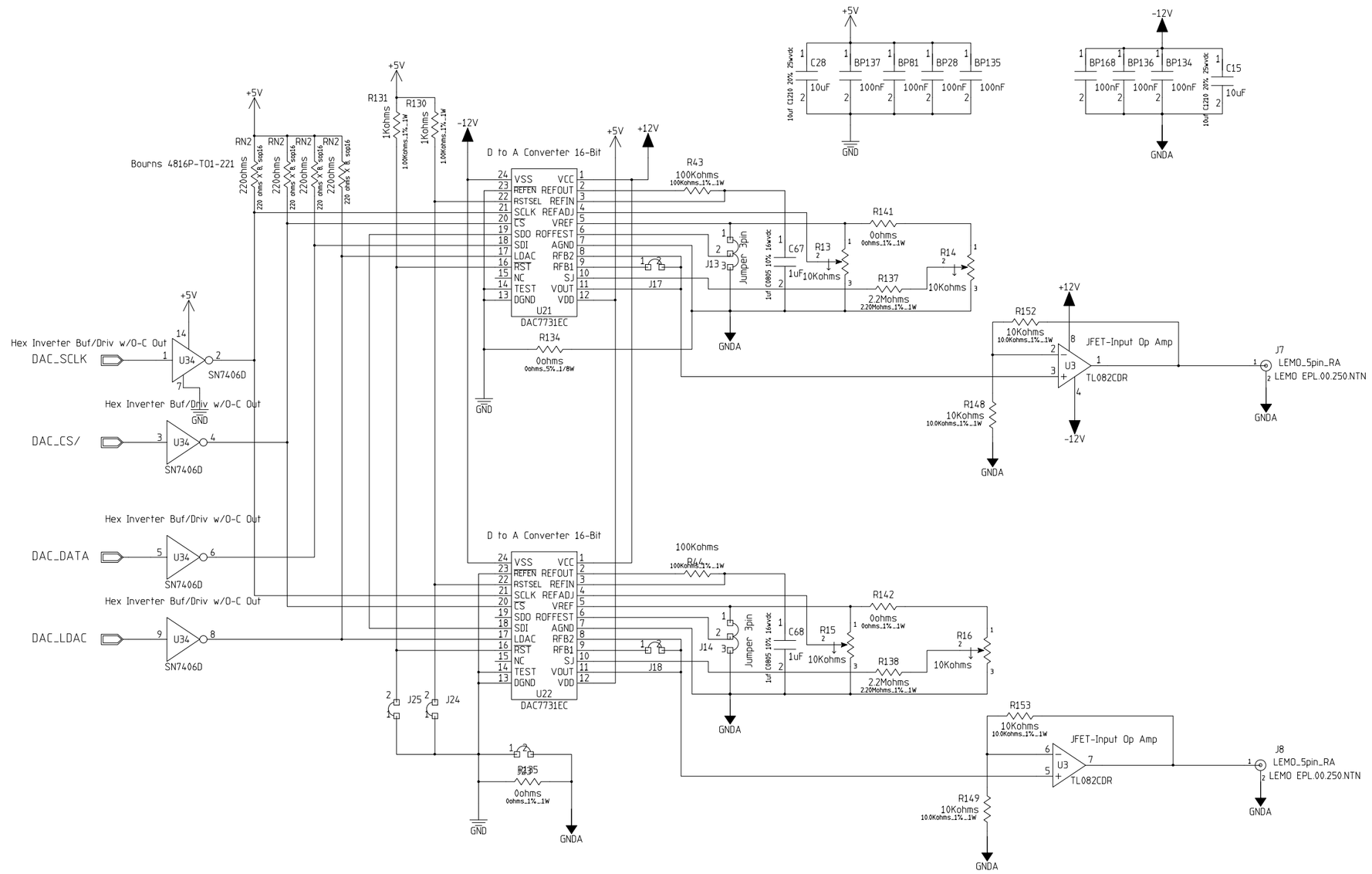
MODFIED 4/11/2005 1:08:34 PM		Page 7 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03.prj

SIZE	DRAWING NUMBER		REV
D	0000-ED-173553	Schematic Page 01 of 01	

H=8ND, V=4LA



MODFIED 4/11/2005 1:08:34 PM		Page 6 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03.prj

SIZE	DRAWING NUMBER	REV
D	0000-ED-173553 Schematic Page 01 of 01	

H=8ND; V=4LA

JUMPER BERG 3PINx2.54mm

TRANSMIT
J56
RECEIVE
GND

555_TRIG
J63
R119 10Kohms 10.0Kohms_1%_1W
J50 General Purpose Timer
+5V
R109 100ohms
100ohms Top Adj 25 turns 10%
R110 2.55Kohms 2.55Kohms_1%_1W
RESET VCC
TRIG OUT
THRES
CONT
DISCH GND
U49 ICM7555ISA
BP5 10nF
BP6 10nF .01uf C1206 10% 50wvdc
Hex Inverter Buf/Driv w/O-C Out
U33 SN7406D
R89 10Kohms
+3.3V
555_OUT

SPST Push Button Right Angle
ALCO TPA11CGRA0
SW1
R145 10Kohms
PB_SW

LED1
LED2
LED3
LED4
VME_LED
CNTRL_LED
Hex Inverter Buf/Driv w/O-C Out
U47 SN7406D
D1 Red DIALIGHT 553-0111
D2 Red DIALIGHT 553-0111
D3 Green DIALIGHT 553-0122
RN1 220ohms 220 ohms X 8, sop16
Bourns 4816P-T01-221

Quad 2-Input NAND Gate
DIG_OUT_1
DIG_OUT_2
U48 N74F3037D
J33 TYCO D-607-10 PCB Terminator
J32 TYCO D-607-10 PCB Terminator

BP97 BP118 BP98 100nF
C43 10uF 10uf C1210 20% 25wvdc
BP80 BP108 BP107 BP83 100nF 100nF 1uf C0805 10% 50wvdc

LEMO EPL.00.250.NTN
LEMO_5pin_RA
J5
J6
J11
J12
R147 10Kohms
R146 10Kohms
R90 10Kohms
R91 10Kohms
R6 511ohms
R5 511ohms
10.0Kohms_1%_1W
511ohms_1%_1W
U33 SN7406D
TRIG_1
TRIG_2

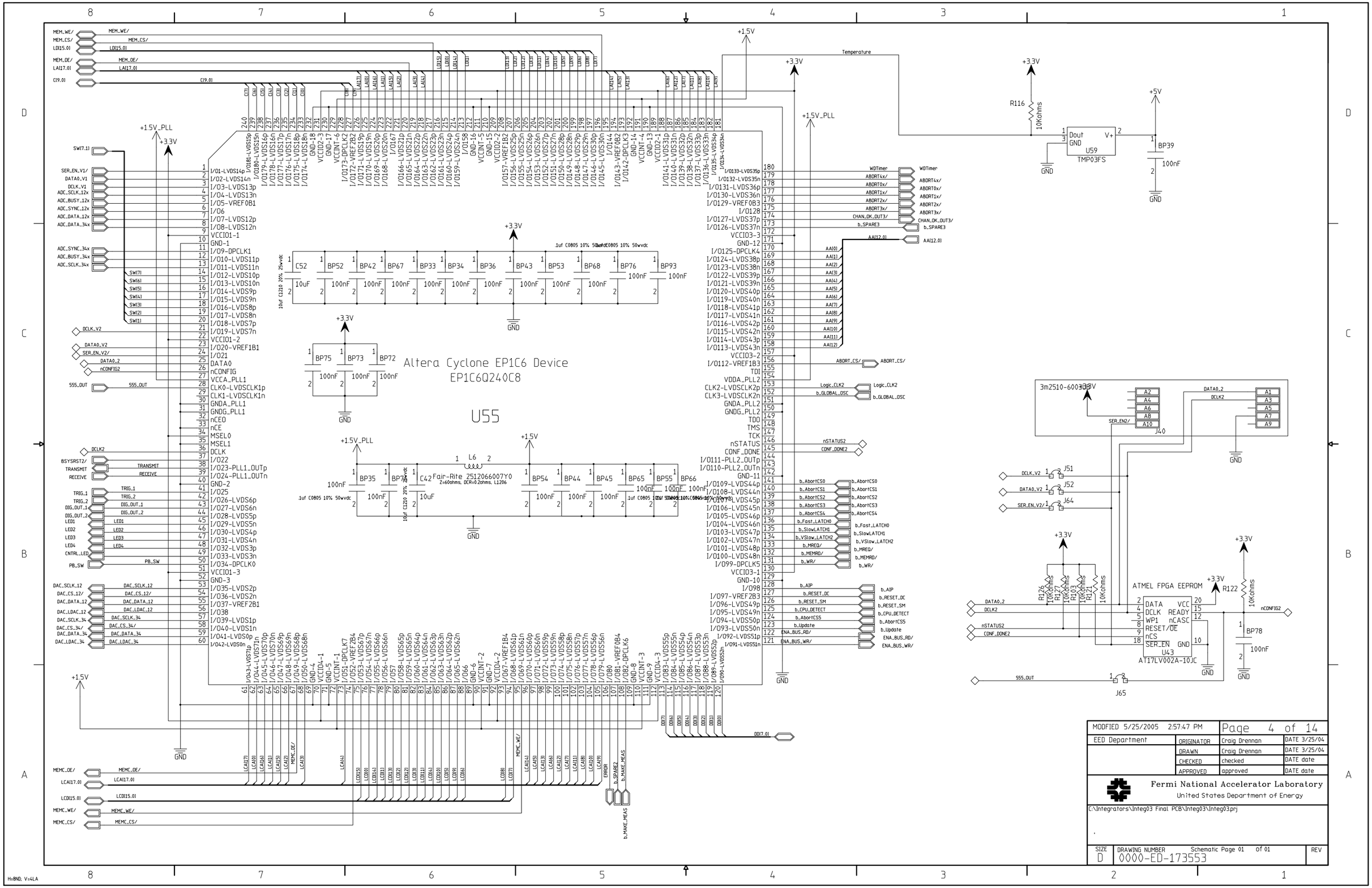
MODIFIED 5/25/2005 3:02:49 PM		Page 5 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03.prj

SIZE	DRAWING NUMBER	REV
C	0000-ED-173553 Schematic Page 01 of 01	

H=4ND; V=4LA



MODFIED 5/25/2005 2:57:47 PM		Page 4 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03.prj

SIZE	DRAWING NUMBER	Schematic Page 01 of 01	REV
D	0000-ED-173553		

H=8ND; V=4LA

AMP 650473-5
Conn 96pin VME RA PCB Male

P2

Octal Registered Transceiver
U74
SN74LVTH543DW

Octal Buffer/Drivers w/3-State
U62
SN74LVTH541DW

Octal Buffer/Drivers w/3-State
U70
SN74LVTH541DW

Octal Buffer/Drivers w/3-State
U71
SN74LVTH541DW

Octal Buffer/Drivers w/3-State
U72
SN74LVTH541DW

Octal Buffer/Drivers w/3-State
U69
SN74LVTH541DW

Octal Buffer/Drivers w/3-State
U73
SN74LVTH541DW

J74
3m2520-6002UB

J73
3m2520-6002UB

LP3856ES-ADJ
Ultra Low Dropout Regulator
U52

LP3856ES-ADJ
Ultra Low Dropout Regulator
U58

OSC CTS Reeves CB3LV Series
X1
CB3LV-3C-25M0000-T

Hex Inverter Buf/Driv w/O-C Out
U33
SN7406D

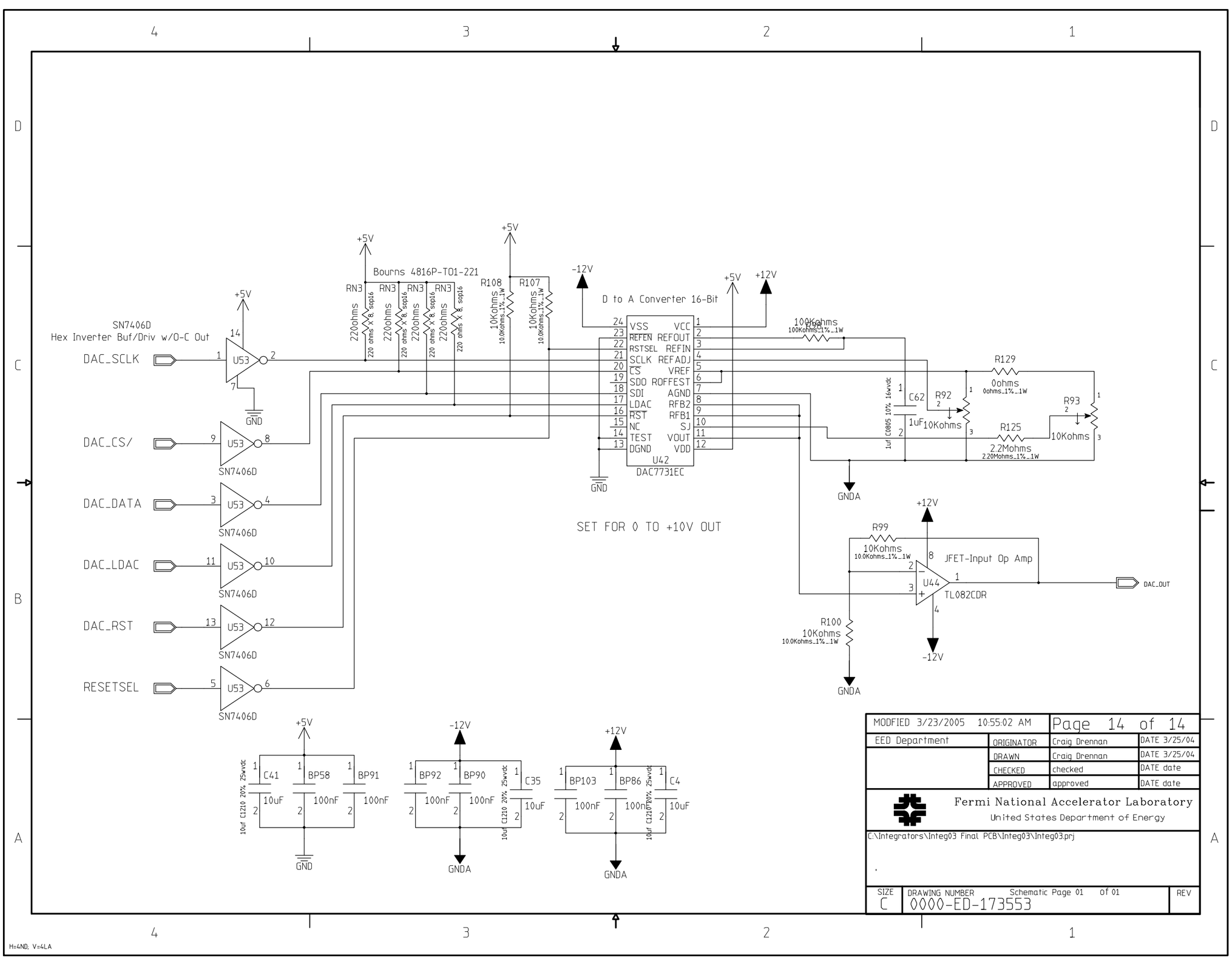
MODIFIED 5/25/2005 2:55:56 PM		Page 3 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03.prj

SIZE	DRAWING NUMBER	REV
D	0000-ED-173553 Schematic Page 01 of 01	

H=8ND; V=4LA



MODFIED 3/23/2005 10:55:02 AM		Page 14 of 14	
EED Department	ORIGINATOR	Craig Drennan	DATE 3/25/04
	DRAWN	Craig Drennan	DATE 3/25/04
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

Fermi National Accelerator Laboratory
United States Department of Energy

C:\Integrators\Integ03 Final PCB\Integ03\Integ03.prj

SIZE	DRAWING NUMBER	REV
C	0000-ED-173553 Schematic Page 01 of 01	

H=4ND, V=4LA