A Working Principle of the DSRD-based Schemes and How this Principle May Be Transformed for the Induction Linac Concept (for SLIM Concept)

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The first part of this note will describe processes of the pulse formation on the resistive impedance and the second part will show the adaptation of a DSRD-based principle for the induction system of the coreless induction linac based on SLIM (Stanford Linear Induction Method) concept [1].

The DSRD-based circuit is based (Fig.1) on two switches. The first switch is ON/OFF switch (Sw). The second one is OFF switch (D1) based on DSRD features. Consequently, there are three time periods. The first period of time is an interval t1 < t < t2, where t1 and t2 are moments when the first switch is turned ON and OFF accordingly. The second time interval is t2 < t < t3, where t3 is a time when DSRD is tuned OFF. The last time period is an interval t3 < t < t4, where tp+t3 = t4 is a pulse duration (i.e. a period of energy delivery on the load).

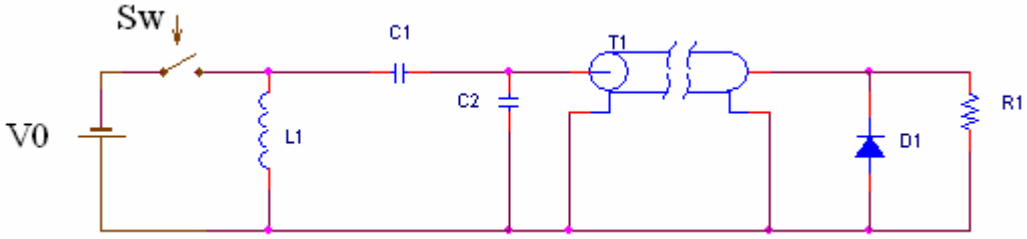


Fig.1 Simple diagram of two stage voltage booster

The energy is accumulated into inductance L1 during the first period of time t1 < t < t2 from a power supply having a voltage V0.

For example, let consider a case when t2-t1=150nsec, L1=40nH, and V0=120V. The trigger pulse length is shown in Fig. 2. The trace shows that the switch is activated at t1=0 and stays ON up to t2=150 nsec. The voltage across inductance L1 and current in the coil L1 vs. time are shown in Fig. 3. and Fig. 4 accordingly. For ideal case, the voltage across inductance has to be a constant vs. time. In our case, there is a small resistive component in the Sw, V0, and L1 loop. That is why there is a voltage drop vs. time that is seen in Fig 2 for t1 <t <t2 interval.

$$i(t) = \frac{1}{L_1} \cdot \int_{t_1}^{t_2} V(t)dt$$

For parameters mentioned above the maximum current is Im~260A for t=t2. There is a small (~11%) leakage current into transmission line. We will not pay attention on this current leakage for this period. If we will not take into account the resistive circuit components than a representation of the equivalent circuit will be as it is shown in Fig 5. The transmission line is shorted by the DSRD diode and the line acts as an inductance L2 for this period of time.

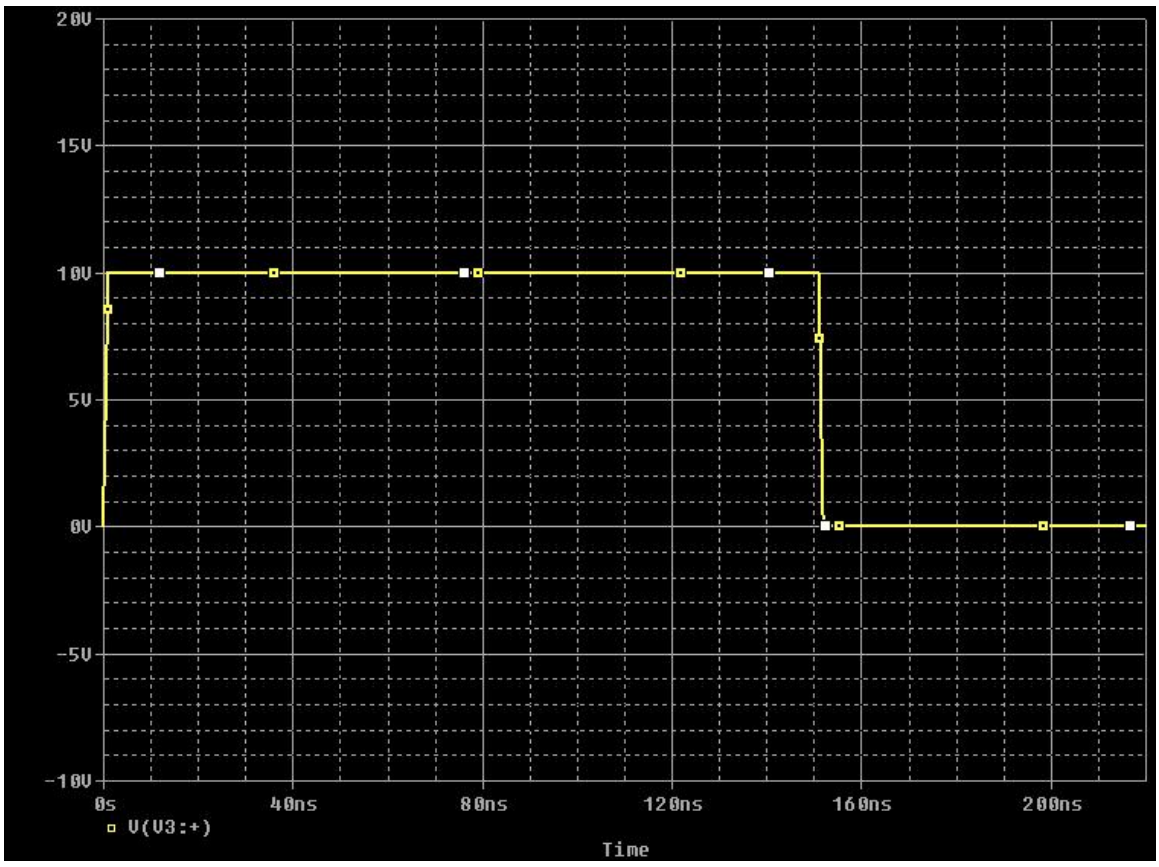


Fig. 2 The trigger width for ON/OFF switch Sw

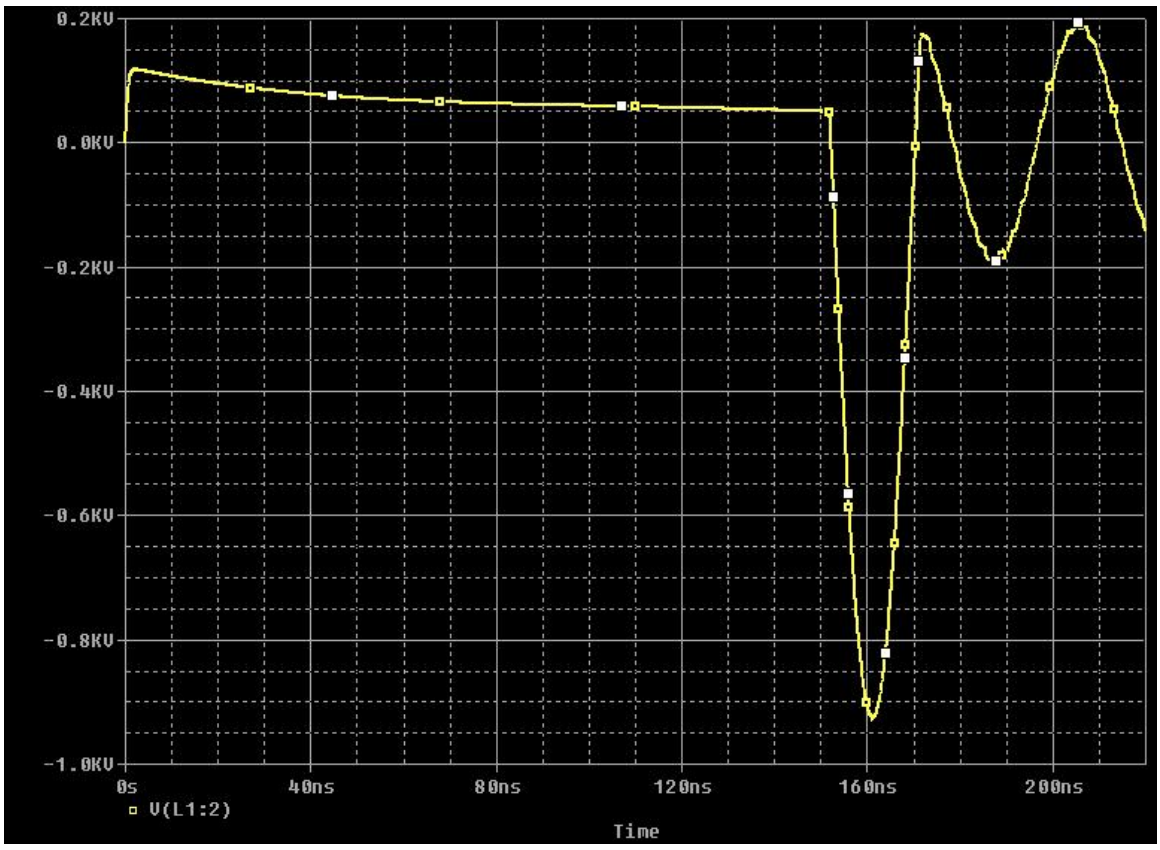


Fig. 3 Voltage across inductor L1 vs. time

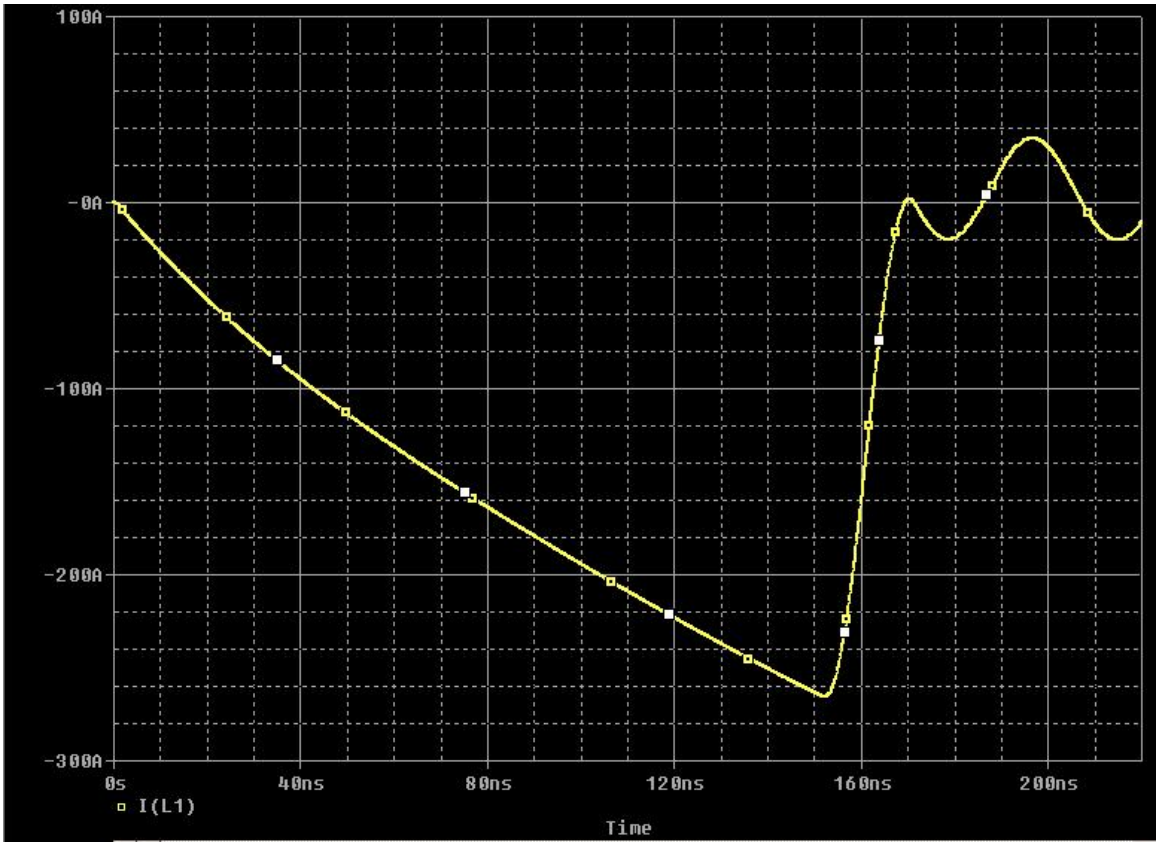


Fig. 4 The current in inductance L1 vs. time

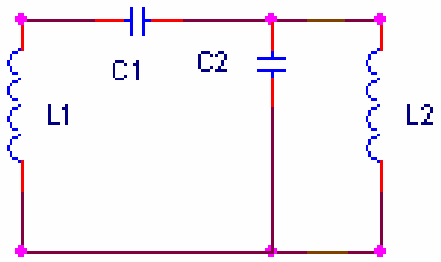


Fig. 5

The period of energy accumulation for the output pulse is finished at t=t2. The amplitude of the current in L1 reaches a maximum.

The switch Sw is turned OFF and the second transient period is started. The current in L1 can not be broken and if the circuit from the left side of L1 (see Fig. 1) is OFF than the L1 current acts on the circuit that is shown on Fig. 5. This LC-circuit has four natural frequencies. One natural frequency is a fast oscillation. The period of fast oscillation is

$$T = 2\pi \cdot \sqrt{\frac{L_1 L_2}{L_1 + L_2} \cdot \frac{C_1 C_2}{C_1 + C_2}}$$

For example, if C1=30nF, C2=1.5nF, and L2=100nH than a half of the oscillating period is 20 nsec. The trace that is shown in Fig. 6, illustrate the transient current in C2 capacitor. The stored in L1 current jumps to C2 capacitor. The amplitude of the L1 current is slightly different due to the leakage current to L2 (i.e. to the transmission line to be exact).

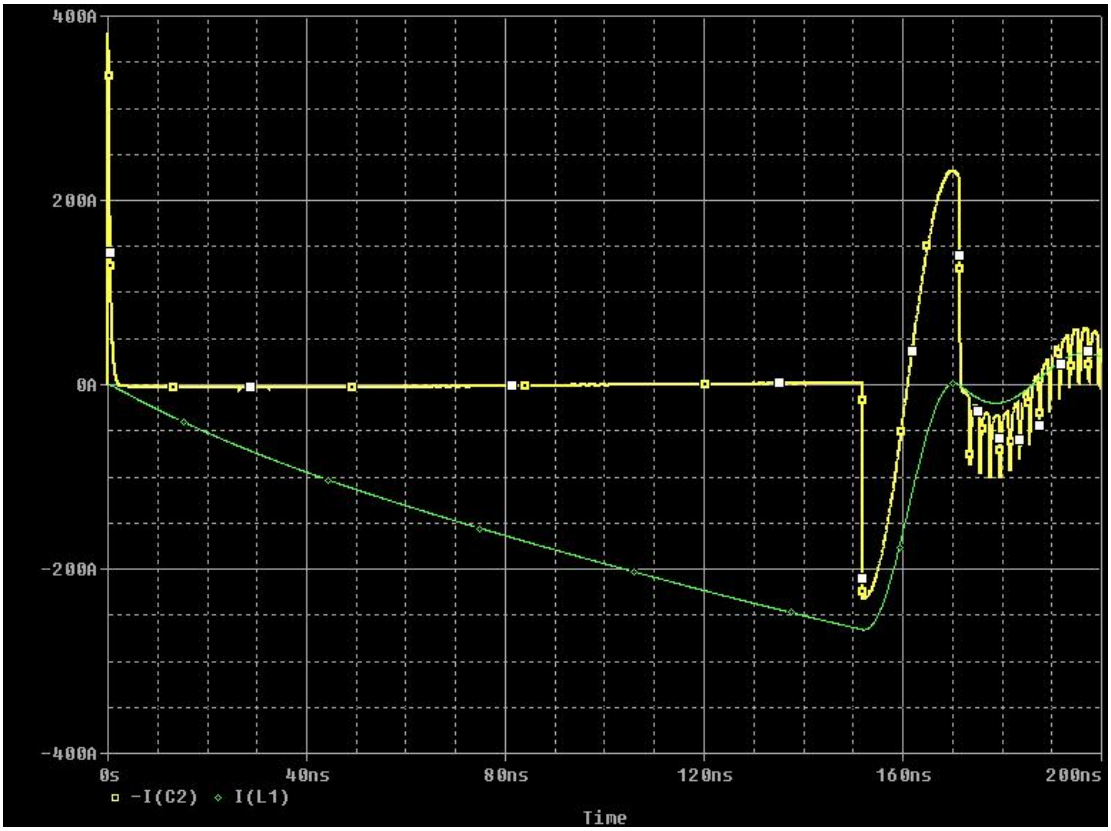


Fig. 6a Trace of C2 (yellow) and L1 (green) currents during the first and second periods

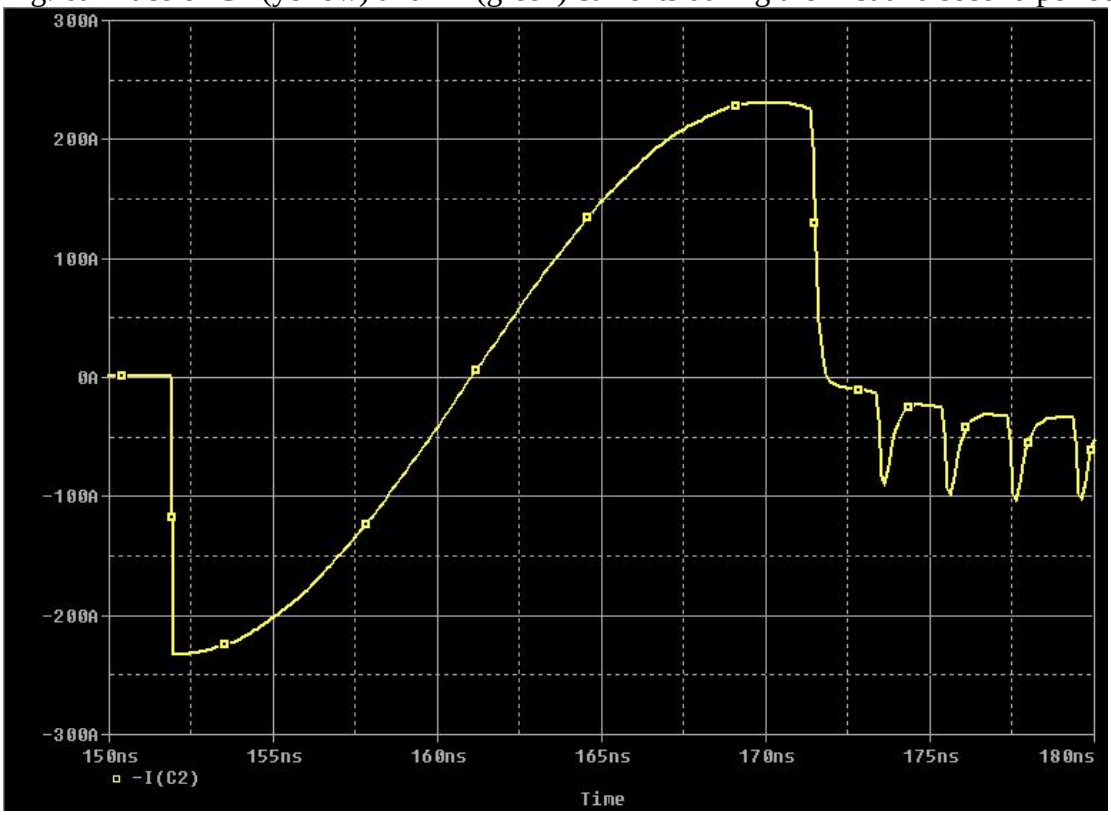


Fig. 6b A shot is the same as in Fig. 6a in more fine horizontal scale This picture shows the transient process of the C2 current. The fist period that is associated with ON/OFF switch work is not shown

The stored energy in L1 will be delivered to C2 capacitor at moment when the C2 current is zero. After that moment the energy will be back to L1 and L2. Due to a fact that the second transient period is much shorter of the first period and the amplitude of the current for the second transient period is practically does not change, the voltage across L1 during second transient period will be much higher than V0. This fact can be seen in Fig. 3. For the circuit parameters mentioned above, the peak voltage at L1 (and at C2) reaches amplitude ~940Vp. The voltage gain is ~7.8. The second transient period will be complete for the moment when the current amplitude in L2 reaches a maximum. The energy will be stored in L2 at this moment. This moment is denoted as t3 moment of time. Up to this moment, the transient processes are relative slow. The fast transient process will be take place during third period (i.e. during $t3 < t < t4$, where $tp+t3 = t4$). Before study of wave processes at this period, we shall look at the current traces in DSRD and on the end of transmission line. These traces are shown for second and third periods in Fig. 7.

Fig. 7 The DSRD current (green) and the transmission line current on its end (yellow) vs. time

As it mentioned above there is a leakage current amplitude at t=150 nsec. During 150nsec<t <170nsec interval both currents are lined up and reaches maximum at t=t3. The energy is stored in inductance of transmission line. At this moment, the injected into DSRD charge in the forward direction will be equal to the pumped in DSRD charge in the reverse direction. The space charge of p-n DSRD junction will be neutralized. The DSRD current is abrupt. The time collapse may be in the subnanosecond range. It depends on a physical feature of DSRD (for example, the doping profile, the carrier concentration, physical size of p-n junction, etc.) in the circuit processes.

The fast collapse in DSRD starts the third period. This period will create the pulse on the resistance load. We will consider the matching impedance case, i.e. the case when the impedance of transmission line is equal to the load resistance. The third period is started at a moment when the DSRD current is abrupt and it is finished when the stored energy in transmission line is delivered to the load. If the electrical length of the transmission line is 1 nsec and its impedance is 50 Ohm, than the detail traces of the currents in DSRD and transmission line is shown in Fig. 8. Here processes in 170nsec<t<175nsec range are shown.

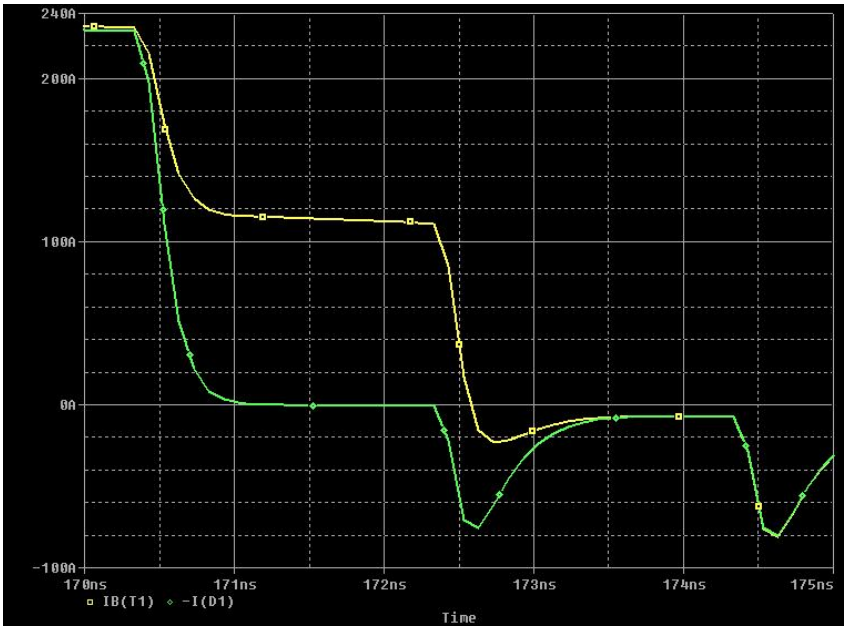


Fig. 8 The DSRD current (green) and the transmission line current on its end (yellow) vs. time for an interval of 170nsec<t<175nsec

Fig. 9 illustrates the load current trace vs. time at 50 Ohm resistance.

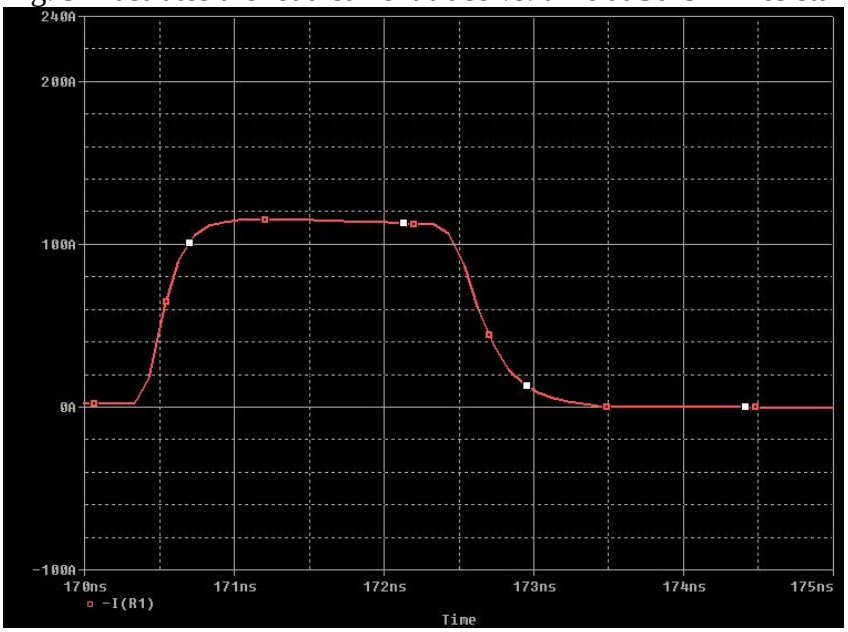


Fig. 9 Output current vs. time for third period

The equivalent circuit setup and wave processes during third interval are shown in Fig. 10. The initial conditions just before the DSRD current break (before t=t3) is as follows. The transmission line TL bears the current I0. The Sw (DSRD in this case) switch is ON. The resistive load is connected in parallel to TL and Sw. There is no current in Rl due to a fact that Sw shunts the TL end. Another end of TL are loaded on C2. The voltage on C2 is zero due to the ON switch state (DSRD shunts C2). The Sw is OFF for t>t3. The current I0 can not stop. It will be split on two equal parts (in the case of matching load). Half of the I0 current will create a wave and propagate through TL. Another half of I0 current will be set on the Rl. The transient process for t3<t<tp is shown in Fig. 10 b) and 10 c). A diagram in Fig. 10 b) shows the part of charge distributed along TL is delivered to the load. However, there is a charge along TL (grey color). The discharge wave moves to the end of TL that is shunted by C2 capacitor. A diagram of Fig. 10 c) illustrate a process when the initial discharge wave has reached C2 and reflected back to the load.

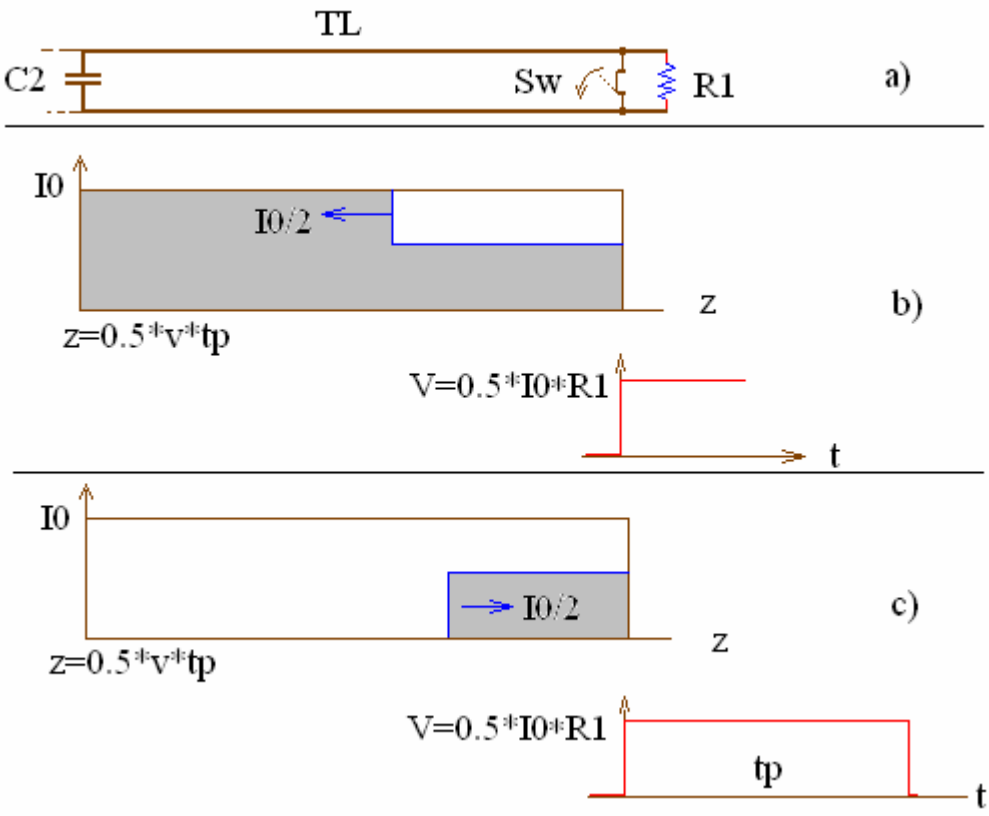


Fig. 10

The C2 capacity is big enough to have a 100% current reflection. When the discharge current wave reaches the load, the stored in TL energy will be delivered on to the load. The third process is completed. For the circuit parameters that is mentioned above, the voltage on the 50Ohm load (for the discussed above example) will be ~5.75 kV. The pulse width is 2 nsec. The total voltage gain is ~48.

There are several schemes that have been used for the rectangular pulse generation. In most common cases, the combination of transmission line with a turn ON switch is used. The energy is stored in the electrostatic manner. During a storage time, the normal switch state is OFF. The switch and transmission line are stressed to hold off the voltage during

a whole charging period. Three basic circuits are typically employed for the square-pulse generation with turn ON switch. They are Line-type scheme, Blumlinein scheme, and Zarem-Marshall-Hauser scheme. Ideal discharging circuits for these three schemes are shown in Fig. 11 a), b), and c) accordingly.

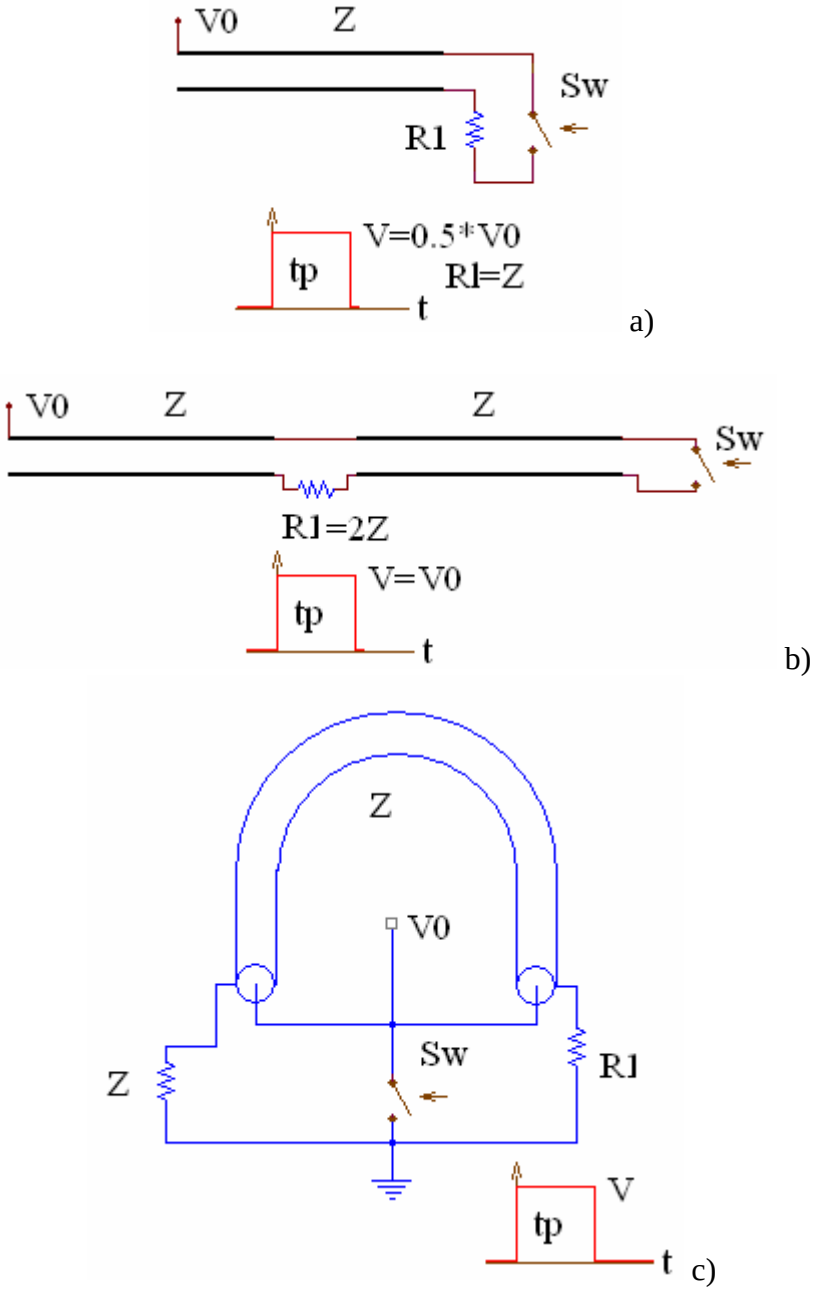
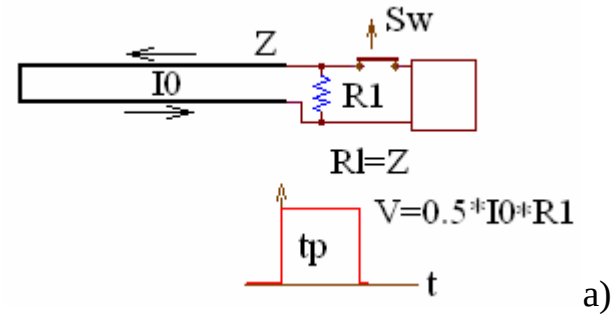


Fig. 11 Simple diagrams of the discharging circuits for a square pulse formation on resistive load

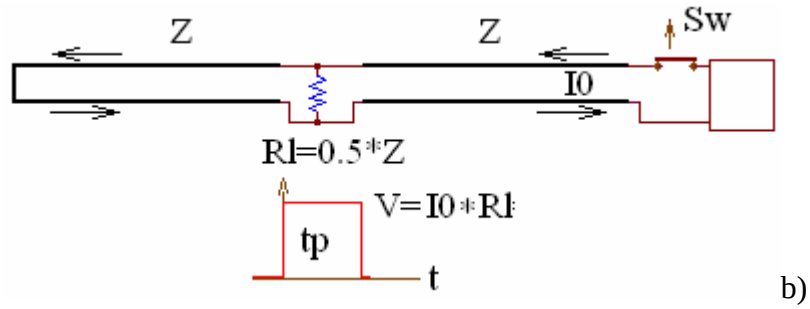
A discharging circuit for line-type scheme generates a pulse width tp on the load Rl with an amplitude V that is half of charging voltage of transmission line Z. A discharge circuit for Blumlein scheme (with dual transmission lines) creates a pulse tp, the amplitude of that is equal the charging voltage V=V0. However, the load impedance must be twice higher of the impedance of used transmission lines. The current through the switch is twice higher in compare with line-type scheme (if the rest parameters are the same). Both circuits generate a rectangular output pulse on the matching load with no after pulses. The

third circuit creates a square-pulse on the mismatching load Rl with no after pulse. The output amplitude depends on the ratio between transmission line (Z) and load (Rl) impedances.

The discharge circuits shown in Fig. 11 a) and b) may be easily transformed for the case in which the turn OFF switch is used. The normal switch state is ON. The switch will stay ON for a magnetic energy storage period. The switch will be OFF only for short period of square-pulse generation. Transmission line and switch will be electrically stressed only for this short period. A circuit diagram for Line-type and Blumlein schemes based on OFF switch is shown in Fig.12 a) and b) accordingly.



a)



b)

Fig. 12 Simple diagrams of the circuits based on OFF switch for a square-pulse generation on resistive load

The load Rl will be shorted for a period of ON time. When the switch is OFF, the transient process is began. During transient process, a rectangular pulse is created if the matching conditions are satisfied. An amplitude of the output pulse will correspond shown in Fig.12 equations. The load in these circuits is connected in parallel with transmission line. The load of the discharging circuits (Fig. 11) is connected in series with transmission line. As a result, to satisfy the Blumlein condition for a circuit based on the OFF switch, the load impedance must be twice lower than transmission one. It is easy to show that the reflection on the load connection for both circuits shown in Fig. 11 b) and Fig. 12 b) will equal 0.5. A modification of the line-type circuit with OFF switch was used in scheme shown in Fig. 10 a).

A method of the pulse generation based on the OFF switch technique may easily be transformed for the induction system of a coreless induction linac. For example, a possible simplified cross section of an inductor is shown in Fig. 13. This drawing is based on the transformation of Fig. 1 circuit into inductor. The transmission line (TL) and DSRD are part of induction system. One end of TL is shorted by capacitors C. Components of current source 3 are not shown. It is assumed, that a central electrode of TL is excited by the current the trace of which is shown in Fig. 13. There are two cavities

1 and 2. The cavity 1 is shorted on the inner radius. The cavity 2 is loaded by DSRD on outer radius. There is a cavity 2 gap near axial axis z. The gap is used for a beam acceleration. It is necessary to introduce the blocking capacitor Cb into inductor. This capacitor will avoid the DSRD shunt by shorted cavity 1 end during initial processes, i.e. during a storage energy in TL to be exact. It was shown in the first part that a high voltage pulse is generated across DSRD. The power of this pulse will be split on two parts. One part will propagate in cavity 1 and another will go in cavity 1.

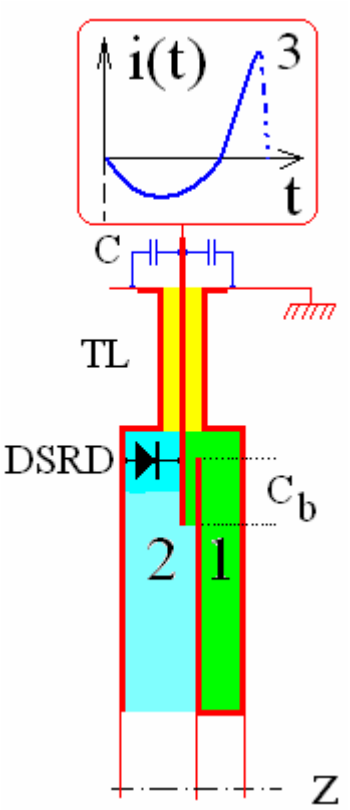


Fig. 13 A possible inductor diagram for coreless induction linac

A capacity of Cb is small enough to decouple cavity 1 without a significant power loss during storage energy in TL. The cavity 2 will transmit the power in accelerating gap. The power in cavity 2 will act on the acceleration field after moment when the wave reaches a short end, reflected back to cavity 2, and launch on accelerating gap. A power in the cavity is much smaller in compare with the power of cavity 2. The cavity with short end is necessary for a stack side by side of inductors along z axis.

Let us evaluate the inductor parameters to accelerate 690A beam with a 2 nsec pulse width. As it is seen in Fig. 9, a 2 nsec, 115 A pulse on 50 Ohm load is generated by a shown in Fig. 1 circuit. If distribute in azimuthal direction (around z axis) six transmission lines with its DSRD, the effective load impedance on the accelerating gap will be approximately 8 Ohm. Six individual cells will work on one inductor. A value of Cb capacitor may be Cb=100pF per each cell. In this case, a peak voltage across Cb is less than 1.5 kV. An accelerating voltage on the gap (red) and a voltage across Cb (yellov) is shown in Fig. 14 for a period 150 nsec<t< 175 nsec. The radial length of TL is 20 cm, if the dielectric constant of TL media is 2.25. A length of DSRD assembly with 6 kV voltage hold off may be 3-5 mm. The radial length of cavity 1 and 2 may be a short enough to transmit power to the accelerating gap.

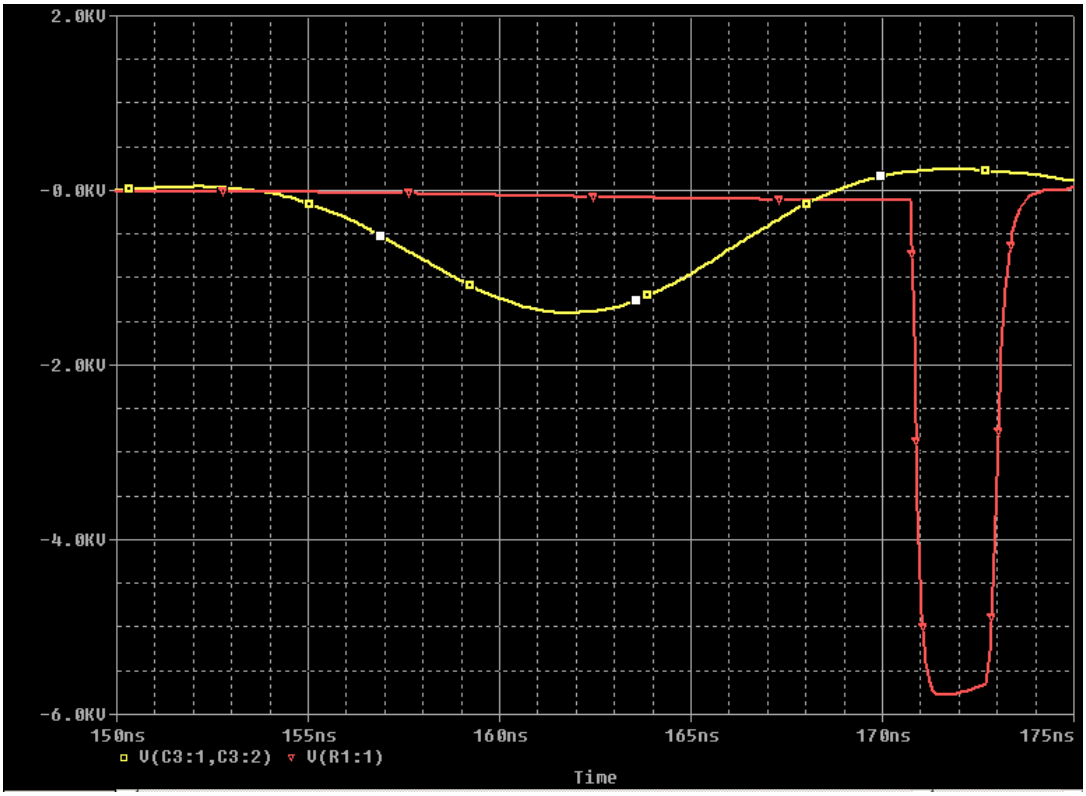


Fig. 14 Accelerating voltage (red) and voltage across blocking inductor capacitor (yellow) vs. time

A cross section of the inductor shown in Fig. 13 may be simplified if a circuit diagram shown in Fig. 12 a) is exploits for the inductor design. For example, the accelerating voltage for shown in Fig. 15 a) inductor on resistive load R_{load} is realized for the input current that is displayed in Fig. 15 b).

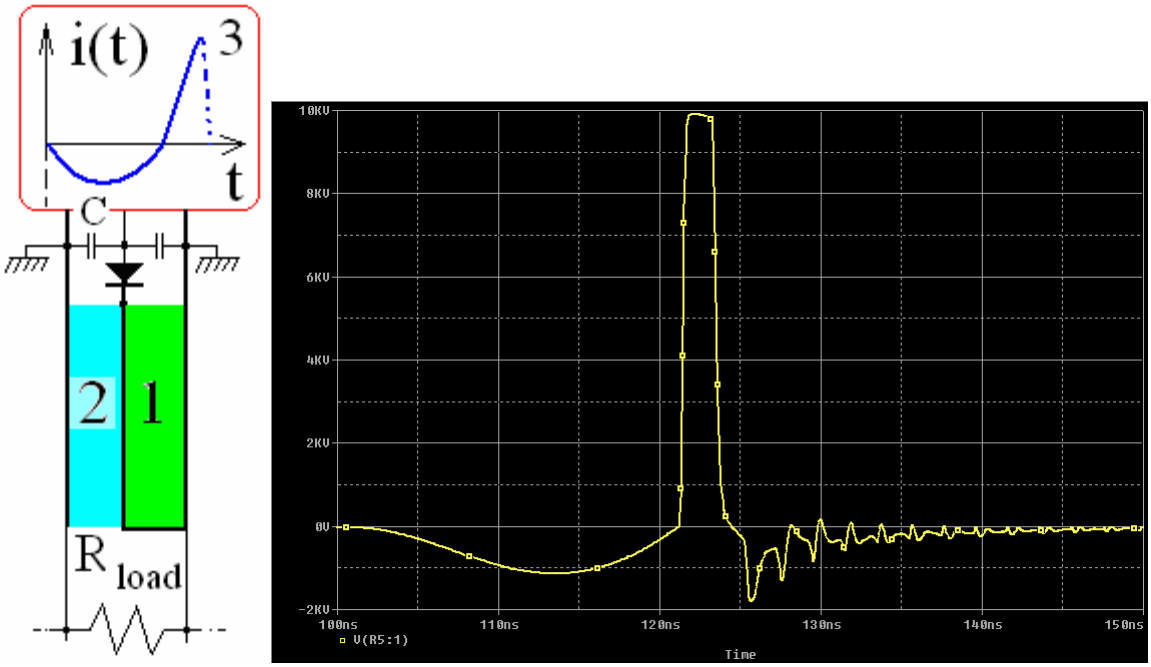


Fig. 15 a) Coreless inductor with the DSRD stack and b) beam loaded accelerating voltage

A simulation of the inductor model was performed for the case of 2 nsec pulse width and 200 A load current. The inductor input (yellow) and output (red) currents are shown in Fig. 16.

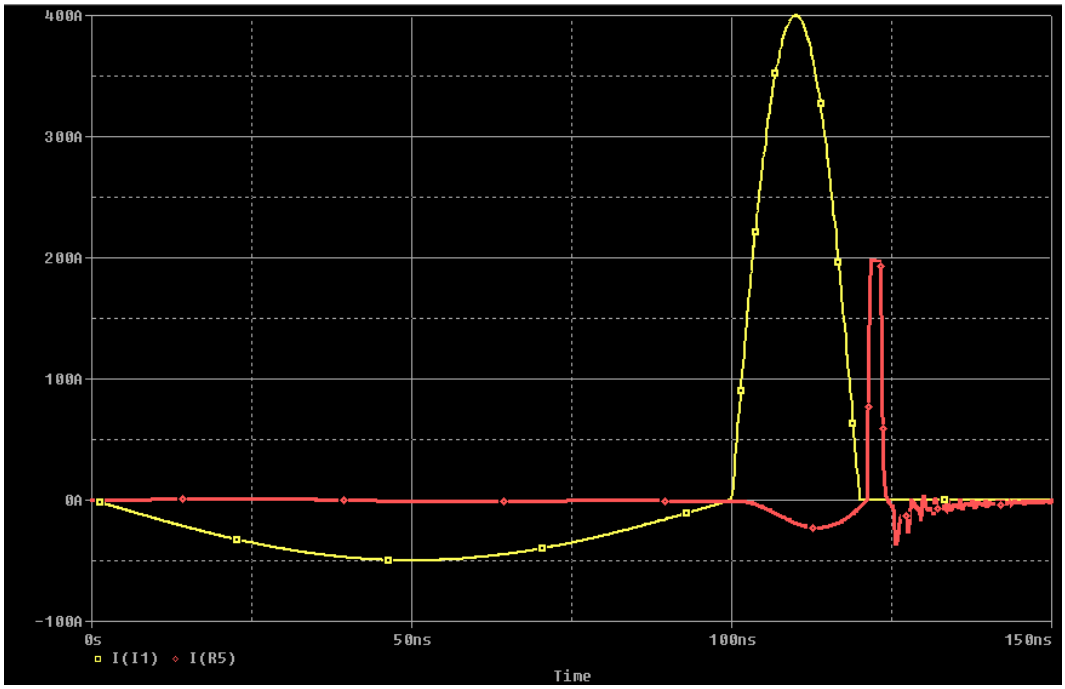
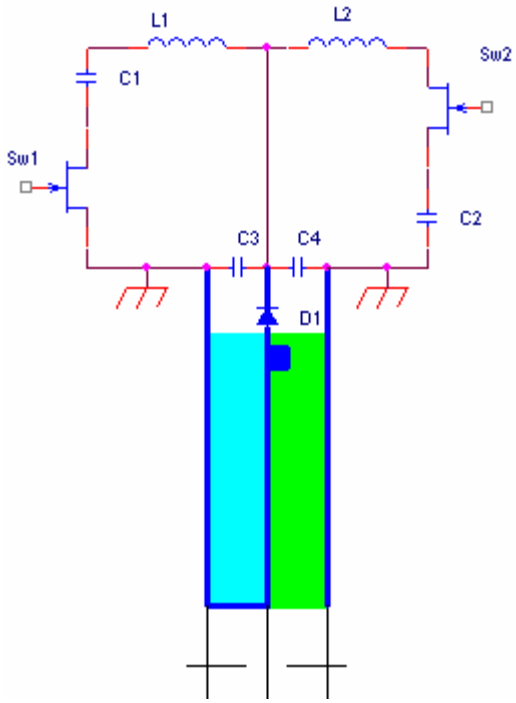


Fig. 16 Input and output current vs. time

The amplitude of DSRD current in forward direction is 50A for 100 nsec of a half of oscillating period. This period is five time less for the reverse DSRD current. Amplitude of the reverse current is 400A.

Two individual LC contours with two in two switches may be employed to create the needed input current. The simplified circuit diagram for this case is shown in Fig. 17.



Capacitors C1 and C2 are charged from power supply. The Sw1 switch is closed and a cycle of pumping DSRD diode D1 is started. Circuit parameters C1, L1, and an inductance of inductor are a key parameter for the transient process in forward DSRD direction. Sw2 is closed at the moment when the forward current is zero (a half period of oscillatory process in the first L1C1 loop). The discharge current in L2C2 loop goes in the reverse DSRD direction. Impedance of second L2C2 contour is less in compare to L1C1. The current amplitude in L2C2 circuit is higher than L1C1 one. The input current diagram vs. time looks like a yellow trace shown in Fig. 16.

Fig. 17 Simplified circuit diagram for coreless induction cell based on DSRD feature

A disadvantage of shown in Fig. 17 circuit is a necessity to employ of two independent trigger channels for Sw1 and Sw2. The second disadvantage of the Fig. 17 diagram is the following fact. The discharge current through Sw2 is high and discharge period is short. The Sw2 switch works hard. As a role, more current through Sw2 will be related longer period for the reverse current process. Sometime it is difficult to realize the necessary condition for L2C2 circuit and Sw2 switch. These disadvantages may overcome by the introducing of the saturating core L2 that plays a role of a magnetic switch. The simplified circuit diagram for this case is shown in Fig. 18.

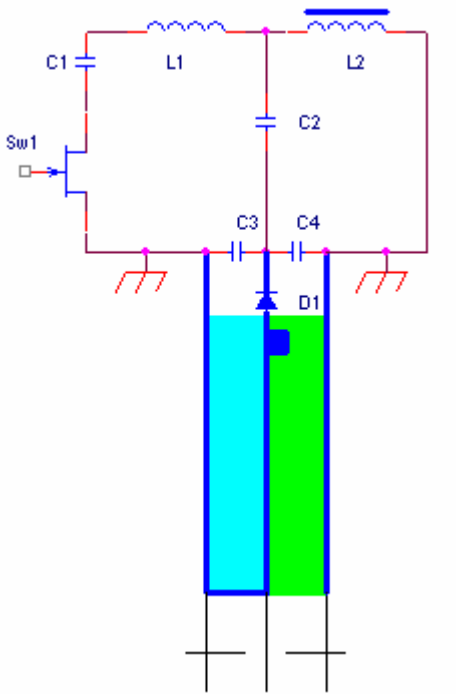


Fig. 18 Simplified circuit diagram for the exciting of inductor with DSRD-based switch. A saturating core is used in the booster system

The magnetic core parameters are chosen in such a way that the core is saturated at a moment when the delivery energy from C1 to C2 (through L1, inductor, and DSRD) is complete. After core saturation, C2 capacitor is quickly discharged through DSRD in the reverse direction.

The transformation of shown in Fig 12 b) circuit in induction system is also feasible. The induction system would be interesting for a multi beam mode. The beam bore circle radius in this case is equal to the length of shorted part of Blumlein line. The detail study of this concept is a subject of another note.

Conclusion

Detail descriptions of working principle of DSRD-based circuits are discussed. The feasible transformation of these circuits to the induction cell is shown. This technical note concerns to earlier discussion of proposed SLIM concept in the frame of the muon progam in FNAL. The high gradient coreless induction system may be interesting and for other applications such as fusion, free electron lasers, etc.

Caviar of the proposed SLIM concept is a solid state OFF switch in induction cell. The natural switch state is ON. Only short (several nanoseconds) interval the switch is OFF. At that time, the delivery of energy to the beam takes place. The energy in the induction system initially is storied in the magnetic field when the switch is ON. Such concept promises to get the high gradient in induction cells.

Reference

[1] A. Krasnykh, Coreless Concept for High Gradient Induction Linac, SLAC-WP-078