Characterization of the Fast Phase Detector in the Booster Low Level RF System

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I. Introduction

The Fast Phase Detector measures the phase difference between a beam current monitor signal and a VCO signal reference for the RF cavities. The phase signal out of the phase detector is used as feedback in a phase locked loop with the VCO. For reasons we will not go into here, a 40 ns to 100 ns portion of the beam is notched out or removed from each booster batch. It is desired to hold the phase signal out of the phase detector fixed during the interval in which the phase signal would show a response the presence of the notch.

Though the current Fast Phase Detector performs sufficiently well, the circuit is more than fifteen years old and most of the essential components are currently unavailable. Therefore it is being proposed that a new Fast Phase detector be designed using available components and incorporating the needed fast sample and hold function.

Since the current Fast Phase Detector is part of a tuned control loop essential to the operation of the Booster, we must characterize it in order to specify the next version. The new phase detector will need to match the current one in regard to scaling, dynamic response, and input bandwidth and dynamic range.

This note documents the results of the characterization tests performed on the current Fast Phase Detector as well as the results of these tests performed on a preliminary prototype of a circuit that could replace the current one.

II. Description of the Current Fast Phase Detector

C. Kerns designed the current Fast Phase Detector in 1987 (DWG# 0331.00-ED-180843). The schematic in Figure II.1 shows high speed comparators on each input to detect the zero crossings of each signal followed an ECL XOR logic gate. The diode bridge following the XOR gate acts to switch current into or out of the integrating amplifier in proportion to the phase difference between inputs A In and B In.

The –10 V to +10 V output represents a phase difference between A In and B In of 0 to 180 degrees. The phase in Degrees is computed from the Phase Out in Volts, according to

$$Phase(\text{deg}) = PhaseOut(Volts) * (-180/20) + 90$$

The current Fast Phase Detector does incorporate sample and hold circuitry intended for use when measuring the phase with a partial turn of beam in the Booster. However, this portion of the circuit has not been used for many years. This sample and hold introduces switching charge errors that are significant in the current Booster Low Level RF control and needs to be improved.

III. Specification for the Operation of the Fast Phase Detector.

The existing Fast Phase Detector works within the specifications given below. A new Fast Phase Detector would need to meet these specifications as well.

1. Input signal frequencies are from 37 MHz to 53 MHz.
2. Input signal strength of the detected beam signal ranges from 30 mV to 300 mV RMS (+2.5 dBm to –17 dBm for a 50 input).
3. Bandwidth (-3dB) of the detected phase is approximately 1 MHz.
4. Output signal is +/- 10 V, with the phase relationship $Phase(\text{deg}) = PhaseOut(Volts) * (-180/20) + 90$.
5. Detected phase accuracy within +/- 0.5 degrees between 60 to 120 degrees and within +/- 1 degree between 30 to 150 degrees.

The next Fast Phase Detector is expected to implement the sample and hold function using A/D to D/A digitization techniques. Hence additional specifications include

6. A/D and D/A output signals should be good to 12 bits.
7. Signal propagation from input to output should be kept below 100 ns and preferably less than 30 ns.
8. The sample and hold function should be able to hold the output for 0 to 300 ns with minimal transient disturbance of the output signal when switching (less than 5.0 mV peak).
9. Three or Four buffered copies of the of the analog phase voltage derived before digitization should be made available as well as four copies of the phase voltage after the sample and hold.

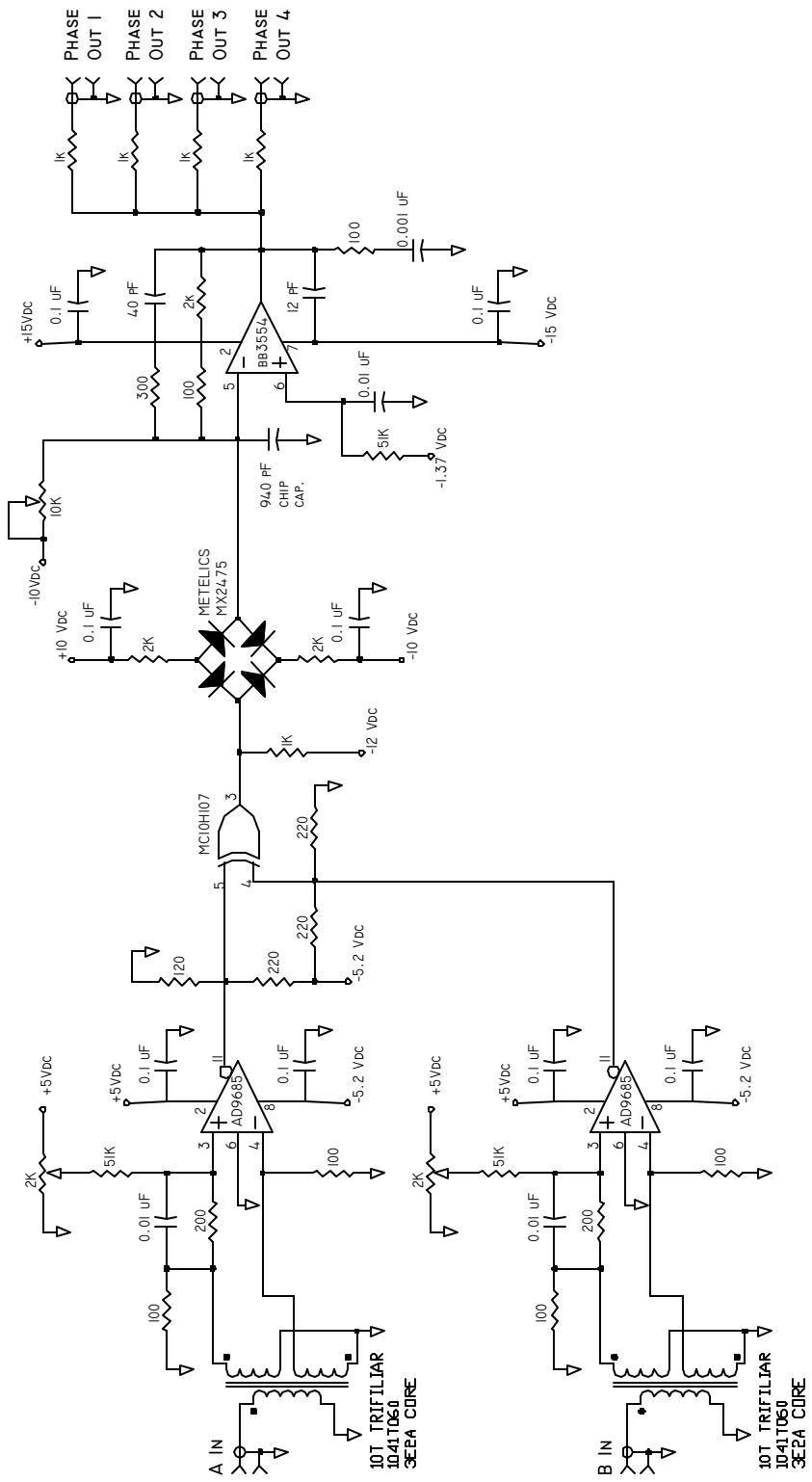

Figure II.1 Schematic of the current Fast Phase Detector, Kerns 1987.

IV. Test Performed on the Fast Phase Detectors.

A number of tests were performed on the current version of the Fast Phase Detector as well as the prototype of its proposed replacement. The following sections describe the tests and present the results.

IV.1 Test 1: The Beat Frequency Test of the Phase Modulation Bandwidth

Two signal generators are used to provide Input A and Input B of the Phase Detector with signals with an offset in frequencies. Since we expect to express the phase difference between two signals of the same frequency we consider the following.

$$Input\ A = Cos(2pF_1t)$$
$$Input\ B = Cos(2pF_2t) = Cos\left(2pF_1t + 2p\,(F_2 - F_1)t\right)$$
$$OR$$
$$Input\ B = Cos\left(2pF_1t + f(t)\right),\quad where\quad f(t) = 2p\,(F_2 - F_1)t$$

It is plain that the phase between these two inputs is a ramping type function with a slope equal to $2p\,(F_2 - F_1)$ Radians / Second. The phase detectors are design to have an output voltage according to

$$PhaseOut(Volts) = \frac{\left|Phase(Deg)\right| - 90(Deg)}{\left(-180(Deg)/\,20(Volts)\right)}$$

Hence the output of the Phase Detector is a periodic triangle-wave with a period

$$\mathrm{T} = 1 \Big/ (F_2 - F_1)$$

A scope picture of the Phase Detector output is shown in Figure IV.1.1. The equipment setup for Test 1 is illustrated in Figure IV.1.2. Test 1 measures the output amplitude of the triangle-wave for fundamental input frequencies of {30 MHz, 36 MHz, 42 MHz, 48 MHz, 54 MHz}with frequency offset in Input B in several steps between 10 KHz and 2 MHz for each fundamental frequency.

The results for the Kerns Phase Detector are shown in Figure IV.1.3, and those for the proposed replacement in Figure IV.1.4.

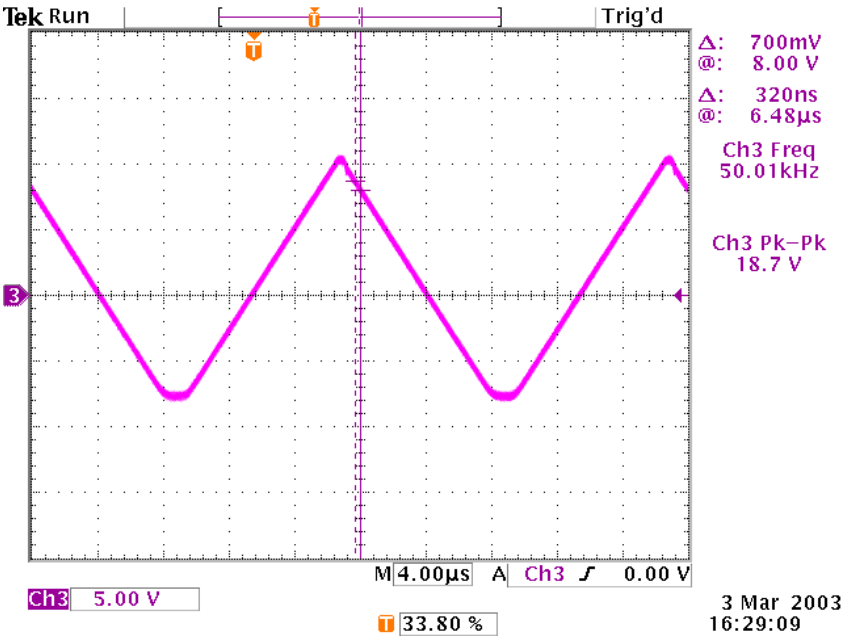

Figure IV.1.1 Example of the Phase Detector outputs seen in Test 1.

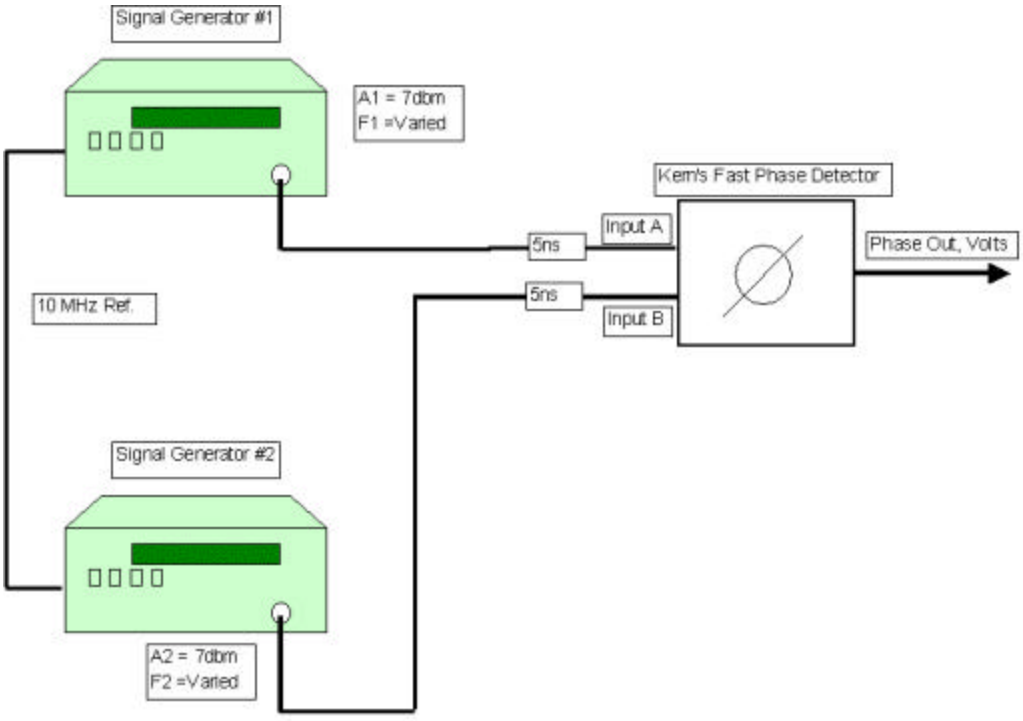

Figure IV.1.2 Setup for Test 1: Beat Frequency Test of Phase Modulation Bandwidth.

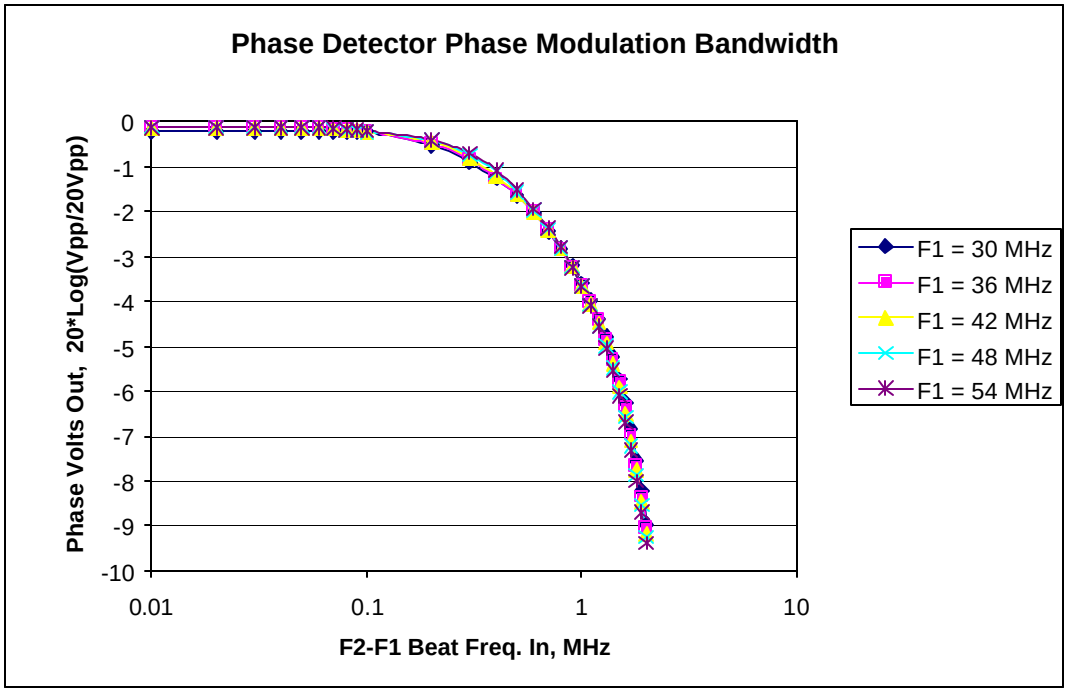

Figure IV.1.3 Results of Test 1 on the Kerns Phase Detector

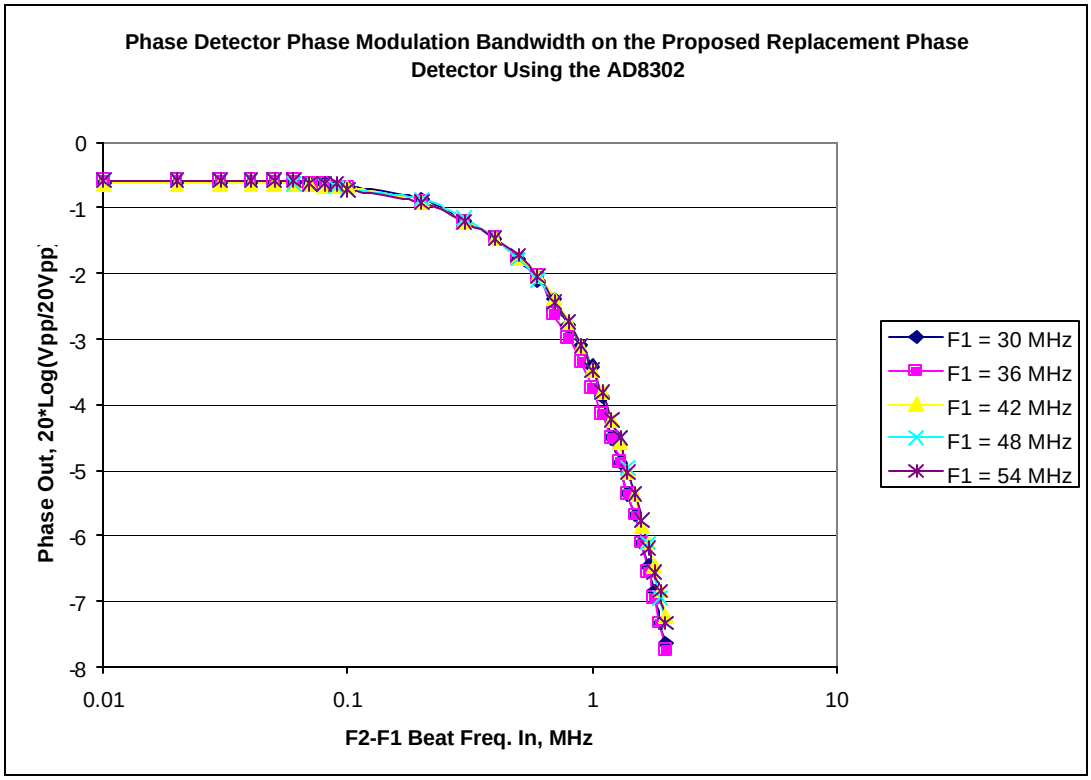

Figure IV.1.4 Results of Test 1 on the AD8302 Phase Detector.

IV.2 Test 2: The Input Amplitude Dynamic Range.

Test 2 provides a measure of the input signal amplitudes for which the phase detectors will give an accurate response. The setup for Test 2 is illustrated in Figure IV.2.1. Here the phase relationship between Input A and Input B is fixed for a given frequency according to the difference in length between the cables connecting the signal splitter outputs to the phase detector inputs. The amplitude of both signals are varied using the amplitude adjustment of the signal generator.

The results for the Kerns Phase Detector are shown in Figure IV.2.2, and those for the proposed replacement in Figure IV.2.3.

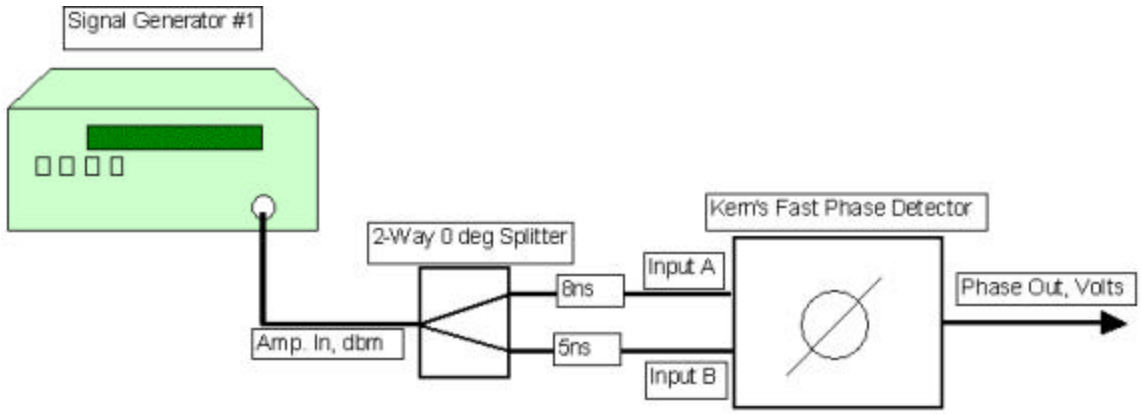

Figure IV.2.1 Setup for Test 2: Input Amplitude Dynamic Range.

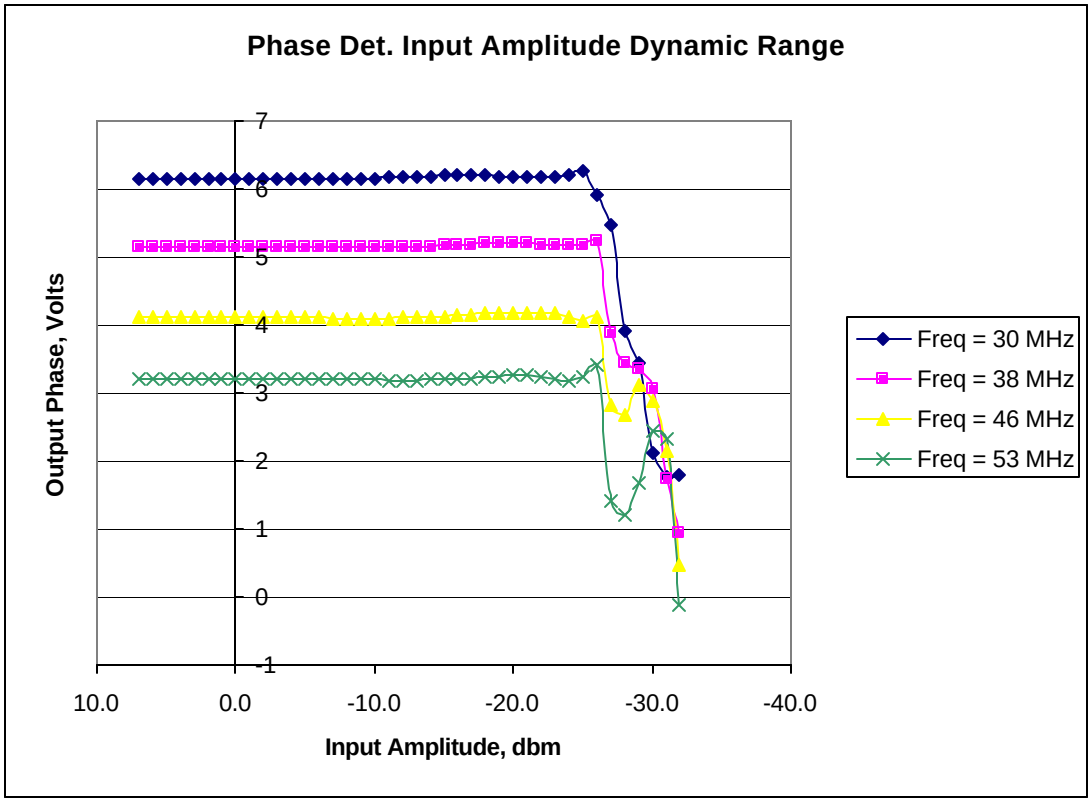

Figure IV.2.2 Results of Test 2 on the Kerns Phase Detector.

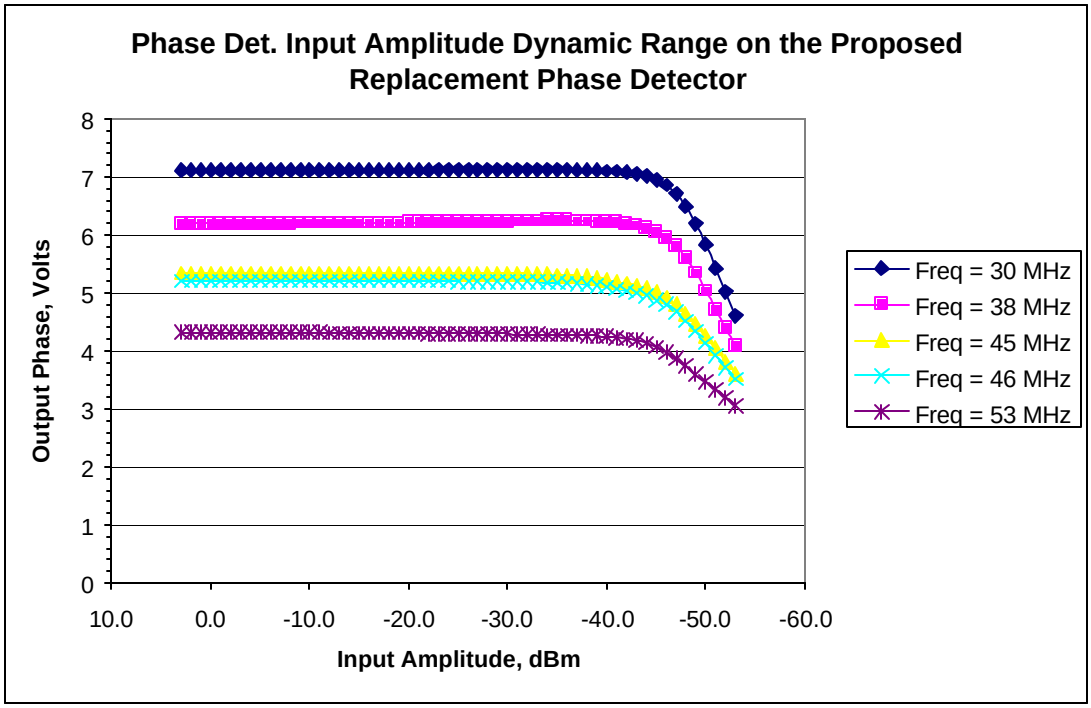

Figure IV.2.3 Results of Test 2 on the AD8302 Phase Detector.

IV.3 Test 3: The Beam Input Amplitude Dynamic Range.

In Test 2 both the beam pickup signal and the VCO frequency reference signal were attenuated. In Test 3 only the beam pickup signal is attenuated. This is more like the situation we are concerned with in the LLRF system since the VCO reference signal is set to always be the same amplitude. Figure IV.3.1 illustrates the setup for Test 3. Three BNC attenuators connected in series are chosen for each of the desired attenuation values used in the test. The nominal value of the attenuation is used, however the particular phase through each attenuator used in the test was measured using a network analyzer and then used to correct the value of phase in degrees measured. This had only a small effect on the final results.

The results for the Kerns Phase Detector are shown in Figure IV.3.2, and those for the proposed replacement in Figure IV.3.3.

Figure IV.3.4 and Figure IV.3.5 chart the output deviations of the phase output signals from nominal output at the largest signal input amplitude, -3 dBm, as the beam signal input amplitude is decreased

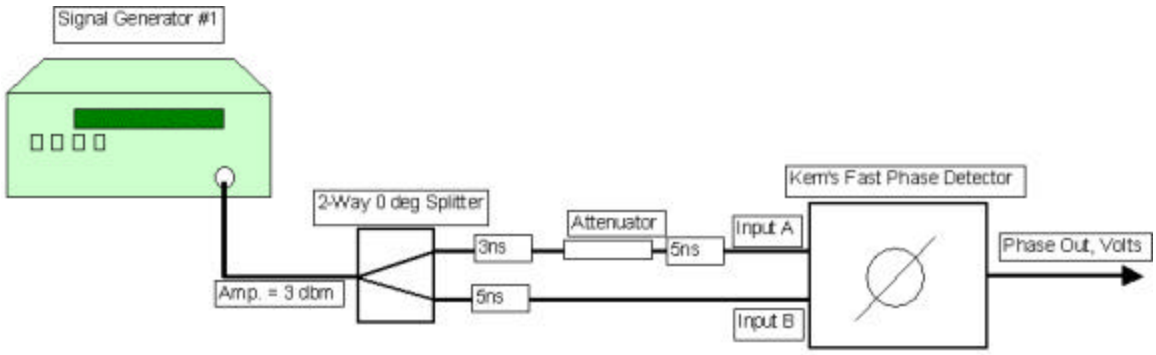

Figure IV.3.1 Setup for Test 4: Beam Signal Input Amplitude Dynamic Range.

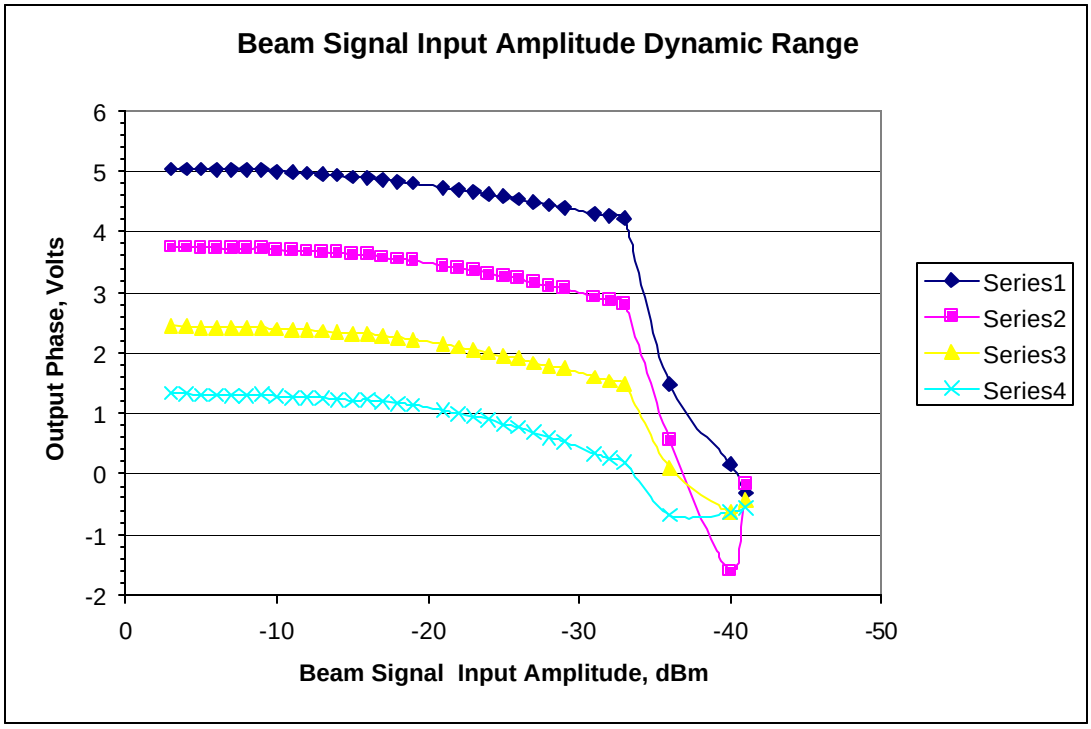

Figure IV.3.2 Results of Test 3 on the Kerns Phase Detector.

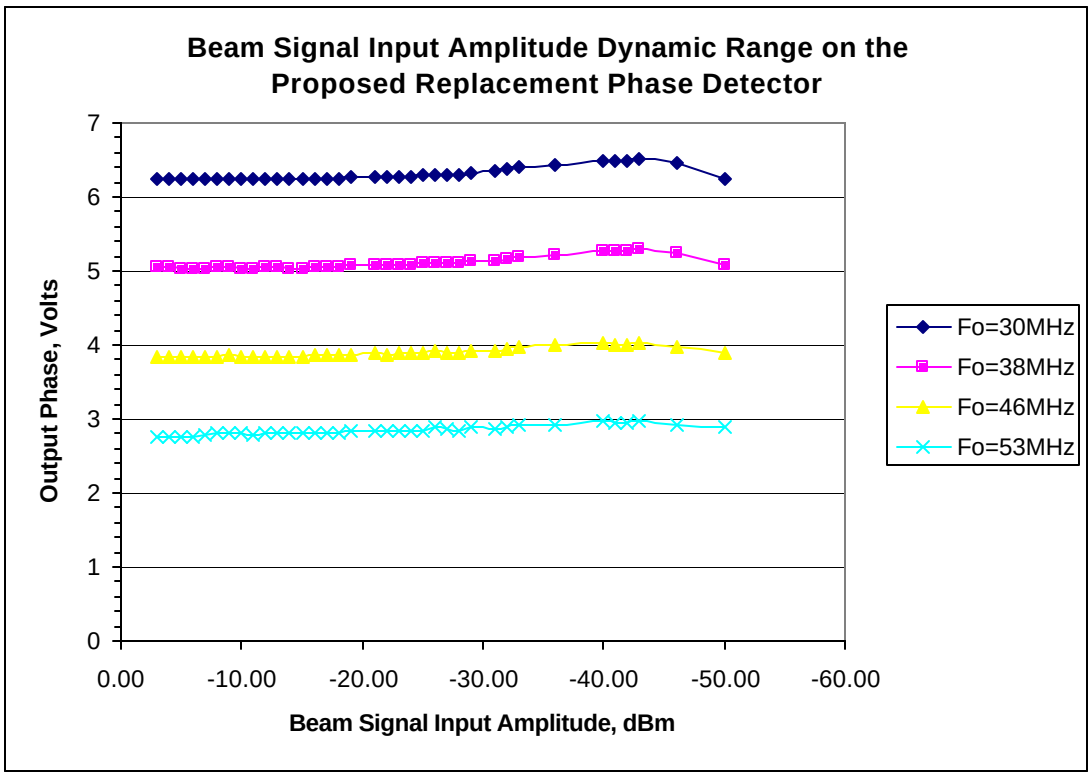

Figure IV.3.3 Results of Test 3 on the AD8302 Phase Detector.

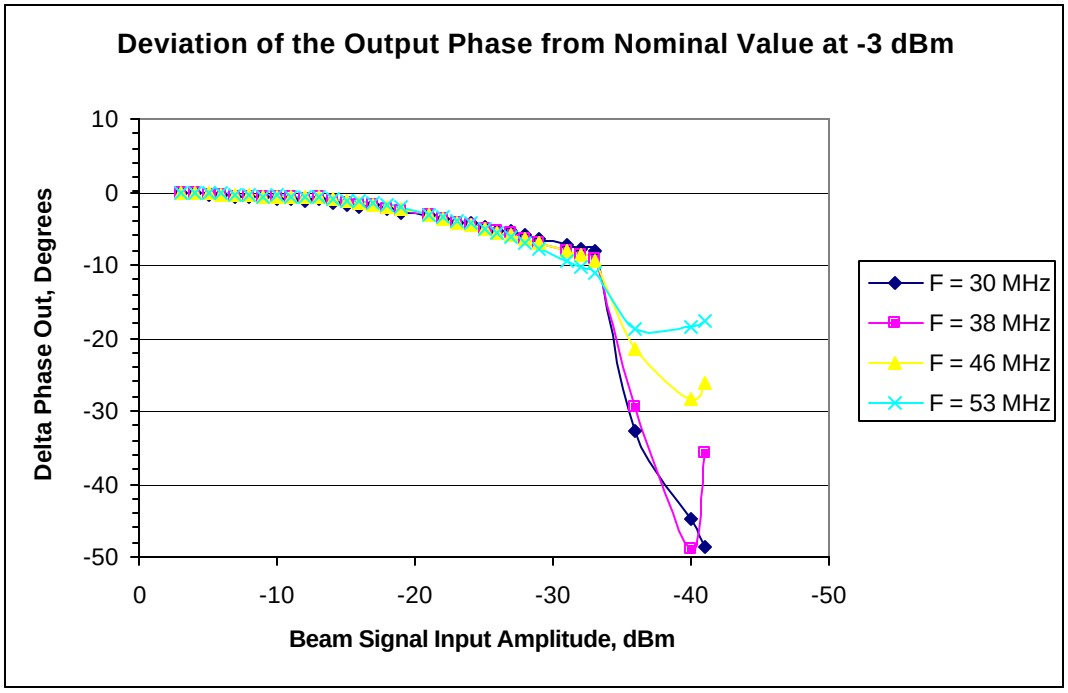

Figure IV.3.4 Phase detector output deviations from nominal, in Degrees (Kerns).

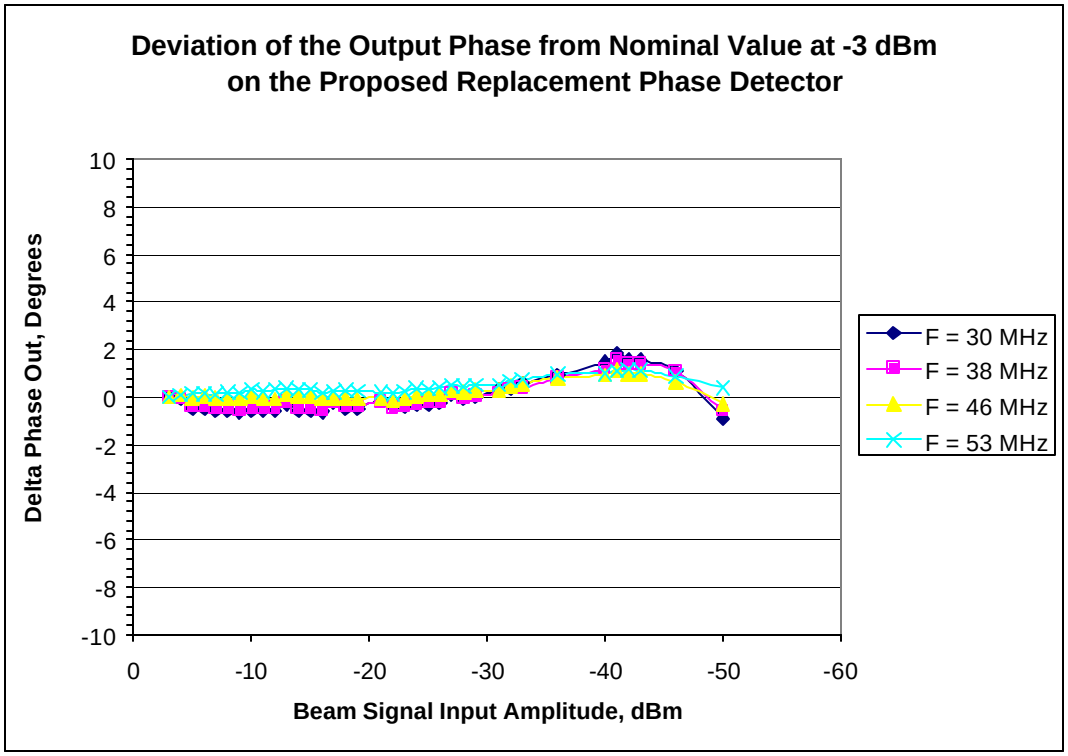

Figure IV.3.5 Phase detector output deviations from nominal, in Degrees (AD8302).

IV.4 Test 4: The Response Linearity.

In Test 4 the rising slope of the phase detectors triangle-wave output is recorded using the oscilloscope. The data is transferred to Excel using a floppy disk. A linear regression is performed on the data for phase outputs between 30 Degrees and 150 Degrees. The residuals from this straight line fit provide the indication of the linearity of the phase detectors response.

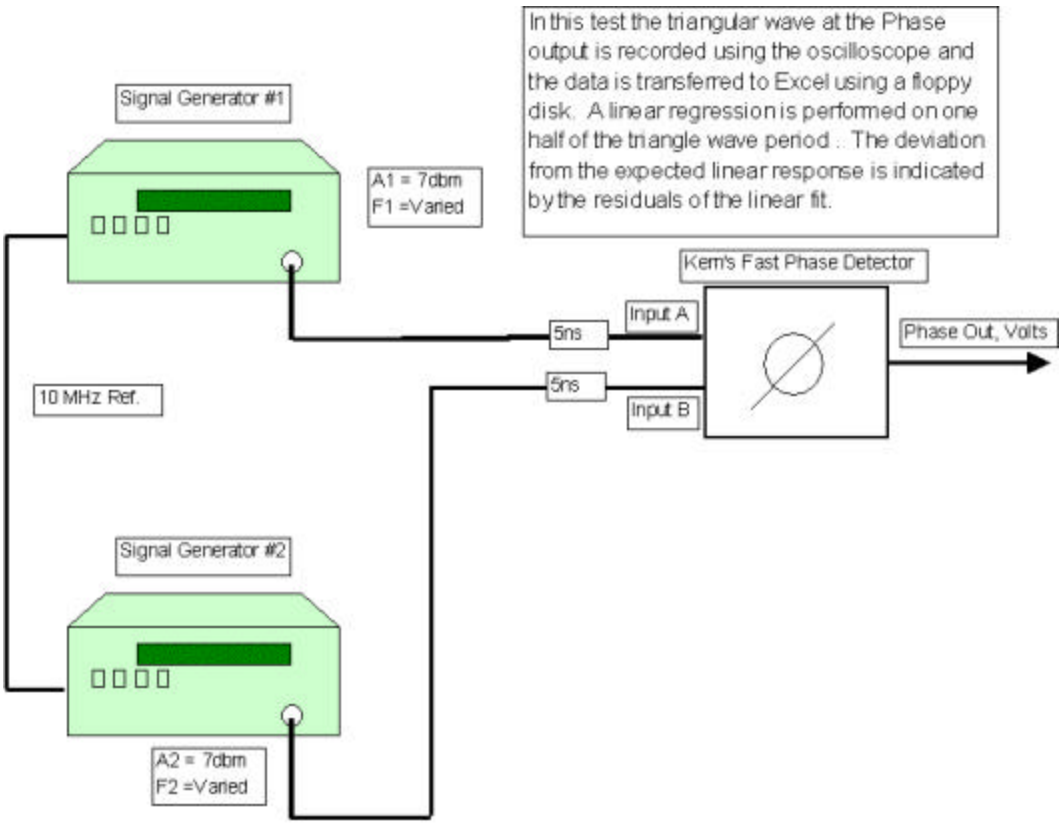

Figure IV.4.1 Setup for Test 4: Output Linearity.

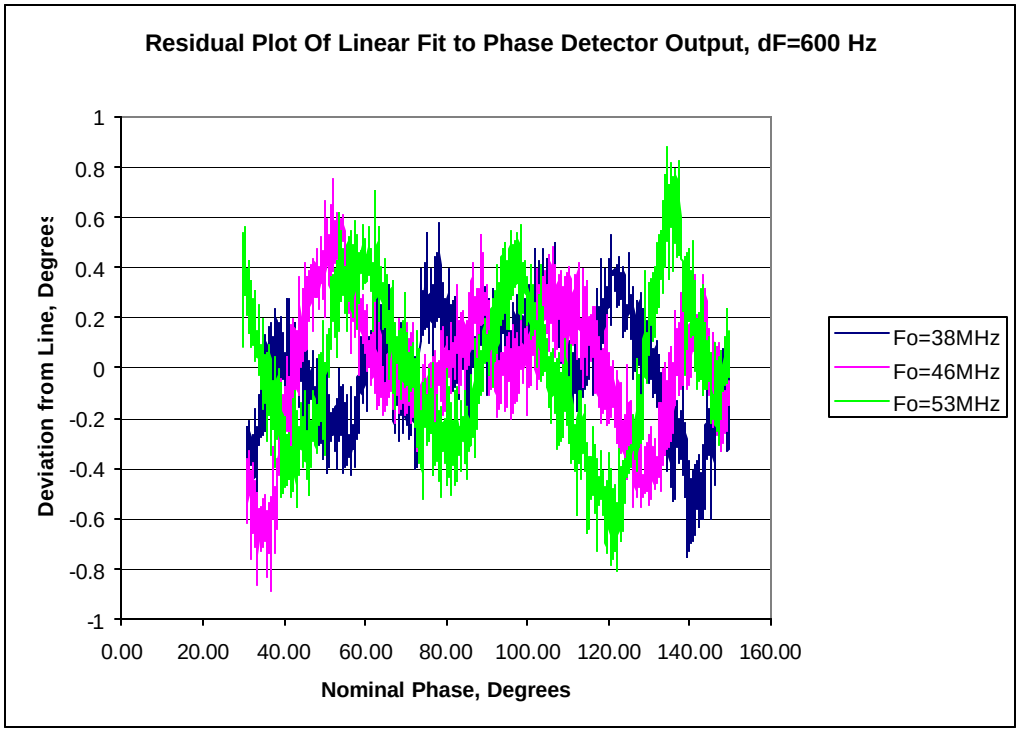

Figure IV.4.2 Linearity results from Test 4 on the Kerns Phase Detector.

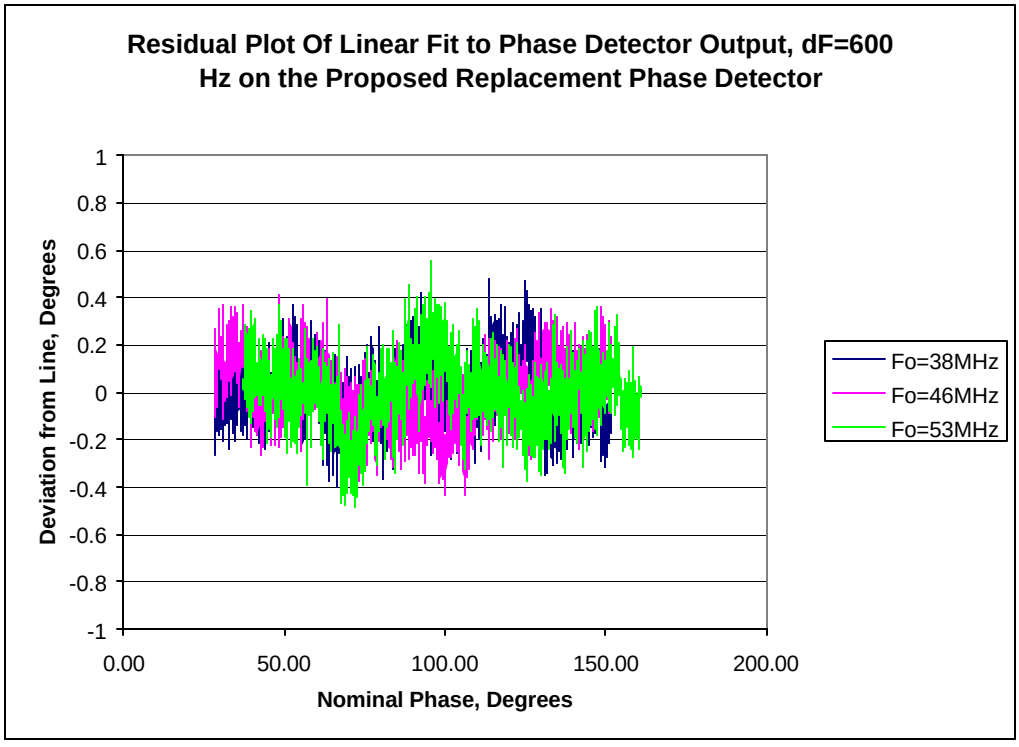

Figure IV.4.3 Linearity results from Test 4 on the AD8302 Phase Detector

IV.5 Test 5: The Notch Recovery.

There will be a flat spot in the normally continuous RF signal produced by the beam and beam pickups. This occurs when a portion of the circulating beam is notched out for the sake of reducing losses at the extraction kicker. The output of the phase detector will need to be held over the period where the beam signal is flat and the phase output is invalid. Test 5 examines the response of each phase detector to this notch in the signal.

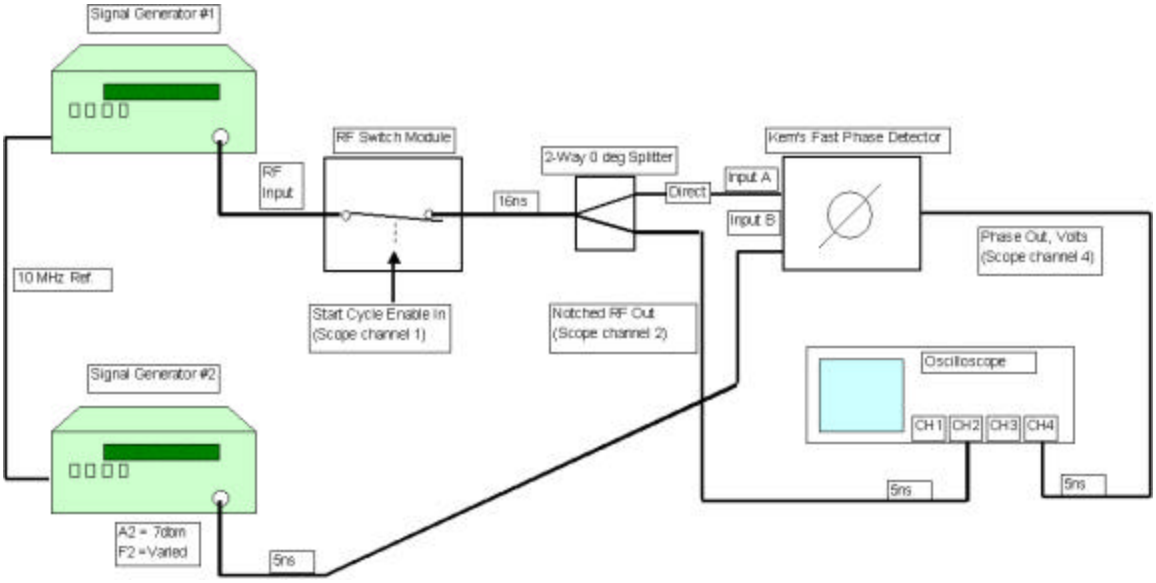

Figure IV.5.1 Setup for Test 5: Phase Detector Notch Recovery

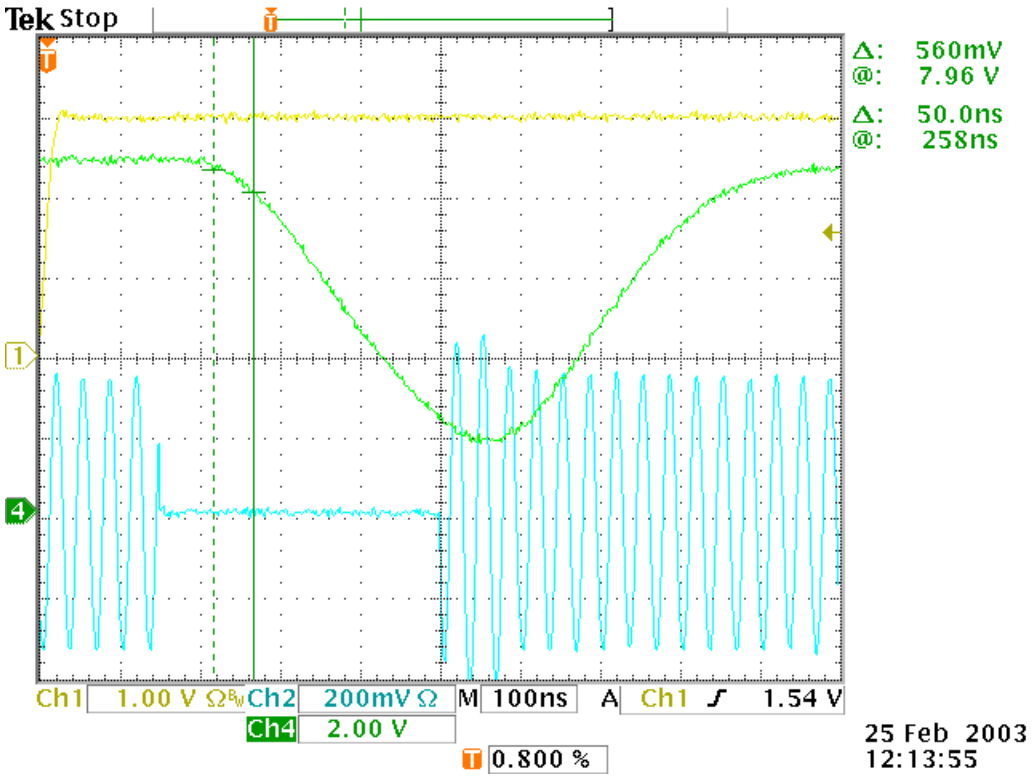

Figure IV.5.2 Response at 30 MHz and 10 bucket notch (Kerns P.D.)

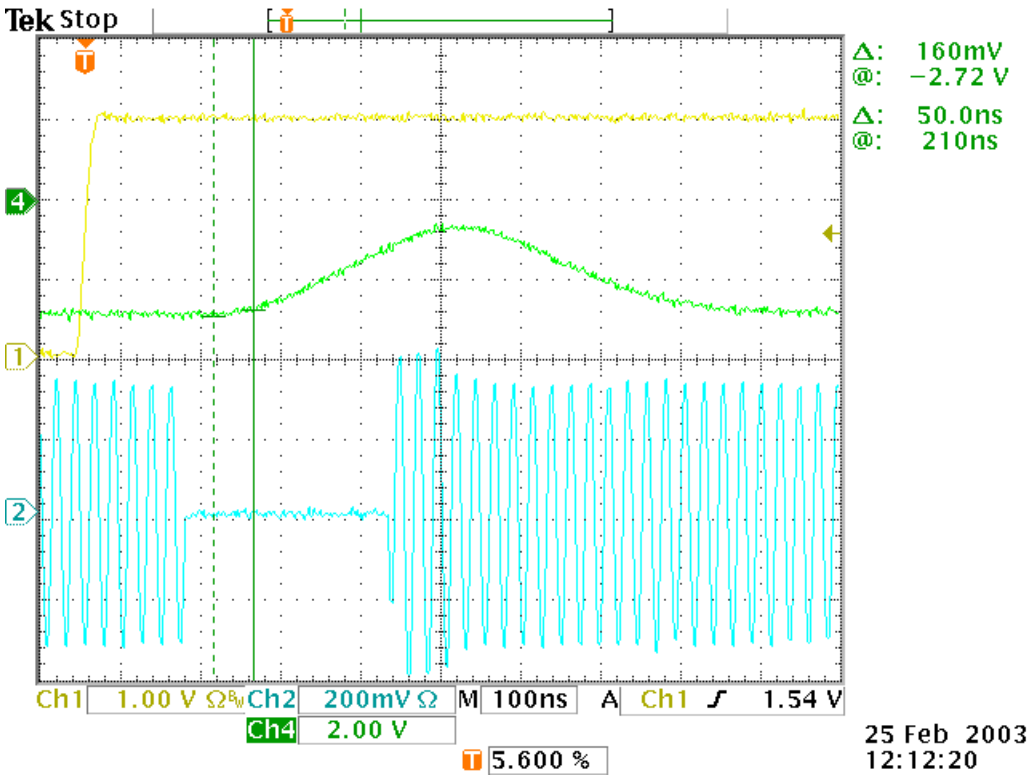

Figure IV.5.3 Response at 42 MHz and 10 bucket notch (Kerns P.D.)

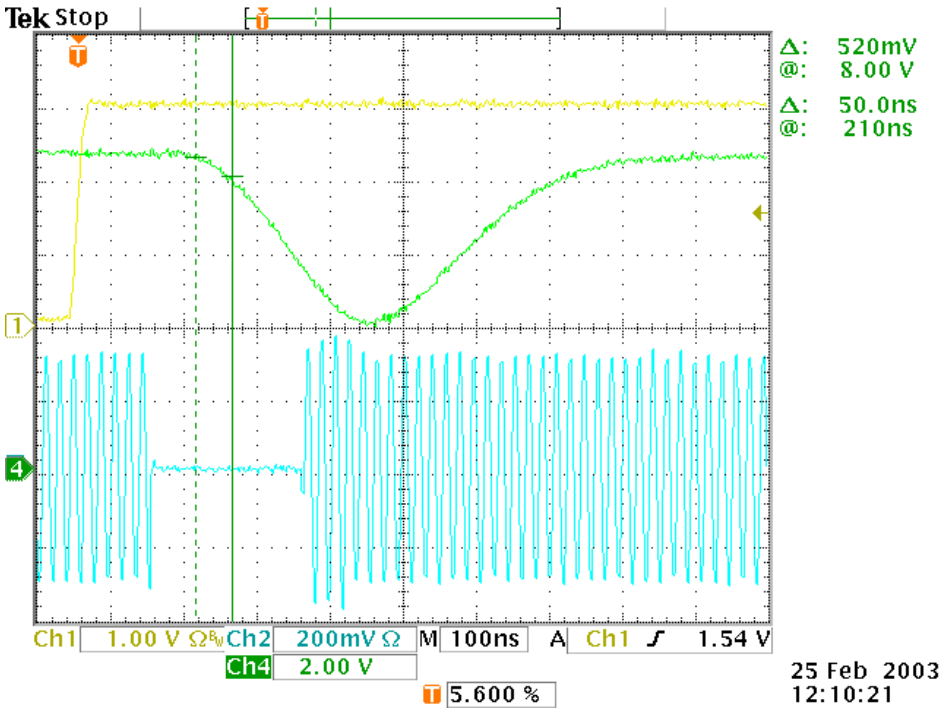

Figure IV.5.4 Response at 53 MHz and 10 bucket notch (Kerns P.D.)

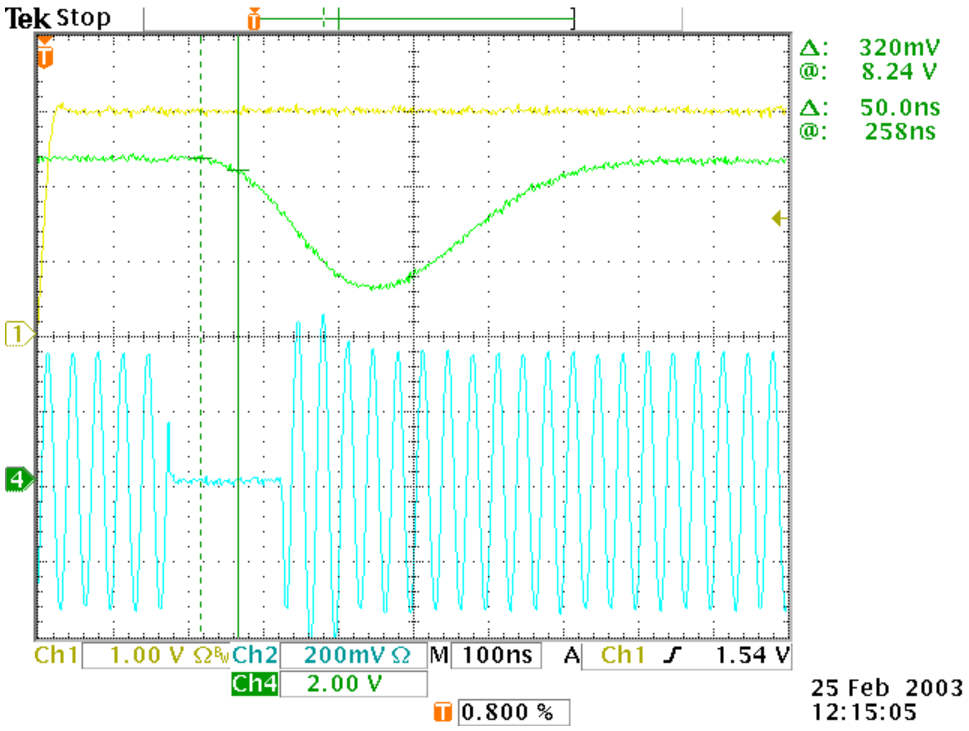

Figure IV.5.5 Response at 30 MHz and 4 bucket notch (Kerns P.D.)

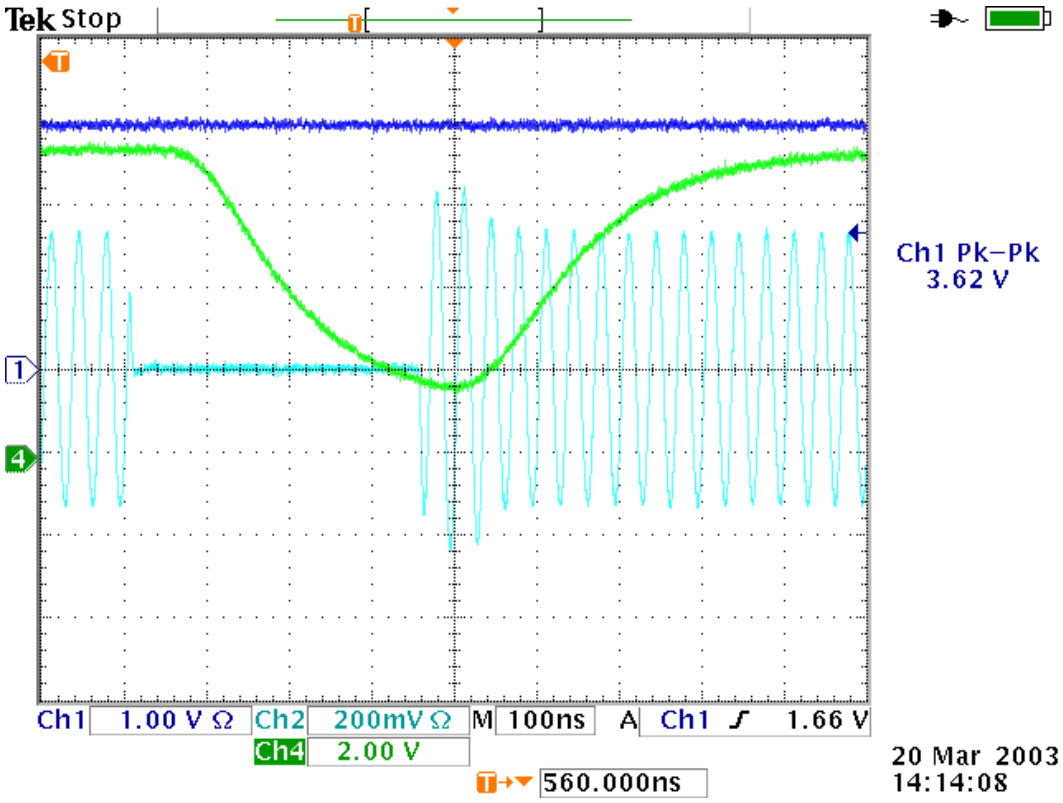

Figure IV.5.6 Response at 30 MHz and 10 bucket notch (Proposed P.D.)

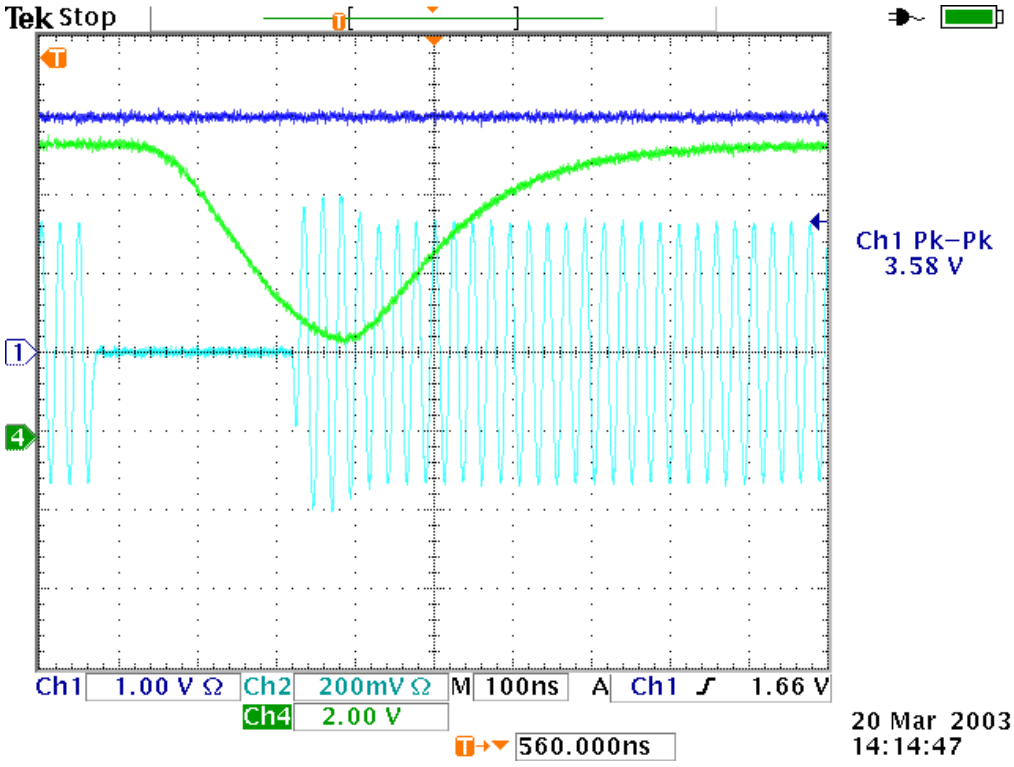

Figure IV.5.7 Response at 42 MHz and 10 bucket notch (Proposed P.D.)

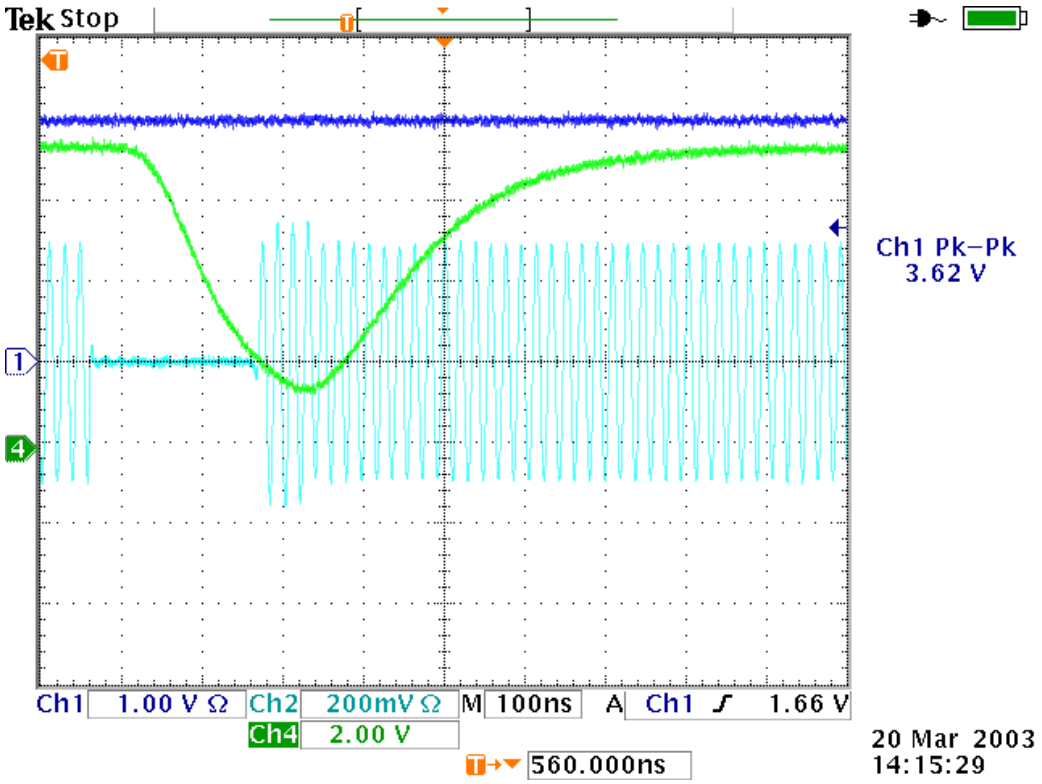

Figure IV.5.8 Response at 53 MHz and 10 bucket notch (Proposed P.D.)

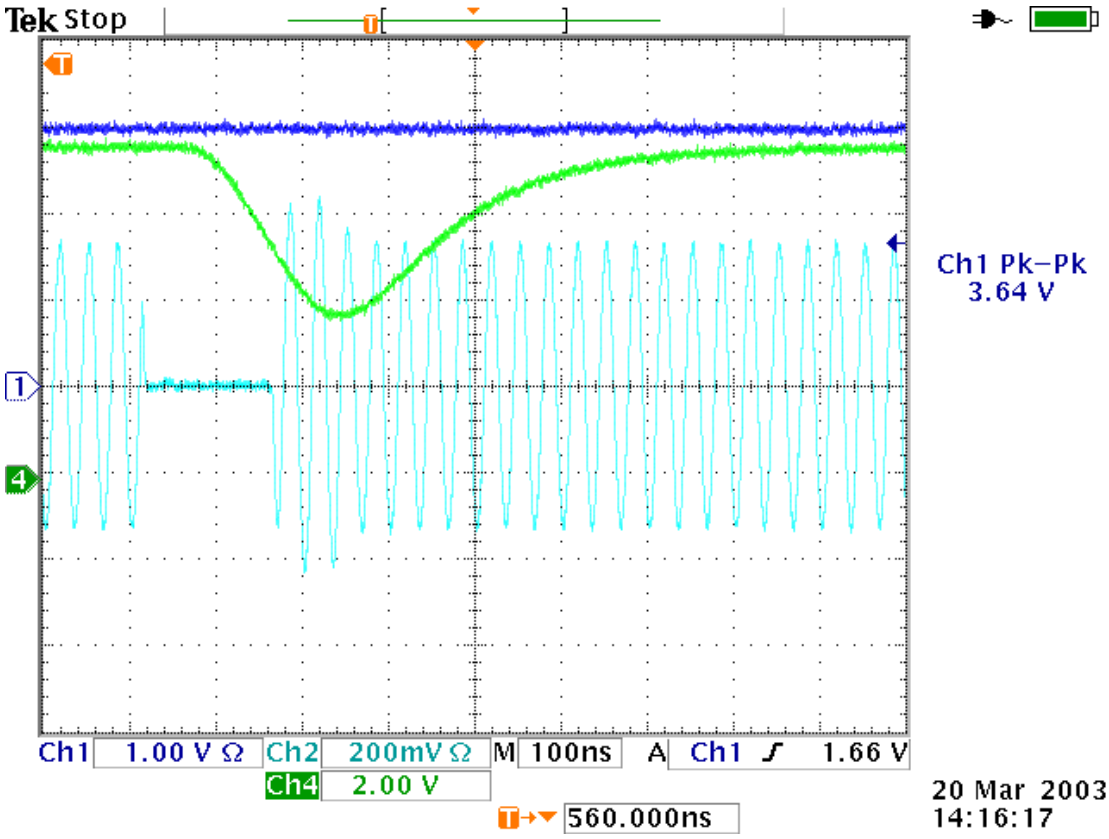

Figure IV.5.9 Response at 30 MHz and 4 bucket notch (Proposed P.D.)