Booster Beam Loss Monitor Data Acquisition and Presentation Specification

Draft for Review

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I. Introduction

This note is to specify and document how the Booster Beam Loss Monitor data is collected using the BLM Integrator/Digitizer VME modules. The following sections will describe how the BLM signals are digitized and the data managed. It will describe the different types of sums that are computed from this data.

There are several user applications that use different variations of the BLM Integrator data.

1. The base "80 µs Integration Samples" are 500 values read from each BLM channel, each Booster cycle. From these samples are derived all the other integration types.

2. The "Full Cycle Sampled Accumulations" is a running sum of the 80 µs samples over a single Booster cycle. These are similar to what you would see at the output of an analog integrator. This data is what is delivered for snapshot plots.

3. The "7.5 Hz Waveform Buffers" manage the Full Cycle Sampled Accumulations for delivery of two cycles of time stamped BLM data every other 15 Hz cycle. This data is used by certain applications, such as B136 BLM Cycle Plot.

4. The "1 ms Integrated Samples" are used for data logging for historical and Booster studies purposes.

5. The "100 Second Moving Sums" are used for control room comfort displays and alarms.

II. BLM Digitizer Module Data Acquisition

II.1 BLM Digitizer Data Processing Description

Integration and digitization of the loss monitor signals is performed by the BLM Digitizer Module. The data representing the digitized signal is buffered on the BLM Digitizer Module using FIFO memory. The output of this memory is accessible to the crate processor via the VME bus.

The module performs the following functions.

1. Digitizes the results of an analog 20.08 µs BLM charge integration into a 16 Bit Word.

2. Baseline subtraction is performed as soon as the 20.08 µs integrations are digitized.

3. Every 80.32 µs an average of 4 each 20.08 µs integrations produce a 16 Bit Word that is written to a FIFO memory.

Note that this is not strictly an 80.32 µs integrated value, but more approximately an 80.32 µs integrated value divided by 4.

4. 40.16 ms of data is collected at a rate of 12.45 kHz for each Booster cycle, resulting in 500 samples per cycle.

5. A conservative estimate for transferring one 16 Bit Word over VME is 1.0 µs. This leads to a total time of 12 ms to transfer one cycle of data for all 24 BLM channels, from the Digitizer modules to the MVME processor board.

(500 samples / channel)*(1 accesses / sample)*(24 channels)*(1.0 µs / access) = 12 ms

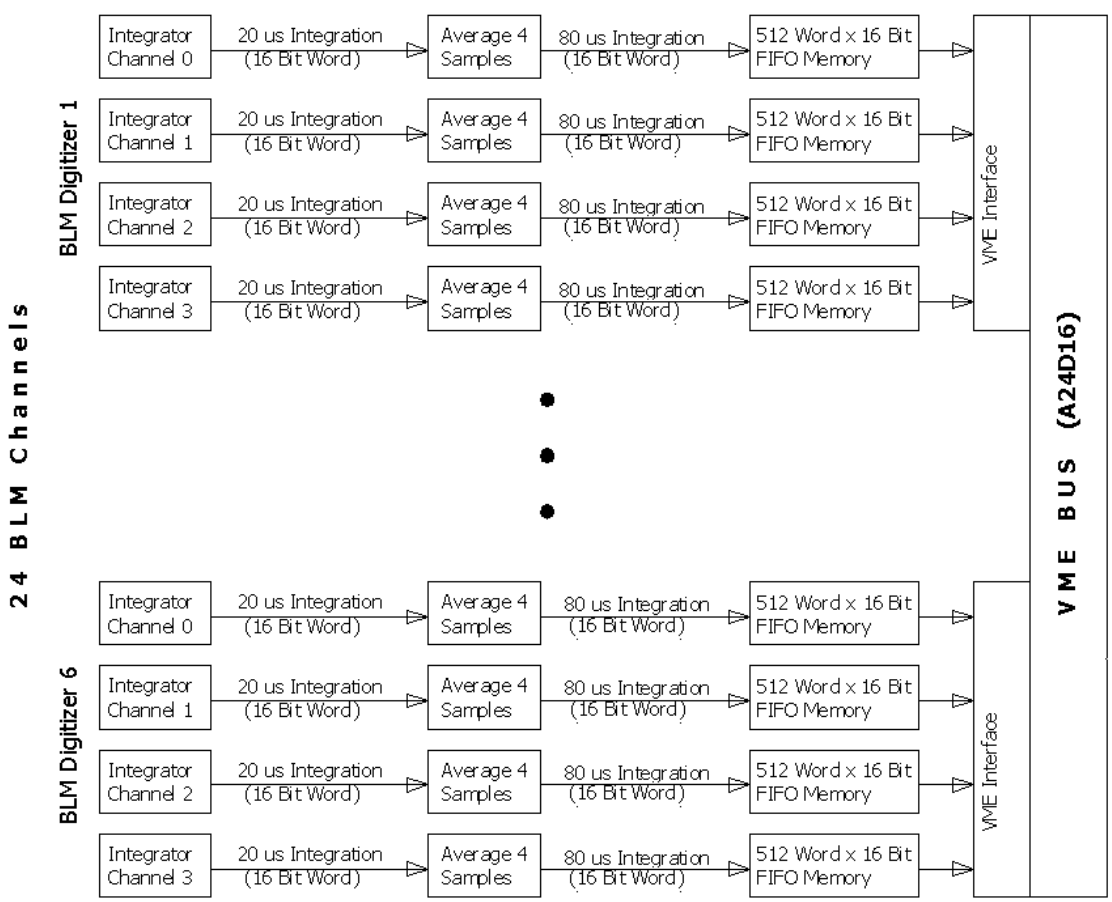

Figure II.1.1 Simplified block diagram of the BLM digitizer data processing

II.2 Scaling Digitizer Values to Rads and Rads/Second

The sealed ion chamber used in the Booster has a scale factor of 70 nano-Coulombs per Rad of radiation that passes though its cross section. The charge produced by the ion chamber is accumulated in the BLM integrating amplifiers. The integration capacitor in the normal operating mode is 100 pF, and the full scale output of the integrator is 10 Volts. Therefore the full scale output in Coulombs is

$$Q = V \cdot C = 10 \cdot 100E - 12 = 1.0\ nanoCoulomb$$

The integrator voltage is digitized with a 16 Bit ADC giving

$$\frac{1.0E - 9\ Coulombs}{65{,}535\ Counts} = \frac{15.26\ femtoCoulombs}{Count}$$

Applying the relationship between Rads and the Coulombs of charge produced by the Loss Monitor Ion chamber we get

$$\frac{15.26\ femtoCoulombs}{Count} \cdot \frac{Rad}{70\ nanoCoulombs} = \frac{0.218\ microRad}{Count}$$

This is the conversion before we *average* four integration intervals together and store the average in the FIFO from which the processor gets its values. Therefore the conversion that is to be applied to the values read from the FIFO's by the processor is

$$4\ \cdot \frac{0.218\ microRad}{Count} = \frac{0.872\ microRad}{Count}$$

The measurement made is an integration or summing of charge from the Loss Monitor ion chamber. If we wish to compute Rad/Second, the rate at which radiation is impacting the ion chamber, we must settle for the average rate over some time interval. The smallest time interval is the 20.08 µs interval that the digitized integrator values represent. Since the values written to the FIFO's is the average value over 4 each 20.08 µs intervals one can compute the Rads/Sec rate these values describe

$$\frac{1}{20.08\ microSeconds} \cdot \frac{0.218\ microRad}{Count} = \frac{0.010857\left(\frac{Rad}{Second}\right)}{Count}$$

III. Summary of the BLM DAQ Process

The following is a sketch of the BLM data acquisition process. The computation of the various types of sums is explained in more detail in the following sections.

Steps in the Process:

1. Signal digitization and collection is triggered every 15 Hz cycle on event $10.
2. The BLM signals are digitized at a rate of 12.45 kHz. Each sample represents an 80.32 µs integration interval.
3. After being triggered by event $10, the BLM signals are integrated and digitized for 40.16 ms, producing a FIFO buffer of 500 data points for each device.
4. The front end processor begins collecting data from the BLM Digitizer modules over the VME bus approximately 40 ms after event $10.
5. It is expected that the front end processor will have collected the data from 24 BLM channels by 52 ms after event $10.
6. At this point in the 15 Hz cycle, 24 each 500 point buffers will have been filled with the BLM data for the *current* cycle. This is the base “80 µs Integrated Data”.
7. 14 ms remain before the end of the 15 Hz cycle and 54 ms remain before the next VME bus transfer must begin again.
8. From the 24 buffers of 80 µs Integrated Data the 24 buffers of “Full Cycle Sampled Accumulation” data are computed.
9. From the 24 buffers of 80 µs Integrated Data the “1 ms Integration Samples” buffers are computed.
10. Using the final values of the “Full Cycle Sampled Accumulation” buffers the 17 second sums are updated and every 250th 15 Hz cycle the “100 Second Moving Sums” are updated.
11. In the remaining time before the front end is required to begin the VME bus transfers with the BLM Digitizer modules, the front end must service the ACNET requests for data. These include the data logging requests for the “1 ms Integrated Samples”, the comfort display requests for the “100 Second Moving Sums” data, and Snapshot or other plotting application requests.

IV. Signal Processing: Computing of Various Sums

Recall that within the Digitizer card the charge produced by the BLM ion chamber is integrated, or summed, over a 20 µs interval and is then digitized to produce a number. These 20 µs samples are summed into 80 µs samples. The 80 µs samples are divided by 4 to reduce the word size for transfer over the VME bus.

Within the crate processor the BLM data is stored as several different types of sums. Once the 80 µs samples are transferred to the processor, they are summed to represent longer intervals of time, and they are summed in distinctly different manners to represent the accumulation of BLM charge (beam loss) in different ways.

IV.1 The Base 80 µs Integration Samples

There is a 500 point buffer for each of the 24 channels of 80 µs integrated data read from the BLM Digitizers over the VME bus. This data is used to produce the other forms of data described below.

IV.2 The Full Cycle Sampled Accumulation.

After the 80 µs samples have been read from the Digitizer cards, the data is summed into 500 floating point values of a continuously integrating signal. That is,

$$y[i] = y[i-1] + float(x[i]), for\ i = 1 \ldots 499$$

$$y[0] = float(x[0])$$

where $y[i]$ are the continuously integrating signal samples and $x[i]$ are the 80 µs integration samples. There is a 500 point buffer of this kind for each of the 24 Booster channels.

Typically it is the last sample in this accumulation that is reported if it is desired to retrieve a single value that represents the loss during a specific cycle.

IV.3 The 1 ms Integration Samples

Each cycle, the data from the previous cycle is summed into 40 each 1 ms sums. That is,

$$w[0] = x[0] + x[1] + \cdots + x[11]\ (sum\ of\ 12\ values)$$

$$w[1] = x[12] + x[12] + \cdots + x[23]\ (sum\ of\ 12\ values)$$

$$w[2] = x[24] + x[25] + \cdots + x[35]\ (sum\ of\ 12\ values)$$

$$\vdots$$

$$w[39] = x[488] + x[489] + \cdots + x[499]\ (sum\ of\ 12\ values)$$

where $w[i]$ are the 1 ms sums. These sums are double precision floating point values. There is a 40 point buffer of this kind for each of the 12 Booster cycle types, for each of the 24 BLM channels in a crate. That is 288 (=12 x 24) of this kind of buffer per crate.

IV.4 The 100 Second Moving Sums (BLMS Support)

For each of 12 booster cycle types, for each BLM channel, 100 second moving sums are maintained. The 100 second sum is the sum of 6 each, 17 second sums. These 17 second sums are stored in a circular buffer, 6 values deep. Each time a new 17 second sum is added to the 100 second sum, the oldest 17 second sum in the circular buffer is subtracted off.

In order to compute the 17 second sums (which are actually 250, 15 Hz cycles), additional sum registers are maintained for 12 Booster cycle types, for each BLM channel. When processing the data for a specific Booster cycle type the final value of the "Full Cycle Sampled Accumulation" ($y[499]$ from equation above) is added to the 17 second sum value for that specific cycle type, for the specific BLM channel.

When a counter counting 15 Hz cycles reaches 250 (~17 seconds) the 100 second sums and their associated circular buffers are updated with the values in the 17 second sum registers. Then the 17 second sums are reset to zero.

Trip settings have been enabled on many of the Booster BLM's. This has been done in an attempt to limit losses in order to prevent excessive activation of the accelerator components. The ACNET devices to which the alarms have been applied are the B:BLxxx0 devices (where xxx is a 3 letter location description). These devices contain sums of the total losses recorded on all beam resets (event 10's) during the last 100 seconds and update every 17 seconds.

To review, there is a 17 second sum register and a 6 deep circular buffer of 17 second sums for each of the 12 Booster cycle types, for each of the 24 BLM channels.

In addition to maintaining these 100 second moving beam loss values, a 100 second moving count of the occurrence of the specific Booster reset events (those triggers which initiate the different Booster cycle types) are maintained. These are also updated by maintaining 17 second counts of the Booster reset events and 6 deep circular buffers of the 17 second counts. In this case there are only 12 sets of counts and circular buffers. One set for each Booster reset event.

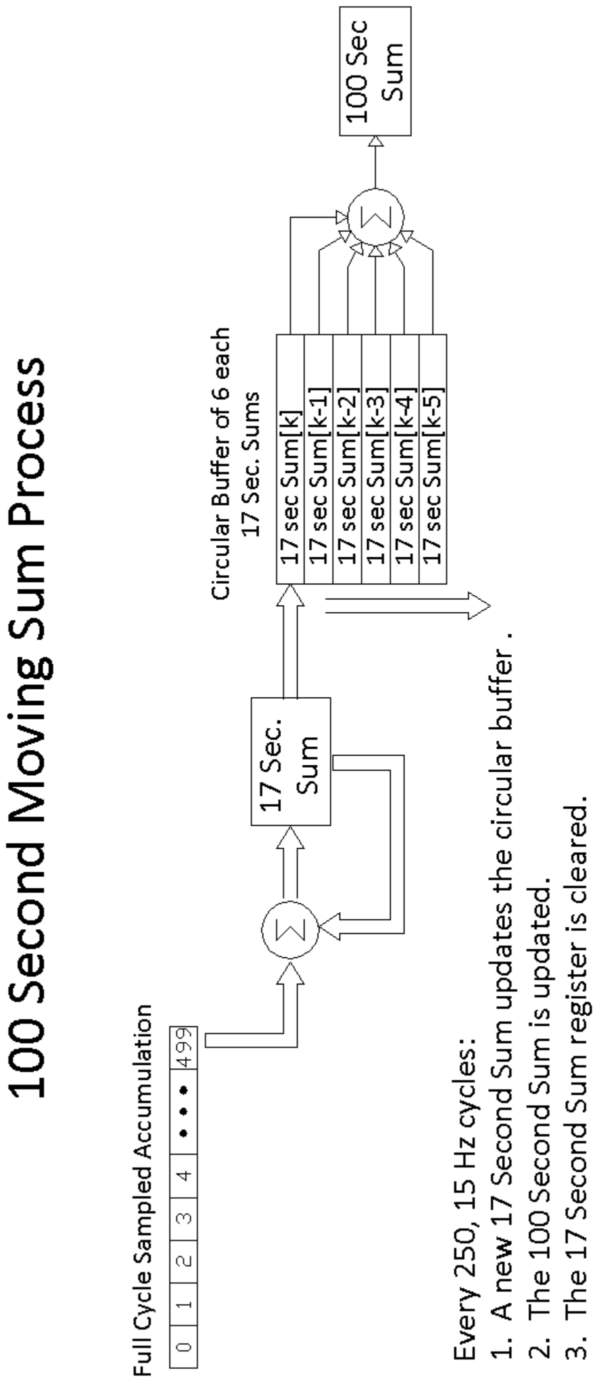

Figure IV.1 Illustration of the 100 Second Moving Sum process

IV.5 The 7.5 Hz Waveform Buffers

Requests may be made from ACNET applications to receive data for a specific set of channels on the BLM front-end processor at a 7.5 Hz update rate. Since the Booster cycles at a 15 Hz rate, two cycles worth of data are returned at the 7.5 Hz rate. The data returned is for the specified channel with no distinction with regard to the type of Booster cycle the data was collected over or whether there was even beam in the Booster during the interval. In addition to BLM data channels, there are channels that report the specific Booster reset events that may or may not have occurred over the last 133 ms (inverse of 7.5 Hz). Also along with the data is included the specific "cycle counts" for the two cycles of data in the update response. The cycle count information can be used to correlate the Booster reset event information with the data taken during the cycle the reset event triggered.

The BLM channel data will be the 500 point Full Cycle Sampled Accumulation waveform. For each BLM channel, 2 of these waveforms are transmitted to the requesting ACNET application every 133 ms.

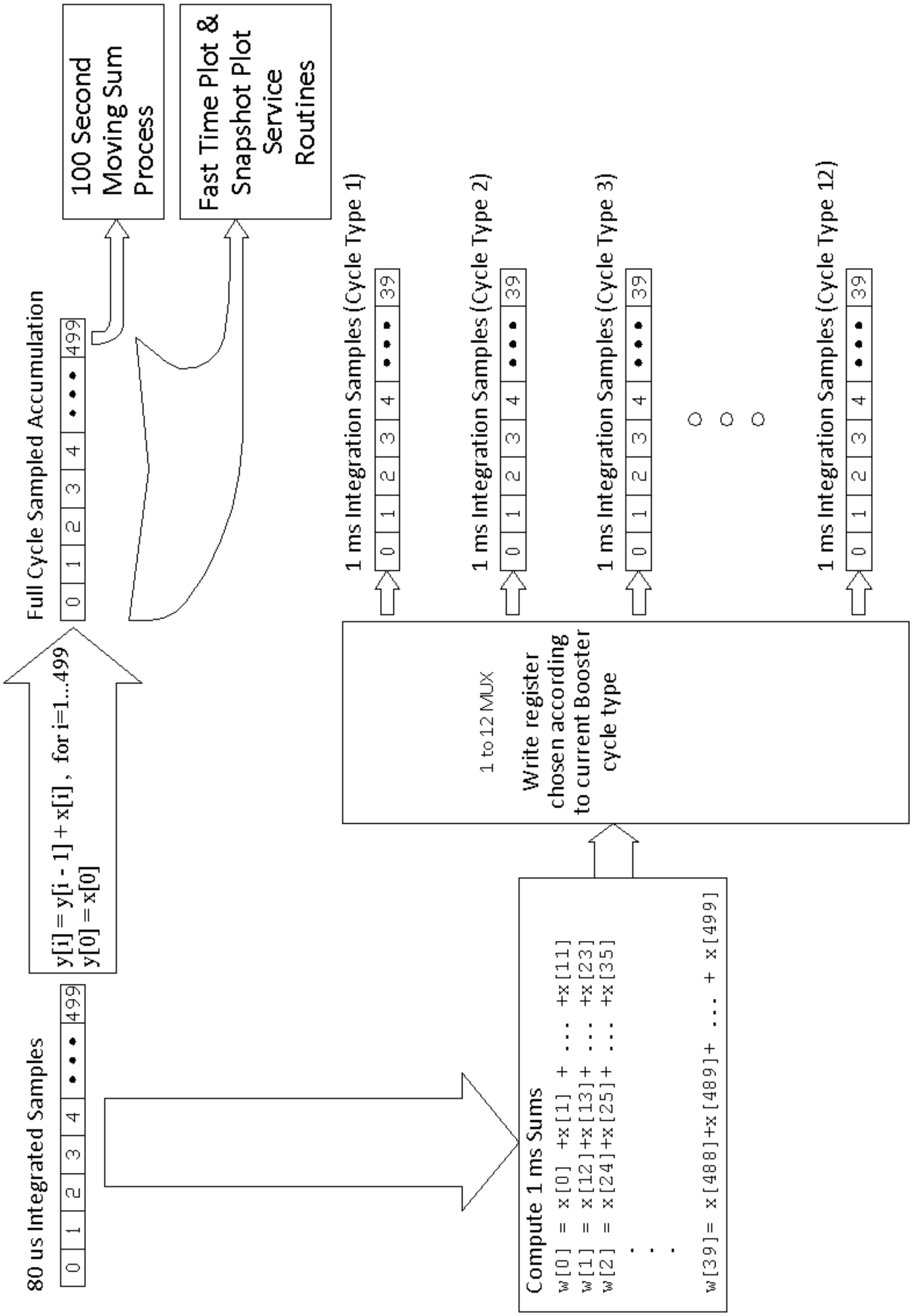

Figure IV.2 Illustration of the computed sums