Four Channel Integrator Digitizer

6U VME Module

March 14, 2005

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I. Introduction

The Four Channel Integrator Digitizer Module was developed as one of the components of the Tevatron Beam Loss Monitor Upgrade. The main features of the module are listed below.

1. There are four channels of "ping-ponged" integrators. Continuous integration of the input charge current is accomplished by connecting each input to two integrators. Charge is integrated on one integrator while the integration result of the second integrator is being digitized and the second integrator is reset.
2. The integrator outputs are digitized by a 16 bit analog to digital converter. This ADC is able to digitize at a sample rate of 500 KHz. In the BLM application it is operated at approximately 50 KHz.
3. A VME interface allows readout of the integrator data and reading and writing of various control and status registers.
4. Interfaces to a custom Control Bus and an application specific Abort Bus are provided on the J2 backplane connection.
5. Four channels of 16 bit digital to analog converters are provided for converting the digitized integrator values and other computed values into analog voltages available on the front panel.
6. There are two general purpose digital inputs and two digital outputs available for use in timing, gating or triggering.
7. All of the functions and features of the board are tied together by two large Field Programmable Gate Arrays. These FPGA's are also used to compute running sums of the integrator values and make comparisons to set "abort" thresholds used in the Tevatron BLM application.

This document is written as a design reference for understanding the details of the module.

I.1 Basic Specifications

Parameter	Conditions	Min	Typical	Max	Units
INTEGRATOR INPUT					
Current Range	DC input, Standard Range Cint = 100 pF	0		+43	μA
	DC input, High Range Cint = 500 pF	0		+214	μA
Voltage Range	DC input, Standard Range Rin = 1765 Ohms	0		+76	mV
	DC input, High Tau Range Rin = 17,760 Ohms	0		+764	mV
	DC input, High Tau and High Range (Cint = 500 pF)	0		3.80	V
Over Range Voltage	Continuous DC input before damage occurs.			+/-20	V
DIGITZER (AD7654)					
Conversion	Standard Range Cin = 100pF		15.26		fC / Count
RMS Error	Standard Range Cin = 100pF Noiseless input		7		Counts
Sample Rate			47.6		kHz
MEMORY					
Circular Buffer per Channel	16 Bit Words		65,535		Words
Injection Turn by Turn Buffer per Channel			8,192		Words
Studies Turn by Turn Buffer per Channel			8,192		Words

II. The Integrator Section

Figure II.1 is a block diagram of an integrator channel. The numbered balloons in the figure refer to the explanations given in Table II.1 of the various components of the integrator channel. The switches shown both internal to the ACF2101 integrator components and external are control by signals from the FPGA logic.

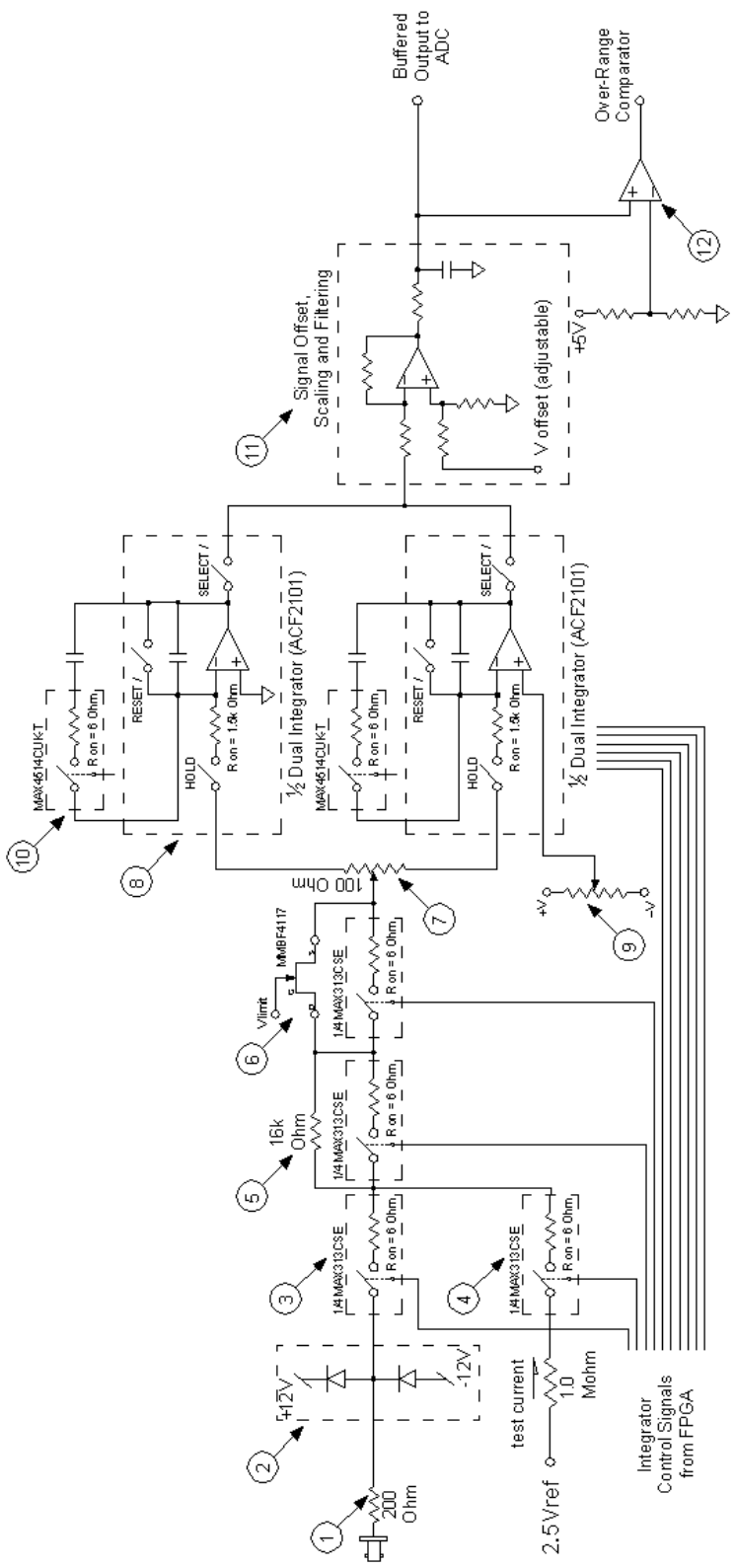


Figure II.1 Block Diagram of an Integrator Channel.

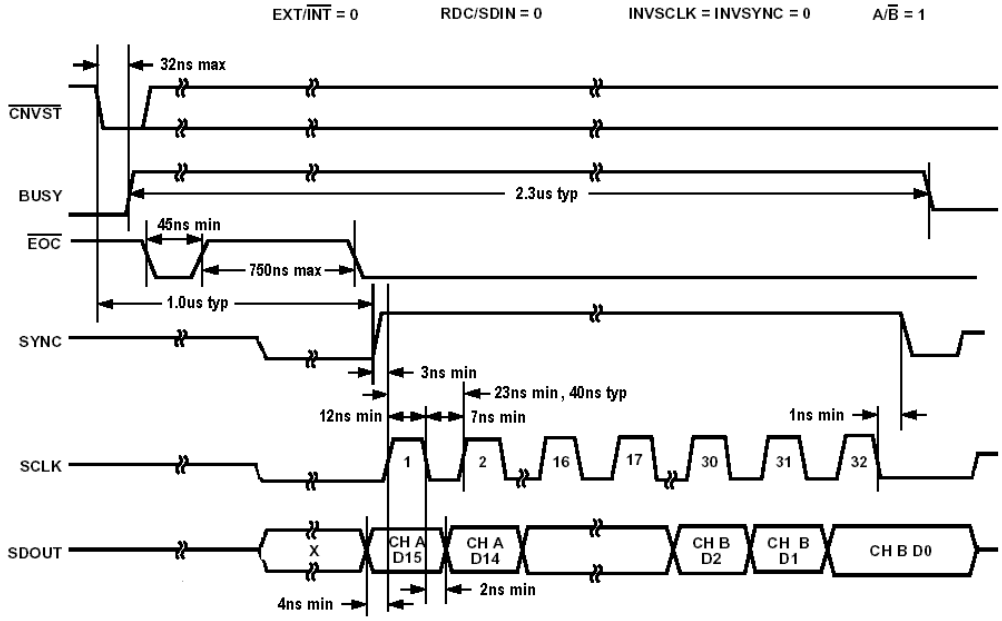
Table II.1 Description of items in Figure II.1.

Item #	Description
1	This first resistor is primarily for current limiting in an input over-voltage situation. Damage to the input components is avoided for input voltages up to 20 Volts DC.
2	These are voltage clamping diodes to protect the input analog switches. They were chosen for their very low reverse current leakage (BAV199LT1).
3	This is the on / off switch for the channel input. This switches the signal current off when using the test source and in over range input signal conditions.
4	This is the on / off switch for the test current input.
5	This is the input time constant select switch. This switch normally bypasses the signal around the 16k Ohm resistor. When the switch is open the 16k Ohm resistor is put in series with the input increasing the input signal time constant by a factor of 10.
6	This is the current limiter bypass switch. When the switch is closed the current limiting FET is bypassed. In an over-range situation the switch is opened and the current limiter is applied to the input signal charge current.
7	This is the input resistance balancing potentiometer. It is adjusted to ensure that the input resistance of each integrator for a particular channel has the same input resistance.
8	The ACF2101 dual channel precision integrator.
9	Integrator amp input offset voltage balancing potentiometer.
10	This is the integrator range select switch. When the switch is open the integration capacitance of the integrator is just the 100 pF capacitor inside the ACF2101. When the switch is closed an additional integration capacitor is added increasing the range of total charge acceptable in one integration interval.
11	This is the ADC buffer amplifier. This inverting amplifier is set for a gain of 2.
12	This comparator provides a signal to the FPGA logic if the integrator output is Over-Range. Special action is taken to avoid saturating the integrators and losing the signal charge.

III. The Digitizer Section

The four integrator signals are digitized using two AD7654AST dual channel simultaneous sampling, 500 kSPS, 16-bit SAR analog to digital converters. The integrator signals are sampled only every 21 us for the BLM application. The "Master" serial output interface of the device is used to transfer the digitized results to the FPGA's. In the "Master" serial interface mode the AD7654 generates the serial data clock used in the data transfer. Also the component option pins are set to transmit the data for both input channels only after the data conversion is complete (Read after Convert). The other options associated with the serial output of the AD7654 can be selected via jumpers on the module, but these are not used for the BLM application. See the datasheet for further details on the other options.

The timing diagram for the Master Serial Read After Convert data transfer is given in Figure III.1. The FPGA's implements the 32 bit shift register which receives the data and makes the data available to the other processing programmed into the FPGA's that write the data to RAM memory and send values out to the DAC's. The ADC serial output signals are buffered and provided to both FPGA's on the module. The upper FPGA on the module writes the data to the Turn-By-Turn buffers when a "Study" has been triggered. The lower FPGA writes the data to the Raw Data Memory circular buffer for use in computing the running sums.



Master Serial Data Timing for Reading (Read after Convert)

Figure III.1 Timing for the ADC serial data output.

Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 2.5 V	Digital Output Code
FSR – 1 LSB	4.999924 V	0xFFFF[1]
FSR – 2 LSB	4.999847 V	0xFFFE
Midscale + 1 LSB	2.500076 V	0x8001
Midscale	2.5 V	0x8000
Midscale – 1 LSB	2.499924 V	0x7FFF
–FSR + 1 LSB	–76.29 µV	0x0001
–FSR	0 V	0x0000[2]

[1] This is also the code for overrange analog input ($V_{INx} – V_{INxN}$ above 2 × (V_{REF} - V_{REFGND})).

[2] This is also the code for underrange analog input (V_{INx} below V_{INxN}).

Figure III.2 ADC output data coding.

ADD CONVERSION BETWEEN VOLTS INTO ADC AND INTEGRATOR COULOMBS

IV. Integrator Control Logic

IV.1 Standard Operation

Each integrator channel integrates continuously by connecting two integrators to the input, integrating with one while the other is being digitized and reset. The basic cycle is shown in the timing diagram of Figure IV.1.1.

V. VME Interface

The VME data transfer modes supported by the Integrator Digitizer Module are A24D16 modes.

i. Standard Supervisory Block Transfer, AM[5..0] = 3F

ii. Standard Supervisory program access, AM[5..0] = 3E

iii. Standard Supervisory data access, AM[5..0] = 3D

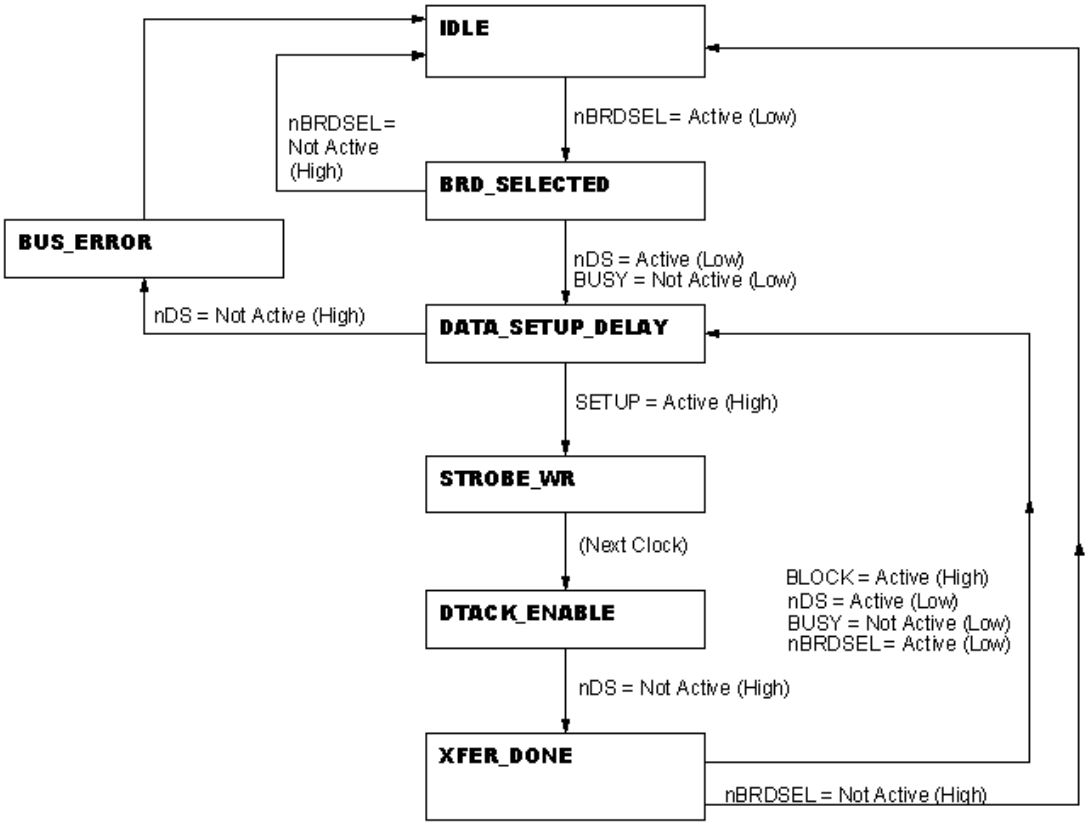
iv. Standard Non-privileged Block Transfer, AM[5..0] = 3B

v. Standard Non-privileged program access, AM[5..0] = 3A

vi. Standard Non-privileged data access, AM[5..0] = 39

Program access is treated exactly the same as data access. Supervisory modes are treated exactly the same as non-privileged modes.

The logic has mainly three main parts. The first is a state machine that handles the handshaking and timing for the VME data transfer. Figure V.1 is a representation of the state transitions. The second is an address decoder that produces the necessary latches and chip selects to Read or Write the registers implemented in the FPGA's or the SRAM data memory buffers. The address decoder portion also generates the necessary control signals for the VME data bus transceivers. The Altera AHDL logic description file for both of these blocks as well as the overall schematic tying these parts together are available on the document www page ***REFERENCE*.**



INPUTS

```
nBRDSEL = !( (nIACK & nLWORD & AM5 & AM4 & AM3 & AM1 & !AM0 & !nAS & !nAMATCH)
           # (nIACK & nLWORD & AM5 & AM4 & AM3 & !AM1 & AM0 & !nAS & !nAMATCH)
           # (nIACK & nLWORD & AM5 & AM4 & AM3 & AM1 & AM0 & !nAS & nAMATCH));
BLOCK = !nBRDSEL & AM1 & AM0; % Block transfer indication %
nDS  = nDS1 & nDS0;
BUSY = Indication that the Present Position Reg is being Read and
       the Resolver Digitizer output is not ready.
SETUP = Active when the data setup delay count reaches 10.
        Total delay is 10 time global clock period
```

OUTPUTS

```
DTACK = DTACK_ENABLE;
BERR  = BUS_ERROR;
WR_GATE / = !DATA_SETUP_DELAY;
RD_GATE /  = !(DATA_SETUP_DELAY # STROBE_WR # (DTACK_ENABLE & !nDS) );
```

Figure V.1 VME interface state transition diagram.