

IMPROVED NOISE PERFORMANCE OF THE ACF2101 SWITCHED INTEGRATOR

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The signal-to-noise ratio and bandwidth of the combination of the ACF2101 dual, switched integrator and a low-level input current is exceptional when compared to the performance of a classical transimpedance amplifier (Figure 1). To further improve the ACF2101 signal-to-noise ratio, a resistor can be added in series with the input sensor.

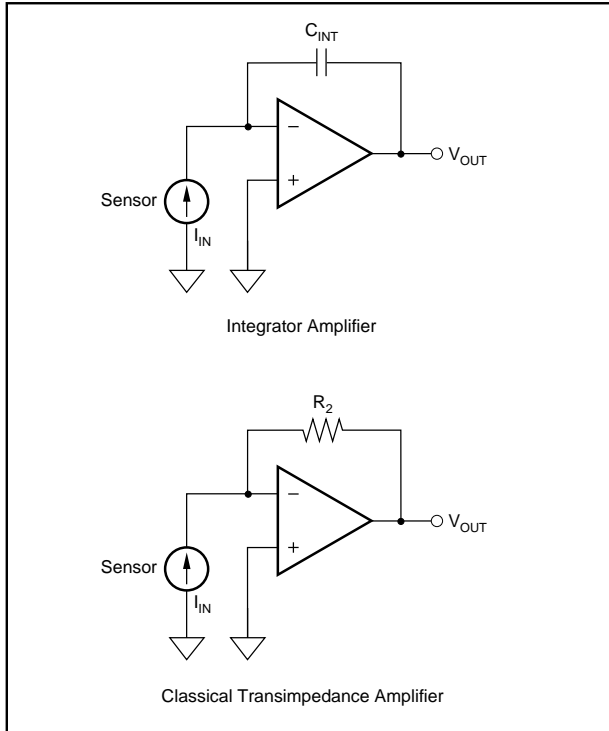


FIGURE 1. Typical Circuits Used to Convert Current Signals to Voltage.

The ACF2101 is a dual switched integrator, as shown in Figure 2. The current from the sensor is integrated by the capacitor (C_{INT}) in the feedback loop of the amplifier. Since the inverting input of the amplifier is kept at a virtual ground, the output of the integrator changes in a negative direction over time. The resulting transfer function of the switched integrator is:

$$V_{OUT} = \frac{-1}{C_{INT}} \int_0^t I_{IN} dt$$

Where:

V_{OUT} = output voltage of op amp

C_{INT} = integration capacitor

I_{IN} = sensor current

The output of the ACF2101 switched integrator is a time averaged representation of the input.

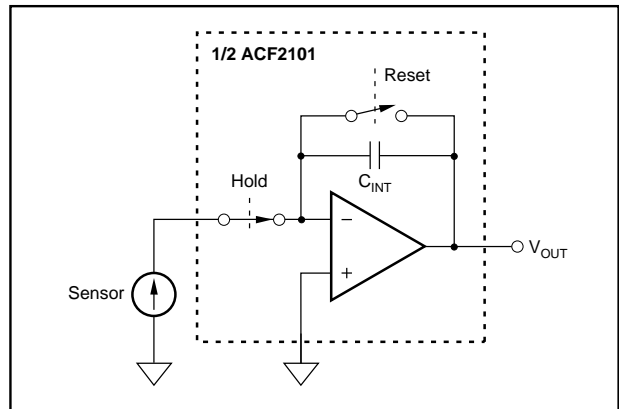


FIGURE 2. The ACF2101 Switched Integrator Block Diagram.

Once the ACF2101 has integrated the input signal over a predetermine period, the HOLD switch is opened, allowing the user to read the output of the switched integrator at a held voltage. The HOLD switch performs a sample/hold function on the signal. Once the signal is read, the RESET switch is closed in order to discharge the integration capacitor, C_{INT} , and bring the output back to the same potential as the inverting input of the amplifier. Once the output returns to ground, the RESET switch is opened. Shortly after the RESET switch is opened, the HOLD switch closes to start the integration cycle again.

Typically, a photodiode is used as the sensor for both circuits shown in Figure 1. A photodiode can be modeled using the sensor model shown in Figure 3. This model includes a current source (I_{IN}), parasitic resistor (R_1), and parasitic capacitor (C_1). Typical values of R_1 range from 100k Ω to 100G Ω . Typical values of C_1 range from 20pF to 1000pF. C_1 can be higher if the sensor is placed at a remote location, and a cable, with parasitic capacitance to ground, is used to transmit the signal to the input of the switched integrator.

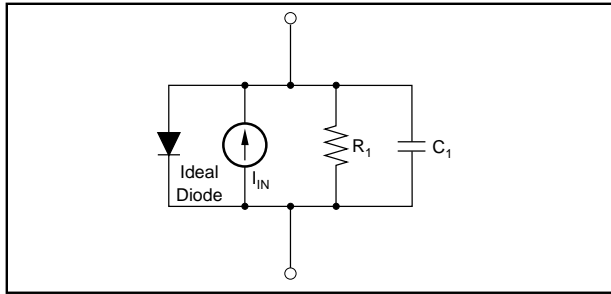


FIGURE 3. Photodiode Model Used in Noise Analysis.

The noise model for the complete photodiode/switched integrator application is shown in Figure 4. In most applications the switched integrator is in the integrate mode for most of the total integration cycle. The model in Figure 4 represents the ACF2101 with the HOLD switch closed and the RESET switch opened. The typical on-resistance of the HOLD switch is 1.5kΩ, and the typical open-resistance of the RESET switch is 1000GΩ.

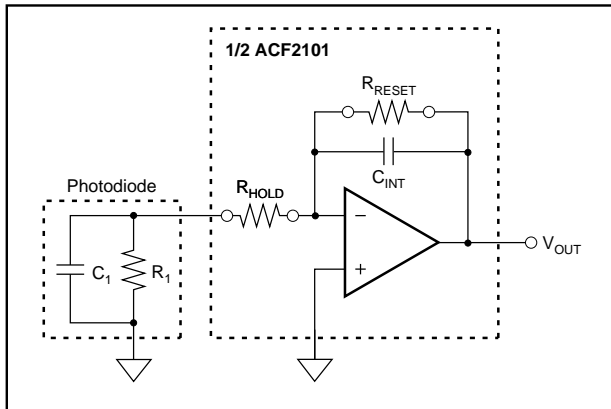


FIGURE 4. ACF2101 Switched Integrator and Photodiode Model Used for Noise Analysis.

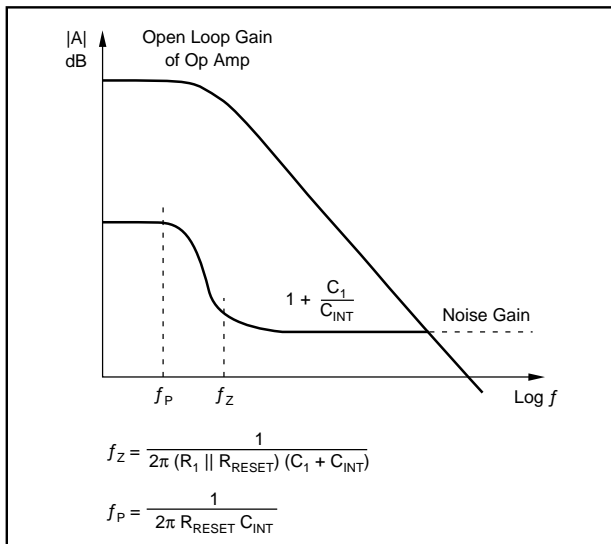


FIGURE 5. Noise Gain of the ACF2101, Switched Integrator.

The three dominate sources of noise at the output of the switched integrator are the gained op amp noise, the charge injection noise of the switches and the kT/c noise of the integration capacitor. A bode plot of the op amp noise gain of the switched integrator is shown in Figure 6. The low-frequency pole of the noise gain is equal to:

$$f_p = \frac{1}{2\pi R_{RESET} C_{INT}}$$

This pole is usually found at very low frequencies. For example, if $R_{RESET} = 1000G\Omega$ and $C_{INT} = 100pF$, the pole would occur at 0.00159Hz.

The zero of the noise gain plot is equal to:

$$f_z = \frac{1}{2\pi (R_1 \parallel R_{RESET}) (C_1 + C_{INT})}$$

This zero is also usually found at very low frequencies. For example, if $R_1 = 100M\Omega$, $C_1 = 50pF$, $R_{RESET} = 1000G\Omega$, and $C_{INT} = 100pF$, f_z would equal 10.6Hz.

As a consequence, the op amp output noise of the switched integrator is dominated by the high frequency op amp noise multiplied by:

$$\text{High frequency noise gain} = \left(1 + \frac{C_1}{C_{INT}} \right)$$

The total rms noise can be estimated as equal to:

$$\text{NOISE}_{OP AMP} = 10 \left(1 + \frac{C_1}{C_{INT}} \right) \mu\text{Vrms}$$

The charge injection noise of the switches and the integration capacitor noise both have broad band noise equivalent to 10μVrms. The total characterized noise of the ACF2101 switched integrator with various input capacitance and integration capacitance is shown in Figure 6.

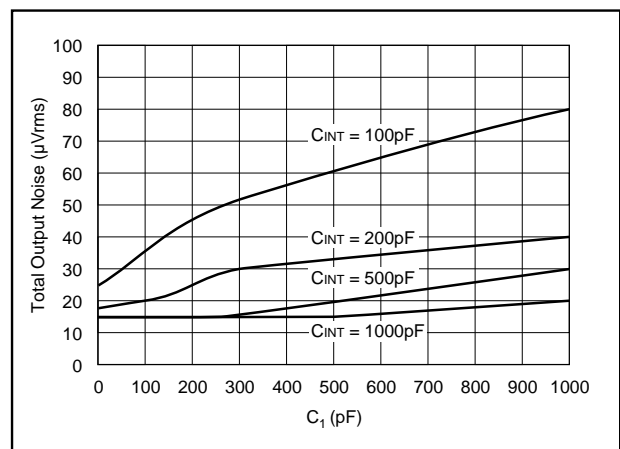


FIGURE 6. Total Output Noise of the ACF2101 Switched Integrator vs Parasitic Photodiode Capacitance, C_1 , and the ACF2101 Integration Capacitor, C_{INT} .

To further improve the signal-to-noise ratio of the ACF2101 switched integrator, a resistor can be added in series with the sensor, as shown in Figure 7. This additional resistor, R_N , in series with R_{HOLD} , adds a pole/zero pair at higher frequencies. When R_N equals 0Ω , the pole/zero pair generated by HOLD switch on-resistance ($R_{HOLD} = 1.5k\Omega$) occurs at frequencies close to the open loop gain of the amplifier. As shown in the bode plot in Figure 8, R_N plus R_{HOLD} attenuates high frequency noise.

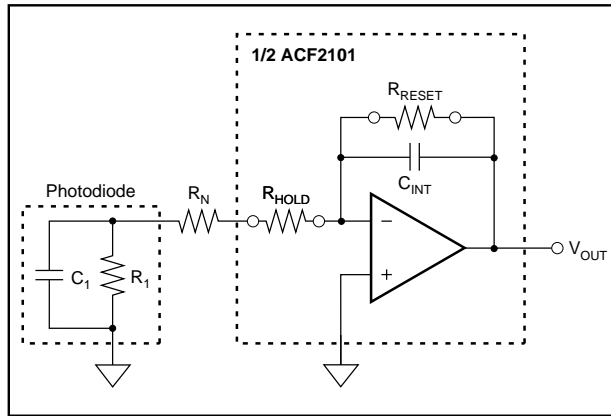


FIGURE 7. The ACF2101 Switched Integrator with an Additional Resistor, R_N , Added in Series with the Photodiode to Reduce Noise.

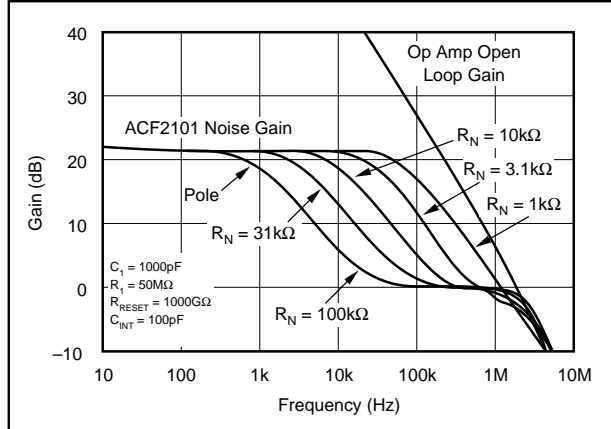


FIGURE 8. Noise Gain Plots of ACF2101 with an Additional Resistor, R_N , in Series with the Photodiode.

An application example is shown in Figure 9. The photodiode is modeled with a parasitic capacitance of 1000pF and parasitic resistance of 50MΩ. The integration capacitor used in the feedback loop of the op amp in the ACF2101 is equal to 100pF. The 20-bit, 40kHz ADC750 A/D converter block diagram is shown in Figure 10. Extreme care should be taken to properly guard the high impedance input pins of the ACF2101 in order to reduce the possibility of coupled noise into the signal.

The design trade-off for improved noise performance of the switched integrator is a slight degradation in the linearity performance of the photodetector. The current from the sensing device will cause an IR drop across R_N . This IR drop will impress a voltage across the sensor, causing a small degree of dark current to start to conduct. As shown in Figure 8, the pole generated by the additional resistor, R_N , is equal to:

$$\text{Pole} = \frac{R_N + R_1 + R_{HOLD}}{2\pi R_1 (R_N + R_{HOLD}) C_1}$$

The pole is directly affected by the value of R_N and C_1 (photodetector parasitic capacitance). Higher values for C_1 will reduce the noise without compromising the linearity performance of the photodetector. The overall circuit performance is best optimized when the photodetector parasitic capacitance, C_1 , is 200pF or greater.

The ACF2101 switched integrator is optimized for good noise and bandwidth performance for low-level input currents. The addition of a resistor in series with the photodiode further improves the noise performance without sacrificing bandwidth.

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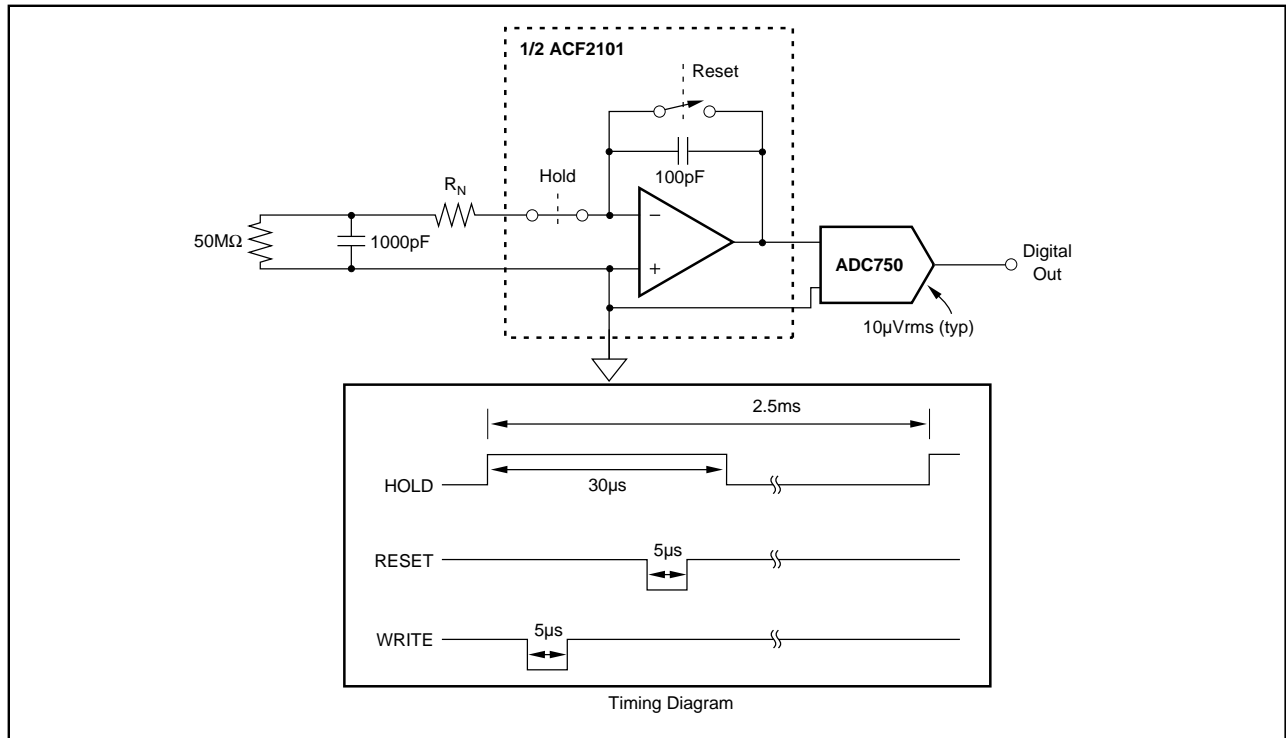


FIGURE 9. Circuit and Timing Diagram used to Test the Noise Performance of the ACF2101 with and without R_N .

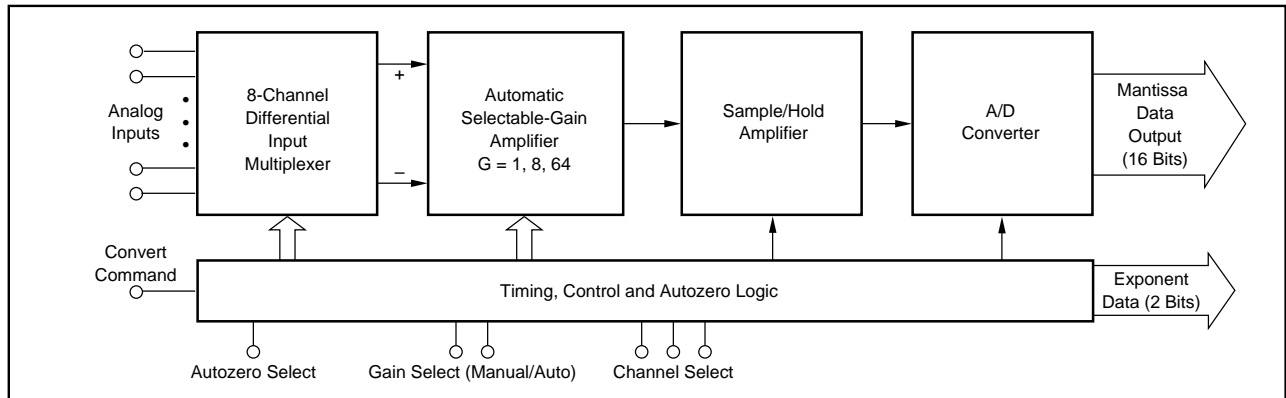


FIGURE 10. Block Diagram of ADC750 A/D Converter.