Dual Phase Detector 2 Module Checkout and Diagnostics

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Module Number: ________________________________

Technician: _____________________________________

Date/Time: _____________________________________

Contents

Introduction

The Dual Phase Detector Module is basically a NIM module providing two AD8302 phase detectors, two ADC converters, three DAC analog outputs, 8 digital inputs and 8, 50 Ohm digital outputs all tied together with an Altera Cyclone FPGA. The module also includes 64kx16 SRAM memory, Flash memory for parameter storage, a USB PC interface with PC Windows interface software and an Ethernet port that we have hopes of writing the firmware for in the near future.

The first application this module is being developed for is as a replacement for the Main Injector Phase Lock controls in the Booster LLRF system.

Bench Setup

Test Equipment Needed:

1. Dual channel RF sine wave generator capable of setting the phase between the two signals. This can be accomplished with the following equipment we have on hand; Tektronix AWG520, Agilent 81150A, or the Tektronix AFG3102.
2. An additional signal generator is needed to produce TTL square wave and pulse signals.
3. DVM Voltmeter.
4. Thermal imaging camera.
5. Oscilloscope.

Test Software Requirements

The PC test interface program and the associated USB drivers need to be loaded onto the PC used for the tests. The Dual Phase Detector uses a USB to 8 bit FIFO interface chip from FTDI, the UM245R. Drivers and documentation for this device are available from www.ftdichip.com. The necessary drivers and instructions for installing them are included in the PC folders.

Test Procedure

Proceed through the following and make the engineer aware of any anomalous behavior.

Power-up Checks

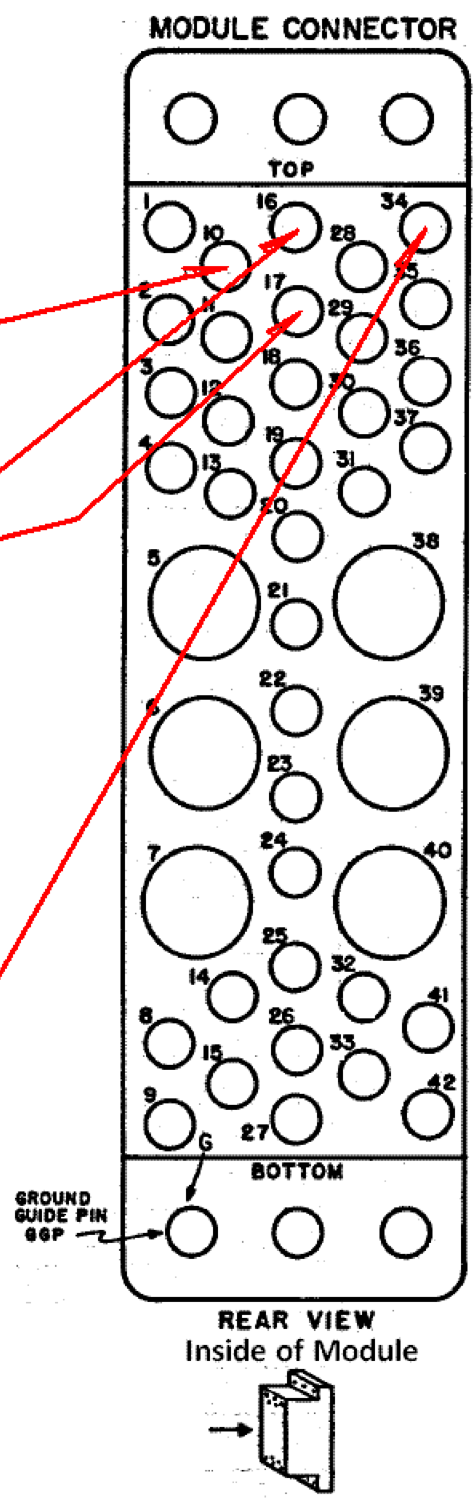
1. Ohm from one leg of each fuse listed in Table XX.1 to ground and enter the value measured in the table. Do not proceed to powering the module if the value is beyond the listed tolerance values. Note: Take the measurement after the on-board capacitance has charged and the reading stops going up.

Table XX.1

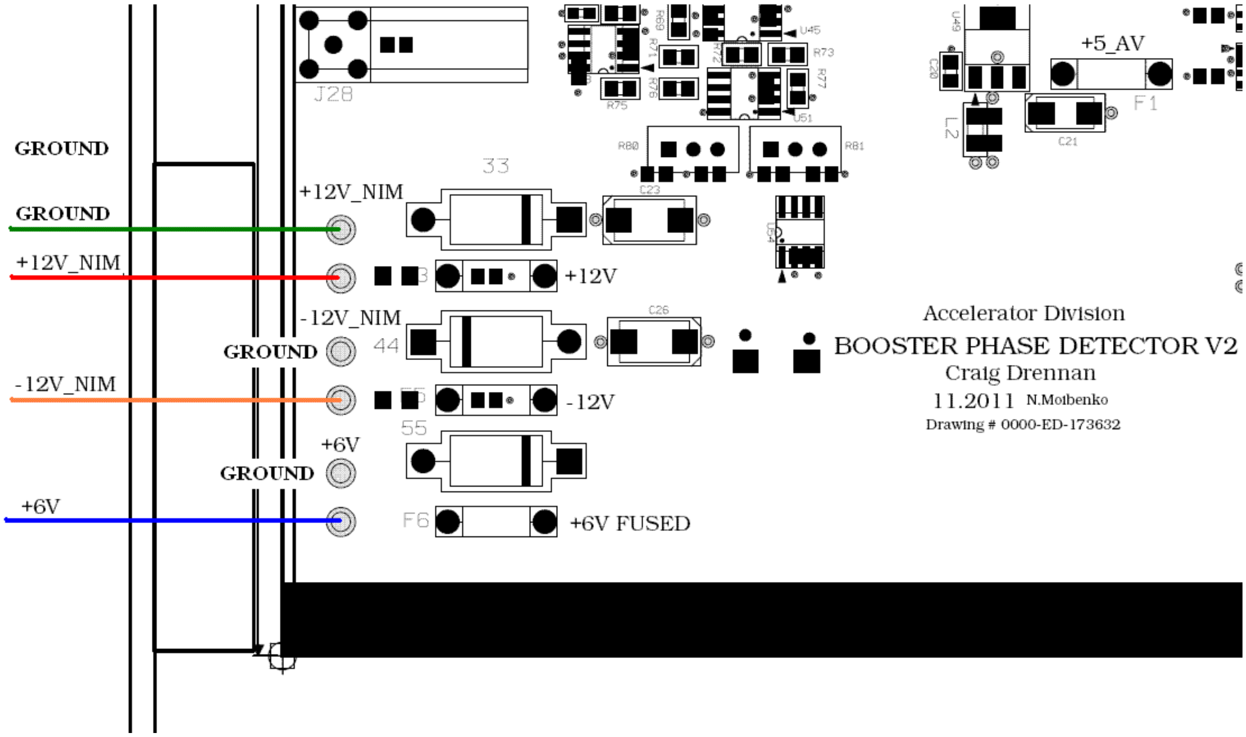
Fuse	Assoc. Voltage	Enter Measured Ohms	Previously Measured	Tolerance
F3	+12 V		56k	20k to 100k
F5	-12 V		46k	20k to 100k
F6	+6 V		11k	2k to 20k
F1	+5 V (analog)		3k	800 to 8k
F2	+1.5 V		223	150 to 500
F4	+3.3V		707	330 to 1500
F7	+5 V (digital)		9.5k	5k to 15k

2. Verify that the power connections have been wired correctly to the NIM Power Connector. See the figure below

PIN	FUNCTION
1	RESERVED
2	RESERVED
3	SPARE
4	RESERVED
5	
6	
7	
8	+200 VOLTS D.C.
9	SPARE
10	+6 VOLTS
11	-6 VOLTS
12	RESERVED
13	SPARE
14	SPARE
15	RESERVED
16	+12 VOLTS
17	-12 VOLTS
18	SPARE
19	RESERVED
20	SPARE
21	SPARE
22	RESERVED
23	RESERVED
24	RESERVED
25	RESERVED
26	SPARE
27	SPARE
28	+24 VOLTS
29	-24 VOLTS
30	SPARE
31	SPARE
32	SPARE
33	117 VOLTS A.C. (HOT)
34	POWER RETURN GND
35	RESET
36	GATE
37	SPARE
38	
39	
40	
41	117 VOLTS A.C.(NEUTRAL)
42	HIGH QUALITY GND
G	GROUND GUIDE PIN



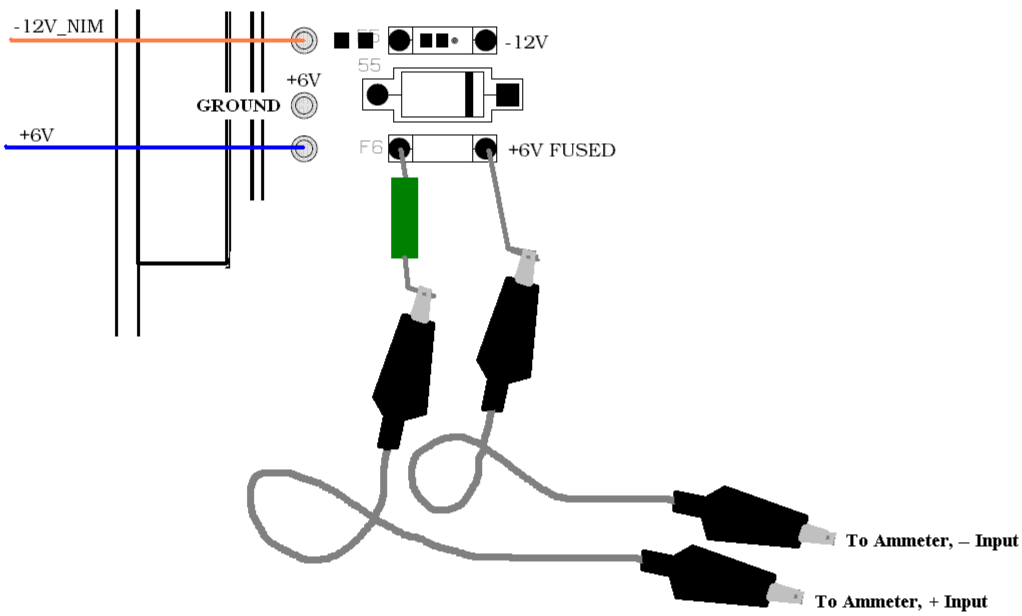
NIM power connector pin assignments.


GROUND
GROUND
+12V_NIM
-12V_NIM
+6V
J28
33
+12V_NIM
+12V
-12V_NIM
44
GROUND
-12V
55
+6V
GROUND
F6
+6V FUSED
R80
R81
C23
C26
+5_AV
F1
C21
L2
Accelerator Division
BOOSTER PHASE DETECTOR V2
Craig Drennan
11.2011 N.Molbenko
Drawing # 0000-ED-173632

3. Disconnect one leg of the +6V Fuse, F6 and insert an ammeter using alligator clips and a resistor lead similar to Figure XX.3. Power the module briefly, note the ammeter reading and then power off the module.

+6 V Initial Current Draw	=	___________ mA

**If the ammeter reading exceeds 800 mA, do not power the board again and seek assistance.*



4. Prepare the Thermal Imaging Camera, power the module and monitor the top surface of the module for temperatures between 20 degC and 80 degC. Note any areas exceeding 65 degC and seek assistance.

Maximum Temperatures	=	________________________ degC

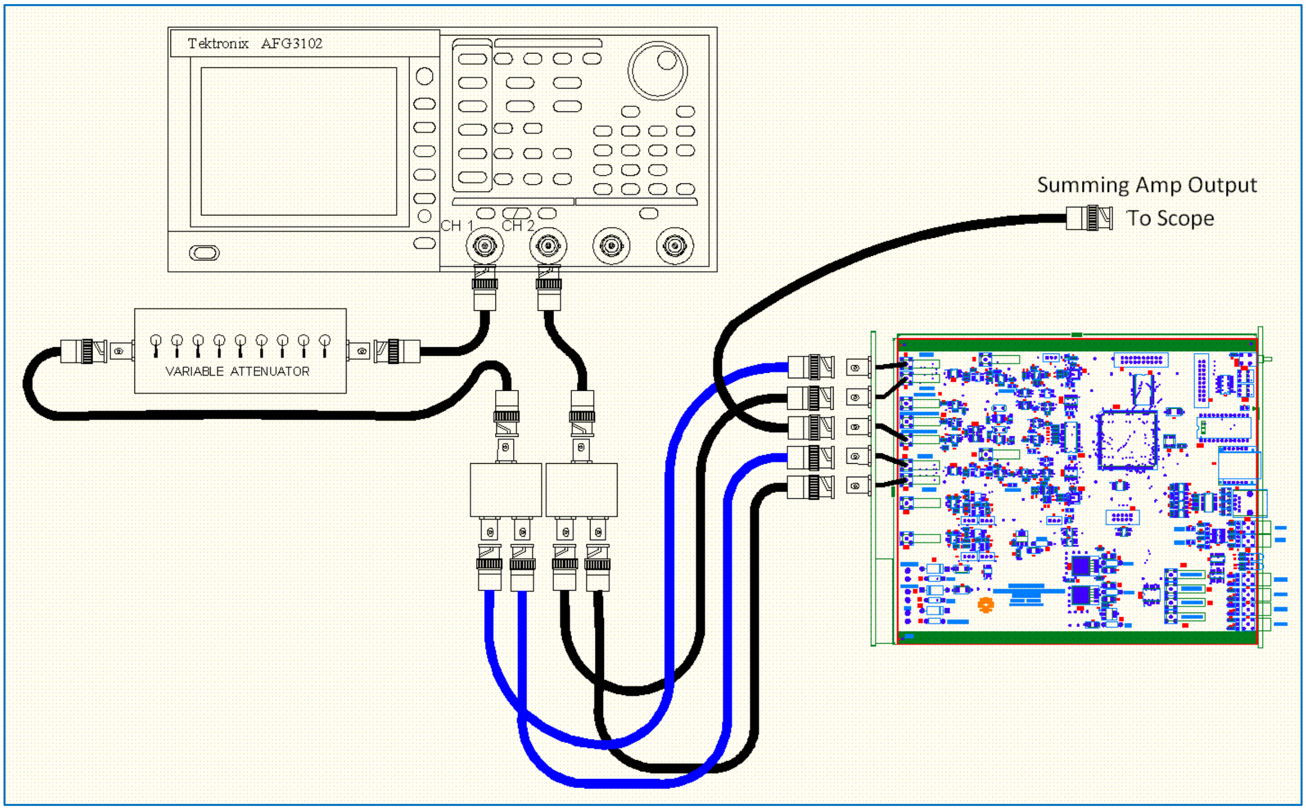
5. Power the module and measure and record all of the voltages at the fuses listed in the table below.

Fuse	Nominal Voltage	Measured, Volts	Previously Measured, Volts	Tolerance, Volts
F3	+12 V		11.905	11.9 to 12.0
F5	-12 V		-11.952	-12.0 to -11.9
F6	+6 V		5.960	5.8 to 6.0
F1	+5 V (analog)		4.910	4.9 to 5.1
F2	+1.5 V		1.494	1.48 to 1.51
F4	+3.3V		3.304	3.28 to 3.31
F7	+5 V (digital)		4.909	4.9 to 5.1

Setup Test Equipment and Program FPGA

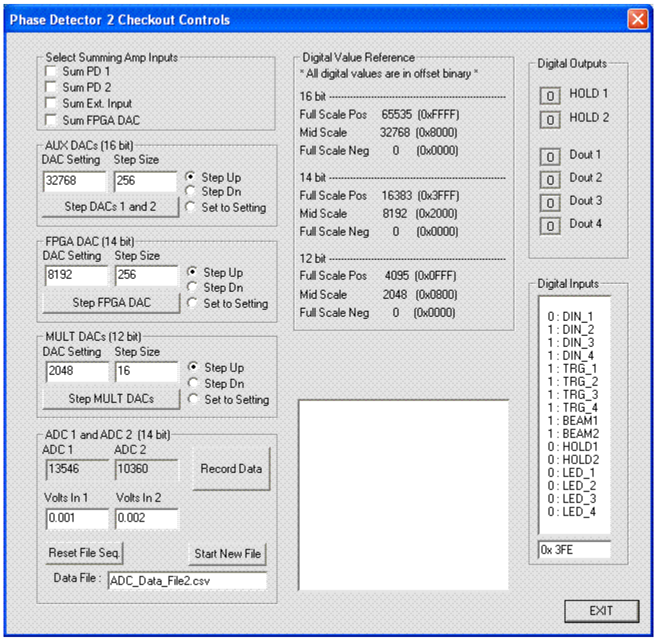
6. Program the FPGA using the prescribed Altera file “phasedet1.pof” provided in the PC folders setup for doing the testing.

7. Connect the signal generator as shown in the figure below. Setup Channel 1 and Channel 2 for 50 MHz sine waves at 0.4 Vpp into 50 ohms.

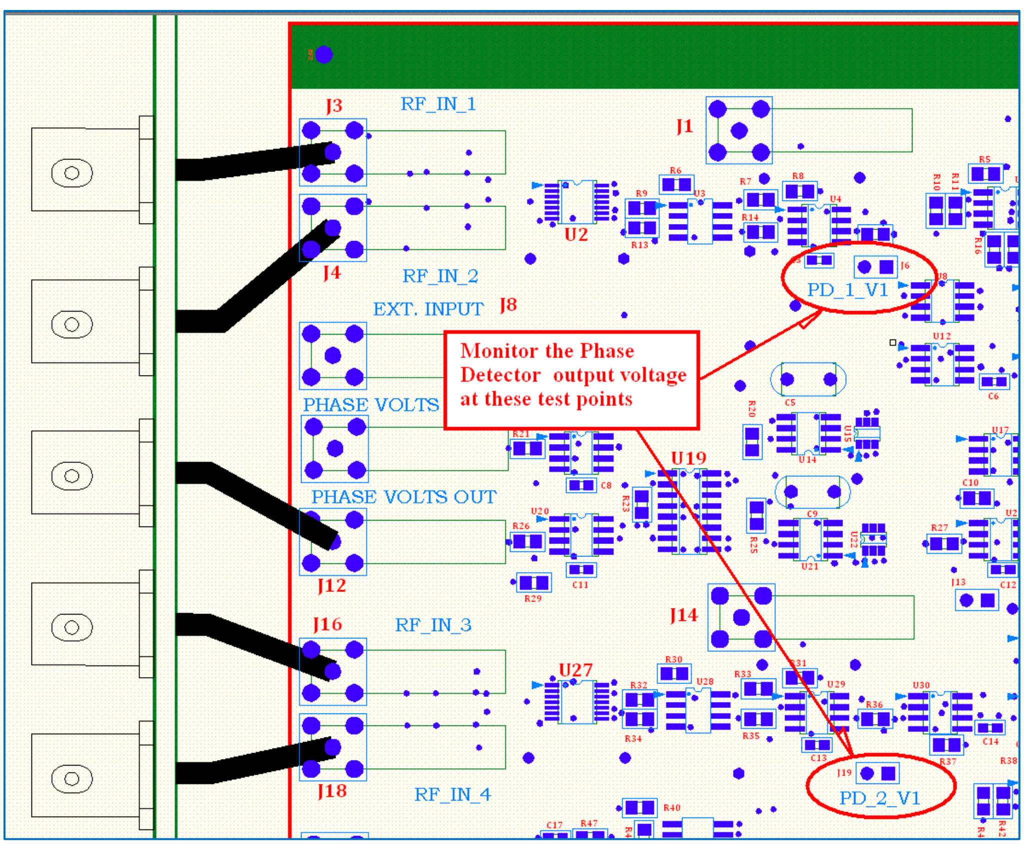


8. Connect the USB cable between the Dual Phase Detector Module and the PC, power the module and start the PC test interface program.

9. Press the “Open PD2 Checkout” button. You should see a dialog box similar to the one below.



10. The Phase Detector 1 and Phase Detector 2 output voltages will be measured at the test points indicated below.



Phase Detector Operational Check

11. Set Channel 2 of the signal generator to a frequency of 50.0001 MHz (50 MHz plus 100 Hz)., Monitor the phase detector output voltages with a scope. Record the following information.

Triangle Wave Volts peak (positive and negative)			
Phase Detector 1	=	_______________	+Vp (Nominal = +/- 8.6)
	=	_______________	-Vp
Phase Detector 2	=	_______________	+Vp
	=	_______________	-Vp

12. In the PD Offsets group select "Set to Setting" and select PD 1 or PD 2 and the "Setting" according to the table below and measure the positive peak voltage of the triangle wave for the selected phase detector output.

Selected PD	Setting	+Vpeak
PD 1	4095	
	0	
	2048	
PD 2	4095	
	0	
	2048	

Note: Leave the phase detectors with an offset setting of 2048 (no offset).

Test Summing Amp and Multiplying DACs

13. In the PD Test Dialog, under "Select Summing Amp Inputs", click the check box for "Sum PD 1". Under "MULT DACs", set the "Step Size" to 200 (DAC Setting should be 8192). Then click "Step MULT DACs" button ***3 times*** and observe the Summing Amp Output on the scope.

____ Did the inverse of the PD output appear at the summing amp output?

Select "Step Dn" for the MULT DACs and step the DACs ***6 times***.

____ Did the signal change polarity at the summing amp output?

Test the Hold Function

14. While observing the triangle wave at the Summing Amp Output and "Sum PD 1 checkbox selected, repeatedly click the "HOLD 1" button in the "Digital Outputs" group.

____ Did the signal change from being triangle to DC when Hold was pressed and back when released?

15. Under "Select Summing Amp Inputs" uncheck "Sum PD 1" and check "Sum PD 2".

____ Did the signal at the summing amp output disappear and then reappear?

16. While observing the triangle wave at the Summing Amp Output and "Sum PD 2 checkbox selected, repeatedly click the "HOLD 2" button in the "Digital Outputs" group.

____ Did the signal change triangle to DC when Hold was pressed and back when released?

Test the FPGA DAC into Summing Amp

17. Under "Select Summing Amp Inputs" uncheck "Sum PD 2" and check "Sum FPGA DAC". In the "FPGA DAC" controls, select "Set to Setting" and set the "DAC Setting" to 16383, and click Step "FPGA DAC".

Summing Amp Voltage Out	=	______________	V (Nominal = 3.7V)

18. In the "FPGA DAC" controls, set the "DAC Setting" to 0, and click Step "FPGA DAC".

Summing Amp Voltage Out	=	______________	V (Nominal = -4.0V)

19. In the "FPGA DAC" controls, set the "DAC Setting" to 8192, and click Step "FPGA DAC".

Summing Amp Voltage Out	=	______________	V (Nominal = 0.0V)

Test LED's, Digital Outputs and Digital Inputs

20. Test the operation of the LED's and Digital Outputs by clicking the associated buttons in the "Digital Outputs" group and measuring the voltage at the Digital Outputs and observing the LED's.

____ Do the Digital Outputs and LED respond properly?

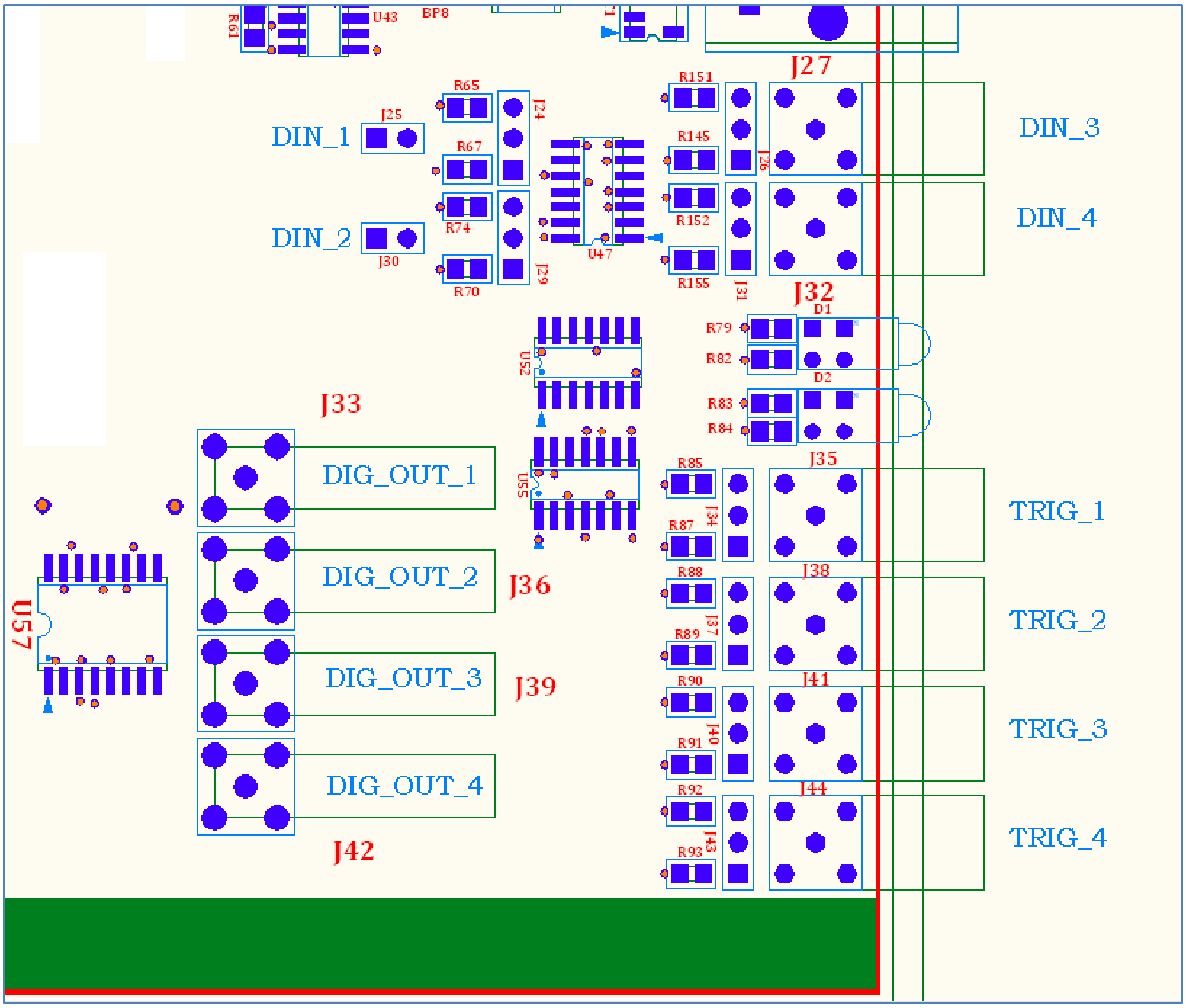
21. In the "Digital Inputs" group, test the operation of each of the listed signals. The diagram below indicates which input is which in the absence of front panel labels.

    The 4 DIN signals and the TRG signals are normally pulled up through 10k ohms causing them to be High by default. You can pull them low by inserting a 50 ohm Lemo terminator. In the case of DIN_1 and DIN_2, you can install a jumper shunt across the pins.

    Signals Beam 1 and Beam 2 should show High with the RF signal generator sinewaves applied to both inputs of the associated phase detector. The Beam 1 and Beam 2 signals will go Low if the RF signal from Channel 1 is removed.

    The HOLD signals and the LED signals can be manipulated with the buttons in the Digital Output group.

_____ Do the Digital Inputs respond properly?

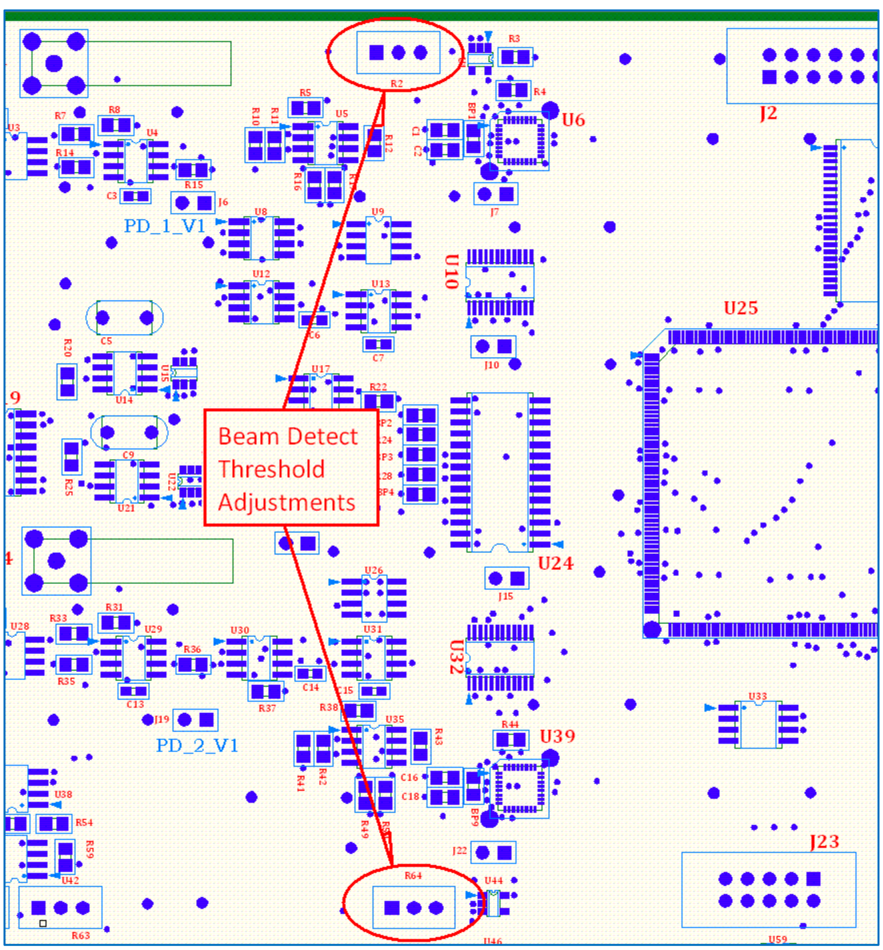


Test and Adjust the Beam Detection Thresholds

22. Adjust the Beam Detection Threshold Adjustments to switch at a RF amplitude difference of 30 dB. The figure below indicates the position of the adjustments (PD 1 is at the top).

    The beam detection works under the assumption that the beam RF comes in the upper RF input of each phase detector (J3 and J16), and that the other input is always present with an amplitude around 0.0 dBm. When the beam input drops 30 dB below this reference input the BEAM_1 or BEAM_2 will go to zero indicating that there is no beam signal.

    Use the variable attenuator in the Channel 1 RF signal to toggle between 29 dB and 30 dB attenuation of this signal. At 29 dB, BEAM_1 and BEAM_2 should indicate 1 in the Digital Inputs group. Turn the pot CW to change the bit from 0 -> 1 and CCW to change the bit from 1 -> 0.



Test and Adjust the Auxilary DAC's

23. The figure below indicates where to measure the outputs of the Auxilary DAC's and where to adjust the gains and offsets for these outputs.

    In the AUX DACs group select "Set to Setting", set "DAC Setting" to 32768 and click "Step DACs 1 and 2". Here, adjust the DAC Offset adjustments for a value out as near 0.000 Volts as possible.

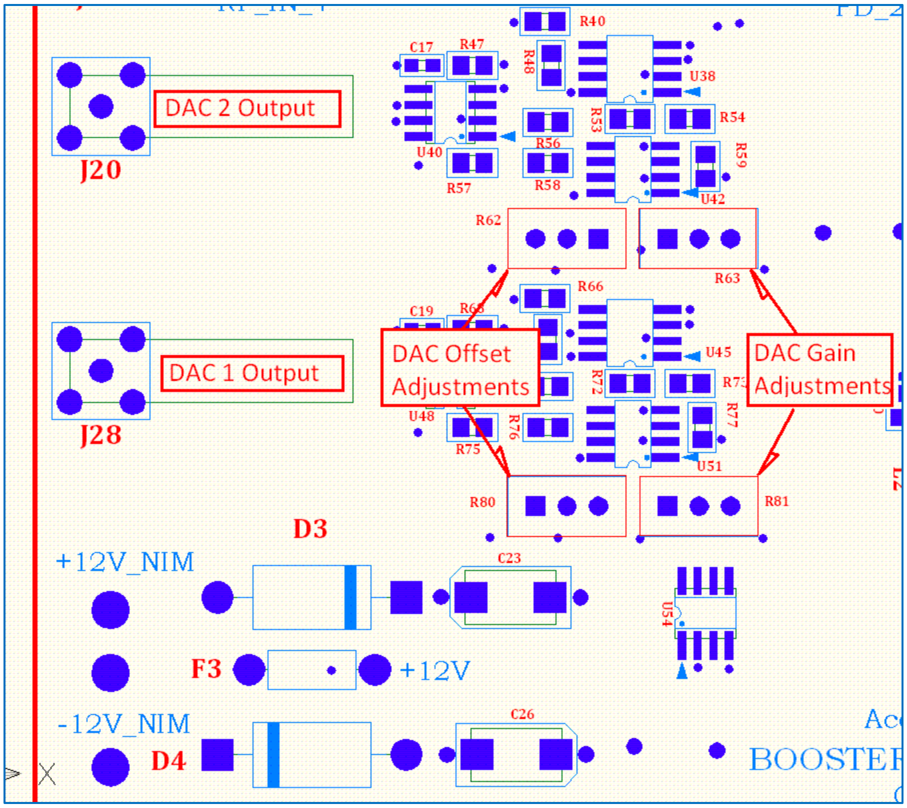
    In the AUX DACs group select "Set to Setting", set "DAC Setting" to 0 and click "Step DACs 1 and 2". Here, adjust the DAC Offset adjustments for a value out as near −10.000 Volts as possible.

    Repeat the two steps above at least one more time. If voltages are within +/- 0.001 V of where they should be that's good.

    In the AUX DACs group select "Set to Setting", set "DAC Setting" to 65535 and click "Step DACs 1 and 2". Here, ensure that the outputs are near +10.000 Volts. Record the results below.

Aux DAC	Setting	Vout
DAC 1	65535	
	32768	
	0	
DAC 2	65535	
	32768	
	0	

Dual Phase Detector 2 Module Checkout and Diagnostics



Test the Calibration of the Phase Detector ADC's

24. On the RF signal generator, set both outputs to 50.000 MHz and synchronize the two channels. In measuring the response of the ADC's you will change the PD Output Volts (the ADC input Voltage) by delaying or phase shifting one of the signal generator channels. Using this method we will record the ADC digital output word for the range of voltages between +9V and –9V (approximately).

    The PD Output voltages should each be examined with a scope to ensure that the voltages are not oscillating, and are actually DC signals. After this the two voltages should be measured with a DVM.

    You will record the PD Output Volts in the "ADC 1 and ADC 2" group, in the "Volts In 1" and "Volts In 2" boxes. The ADC response is displayed in the "ADC 1" and "ADC 2" boxes automatically.
    To record each data point to a file, click the "Record Data" button. That data point will be recorded to the listed in the "Data File:" box and a copy is displayed in the List box to the right of the controls.

Dual Phase Detector 2 Module Checkout and Diagnostics

When the data record is considered complete, click the “Start New File” button to close the current file and open a new one. The file of data should be opened with Excel and plotted to examine the results.

Rename the file indicating the Module Number of the module being tested and file in the test results folder.

Finish by Saving the Test Results

25. Do a “Save As” on this document with a filename indicating the Module Number of the module being tested and file in the test results folder.