Progress on Testing of New Electronics for Phase-Locking Booster to the Main Injector RF

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February 2, 2012

I. Introduction

A new dual phase detector NIM module is under development for use in the Booster LLRF system. The goal for this module is to be able to provide the phase error feedback and control used to perform the Booster acceleration phase lock and the Main Injector phase lock functions. In doing this, this module could eventually replace the following LLRF NIM modules:

1. The Timing Generator, 0331.00-ED-180859
2. The 32 Countdown Module, 0331.00-EC-180846
3. The High Stability EMI Protected Phase Detector
4. The Program Generator, 0331.00-ED-180850
5. The Parabola Zero Box, 0331.00-EC-180858
6. The Fast Phase Detector, 0331.00-ED-180843
7. The Mode Controller, 0331.00-ED-180845

The change is motivated by replacement parts obsolescence and a desire to improve the characteristics of the MI phase lock. Even as sophisticated as the current analog controls are, the transition to MI phase lock puts an oscillation into the beam.

Opportunities for testing the new modules and MI phase lock methods with the rest of the LLRF system and with Booster beam are rare, but some progress has been made. This note will describe the testing done in recent weeks.

II. No Beam Testing

II.1 Description

The MI phase lock is made between the MI RF reference delivered to the Booster LLRF area and the DDS-VCO LLRF frequency source. There is no need for actual beam in the Booster to initially tune up the phase lock processes. Several settings can be adjusted and other configuration details can be determined without having to have beam.

II.2 Setup

Below is a list of details on the system configuration for the No Beam testing.

1. The accelerator controls Time Line Generator (TLG) needs to be setup with Booster reset events associated with a cogged cycle, one where MI phase lock is expected to be executed at the end of the cycle.
2. The MI phase lock arming trigger for the test stand, B:PEFFTR, needs to be set to trigger on the MI phase lock cycle that the TLG is going to produce.
3. The Normal / Test switch needs to have its trigger inputs setup to use the test module signal on the MI phase lock cycle. Trigger B:PHDSW selects the test module signal and B:TRIG6 selects the normal phase error signal.
4. The phase error feedback signal needs to be switch from the normal signal directly out of the Program Generator and the Summing Box to be the phase error selected by the Normal / Test switch. This is done by moving the phase error cable to the DDS-VCO from the Normal spigot to the Test spigot at the test stand.
5. Since there is no beam the Beam Gate input to the DDS-VCO will not be active and will disable the phase error feedback to the LLRF reference. The Beam Gate signal is routed to the DDS-VCO module through the feed through panel "B" in rack LLRF4 on spigot number 6 (4-B-6). Adjacent to this feed through on spigot number 5 (4-B-5) is another gating signal, Accel. Phase Lock Gate. This second gate is generated whether there is beam or not. To eliminate the need for the Beam Gate we can tie the Beam Gate input of the DDS-VCO to the Tee connection at spigot 5.
6. A different frequency curve needs to be used in the DDS-VCO LLRF source. The modified curve needs to be flat, an unchanging frequency value for at least 3 ms before the end of the curve. This value should be 1000 Hz down from the expected MI RF frequency.
7. The DDS-VCO frequency threshold value, B:VPLFRQ, at which the module puts out the MI phase lock trigger, VXPLTRG, needs to be set at this frequency that is 1000 Hz below the MI RF frequency.
8. The Dual Phase Detector module also requires a valid Beam Gate signal under normal conditions. For the No Beam testing, the terminator installed in the T1 trigger input on the front of the module can be removed allowing the input to be pulled high. This is a "Run_MIPL_Always" signal that bypasses the requirement for a Beam Gate Signal.
9. The Dual Phase Detector module also has an internal parameter that can be set to control the output of the module before the occurrence of the MI phase lock trigger, when there is no beam. This is parameter #9, the NO BEAM OFFSET.

To end the testing and return to Normal operation the following actions need to be taken.

1. The phase error feedback cable to the DDS-VCO should be switched from the Test spigot, at the test stand, to the Normal spigot connection.
2. The normal frequency curve needs to be reloaded into the DDS-VCO LLRF source.
3. The MI phase lock frequency threshold value, B:VPLFRQ needs to be restored to its previous value.

4. The Beam Gate input to the DDS-VCO needs to be returned to the Beam Gate signal at feed through spigot number 6 (4-B-6).

III. Results from tests made June 24 to February 1, 2012

January 24

The normal phase error signal from the Program Generator and Summing Box had been left unconnected from the test stand Normal / Test switch module because the input protection diodes on the analog switches would pull the input signals down if the module was not powered. We could leave the module powered, but it was just safer to disconnect the phase error signal when we were not expecting to do testing.

On this day, the module was powered and we attempted to connect the normal phase error signal to the Normal switch input. For some reason this resulted in a failure to accelerate beam and sparking of the RF cavities.

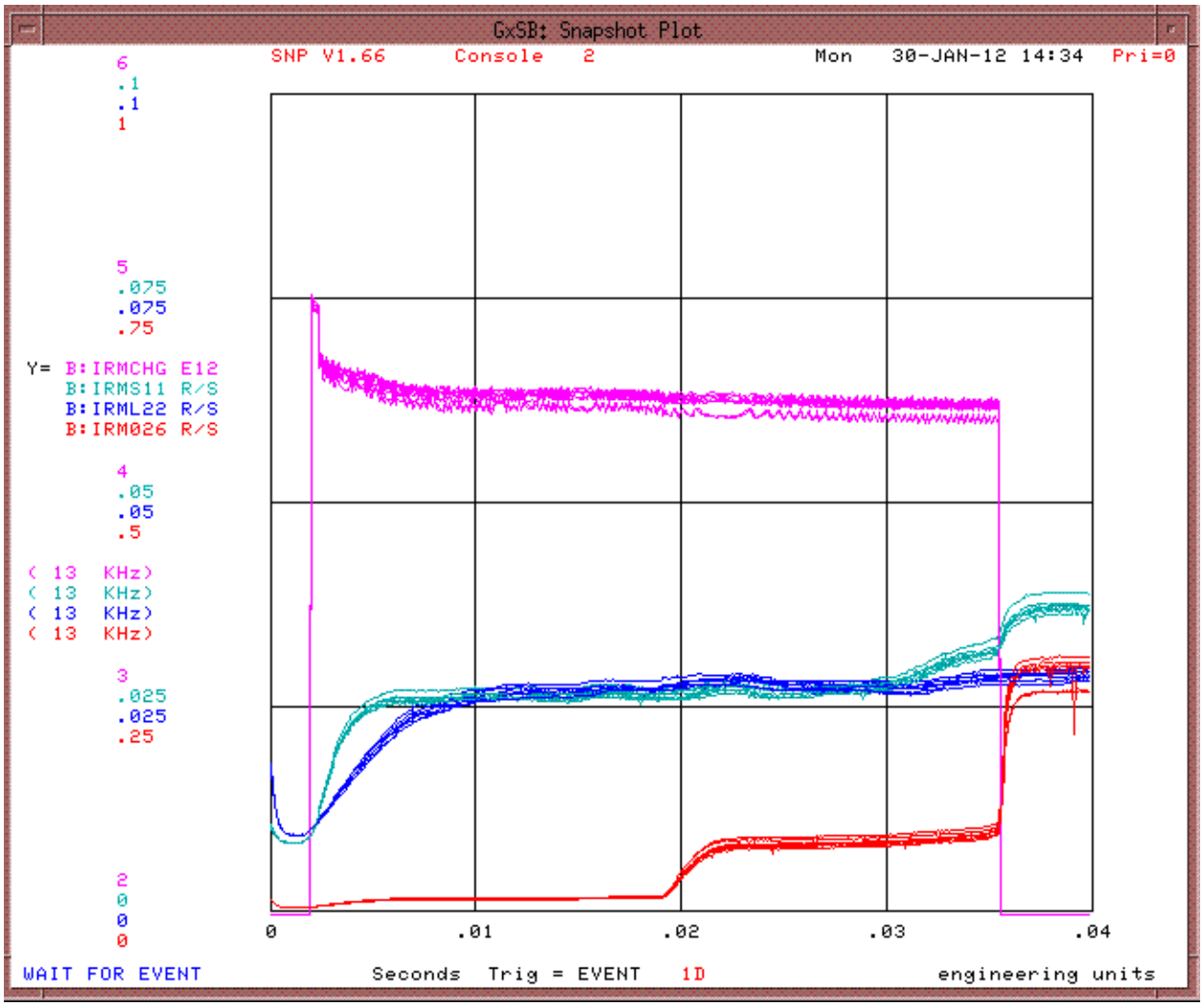
This issue appears to have been resolved by removing the 500 ohm input terminating resistors in the Normal / Test switch module. We successfully connected the phase error signal to the switch input after lunch, and left it in this configuration.

January 25

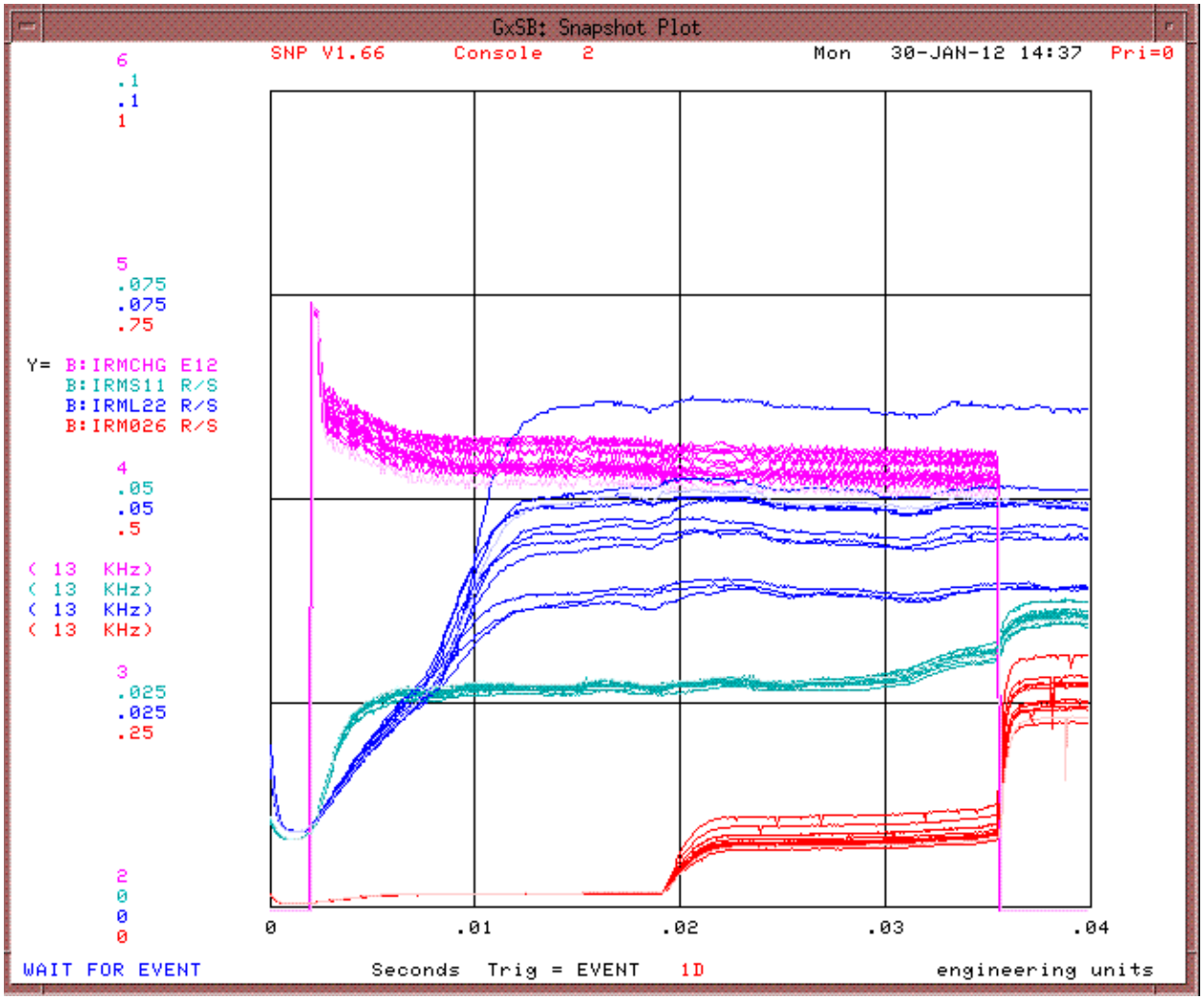
The next step was to use the normal phase error feedback through the Normal / Test switch to control the LLRF system. This had been done successfully in past efforts. However, we failed to acceleration beam in the Booster beyond the 5 ms mark in this configuration. Several investigation were made to determine if and how the phase error signal was made different in this configuration. Bill Pellico provided a difference amplifier module to be used to compare the input and output of the switch more closely. There was a small deviation that occurred during the highest dF/dt portion of the curve. Bill adjusted the start time of the LLRF Frequency curve and the deviation went away and beam accelerated satisfactorily using the normal phase error feedback through the switch.

January 30

An attempt was made to use the phase error feedback from one of the new modules to control the Booster acceleration for a non-Main Injector phase lock cycle ($1D s). The use of the new phase detector was unsatisfactory. No tuning was attempted since this configuration had worked successfully in the past and there was a strong hope that a solution would be found that precluded significant changes to other LLRF system control parameters. Further testing in this configuration was postponed. Plots showing the system efficiency and losses are given below for the normal system and the test system on this day.



Plots for the LLRF system using the normal phase error signal through the Normal / Test switch.



Plots for the LLRF system using the test phase error signal through the Normal / Test switch.

It could be that some small amount of tuning could allow the test configuration to perform satisfactorily, but this was not attempted on this day.

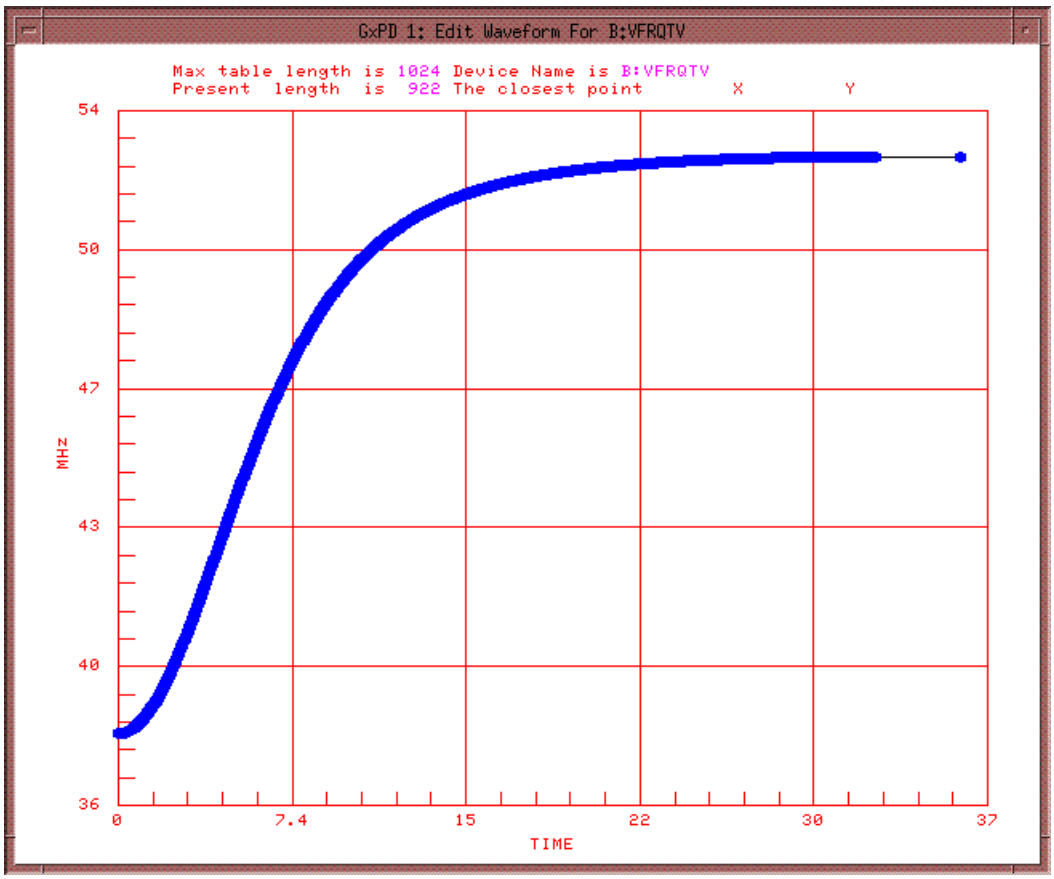
February 1

This week the Booster and Main Injector were shutdown for installation and maintenance and it was a good opportunity to perform the No Beam phase lock tests. The system was eventually setup as described previously for the No Beam testing. After this setup and some tuning of the gain, offset and phase error reference curve parameters, the phase lock was very much like that seen on the bench, in the lab. Below is a list of observation made during the test.

1. The actual gain of the DDS-VCO phase error feedback was approximately twice as high as expected and hence the final gain settings were smaller than those used on the bench.
2. The normal frequency curve loaded into the DDS-VCO LLRF source uses all 1024 time value pairs allowed by the modules configuration. The curve was modified to flatten the curve to a constant 52.809 MHz between 32.2 ms and 35.8 ms using all of the original time value pairs

established by the original frequency curve. Small glitches in the output frequency of the DDS-VCO module were seen by the phase detector and it was strongly suspected to be caused by numerical or other signal issues within the DDS-VCO module.

The frequency glitches were eliminated by removing most of the time value pairs from the curve between the 32.2 ms pair and the 35.8 ms pair. A plot of the resulting frequency curve is shown below.



The frequency curve used for the No Beam MI phase lock testing on February 1, 2012

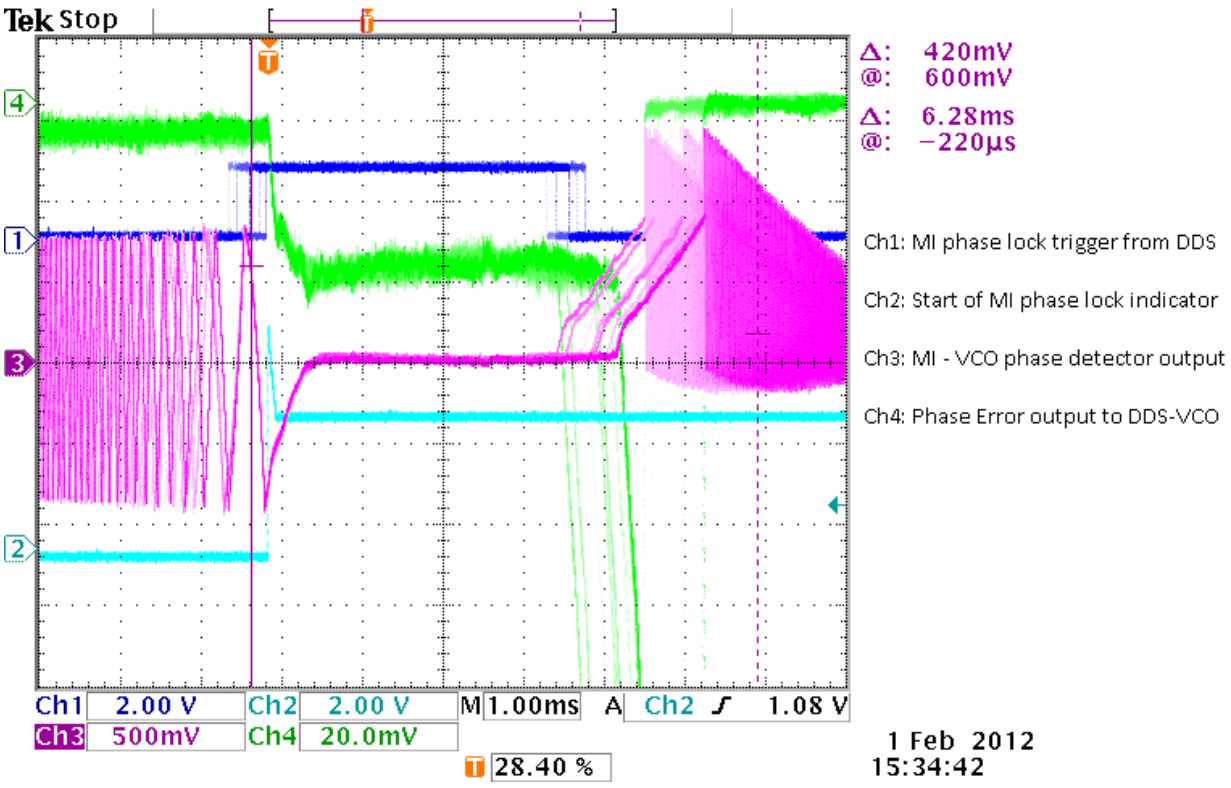
3. It was noted that we had barely, if at all, reach the frequency difference of 1 kHz between the DDS-VCO output and the MI RF signal before MI phase lock cycle started. This is attributed to noise on the phase error feedback summing with the frequency curve and triggering the MI phase lock trigger before reaching the 52.809 MHz segment of the frequency curve.

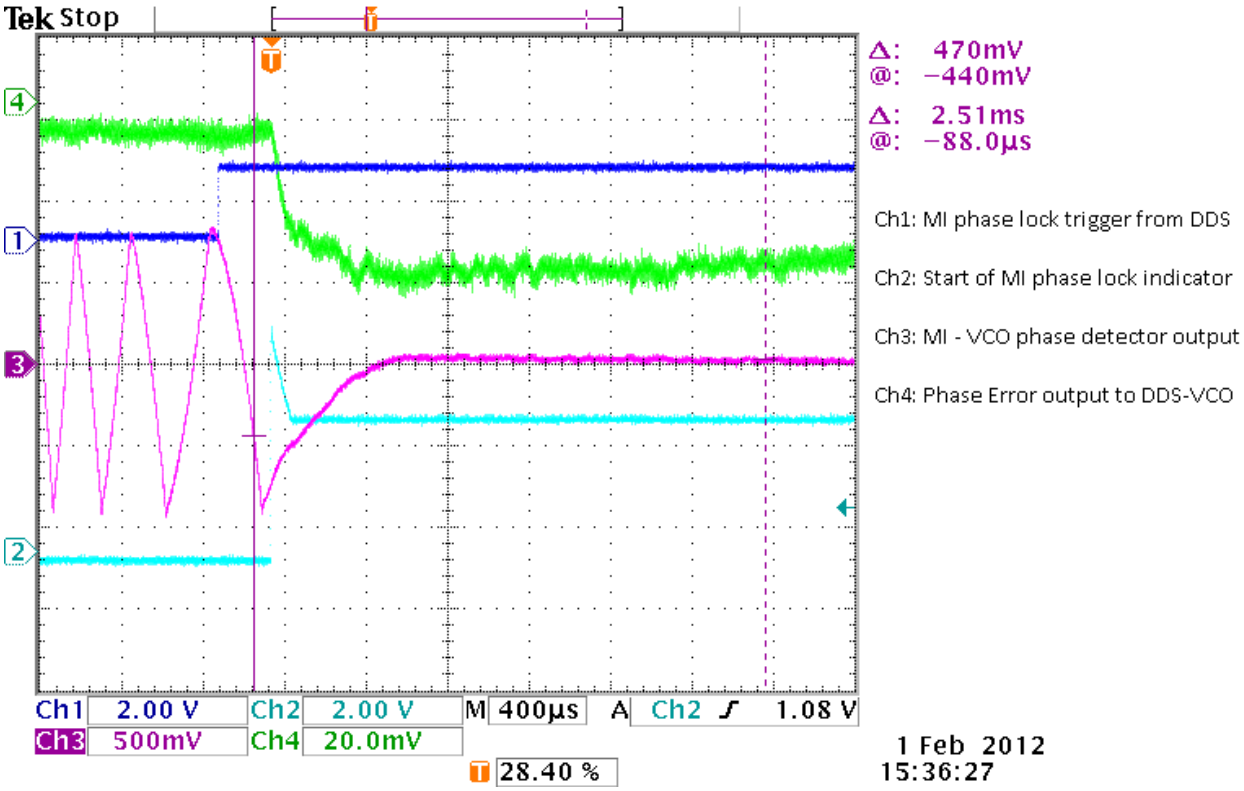
   A remedy of this issue may be to delay the start of the MI phase lock cycle a small amount of time, say 0.5 ms, after the occurrence of the MI phase lock trigger to allow the DDS-VCO output

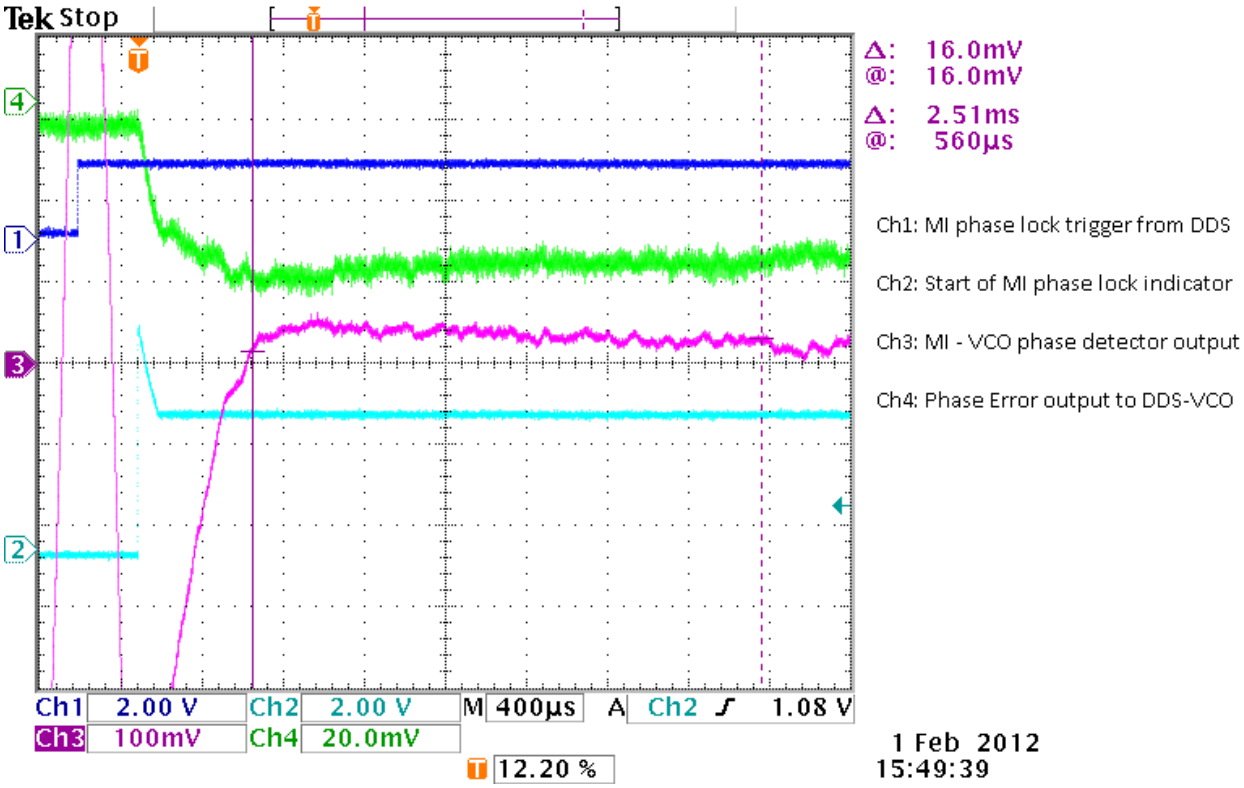
frequency to advance further into the flat portion of the frequency curve. This trigger delay has since been added to the FPGA logic for use in the next round of tests.

4. As noted previously, the gain of the DDS-VCO between the change in phase error voltage in and the change in the frequency out was higher than expected. The phase error voltage changed only 40 mV to accomplish the 1 kHz frequency change on the output of the DDS-VCO. In the computation of the MI phase lock phase error feedback a trade off exists between the bit resolution of the digital values and the full scale range of the numbers. I believe that we could probably increase the bit resolution for this case.

Below are some scope plots of the signals observed during the February 1 No Beam MI phase lock tests.




Tek Stop
Δ: 470mV
@: −440mV
Δ: 2.51ms
@: −88.0µs
Ch1: MI phase lock trigger from DDS
Ch2: Start of MI phase lock indicator
Ch3: MI - VCO phase detector output
Ch4: Phase Error output to DDS-VCO
Ch1 2.00 V
Ch2 2.00 V
M 400µs
A Ch2 1.08 V
Ch3 500mV
Ch4 20.0mV
28.40 %
1 Feb 2012
15:36:27


Tek Stop
Δ: 16.0mV
@: 16.0mV
Δ: 2.51ms
@: 560µs
Ch1: MI phase lock trigger from DDS
Ch2: Start of MI phase lock indicator
Ch3: MI - VCO phase detector output
Ch4: Phase Error output to DDS-VCO
Ch1 2.00 V
Ch2 2.00 V
M 400µs
A Ch2 1.08 V
Ch3 100mV
Ch4 20.0mV
12.20 %
1 Feb 2012
15:49:39