
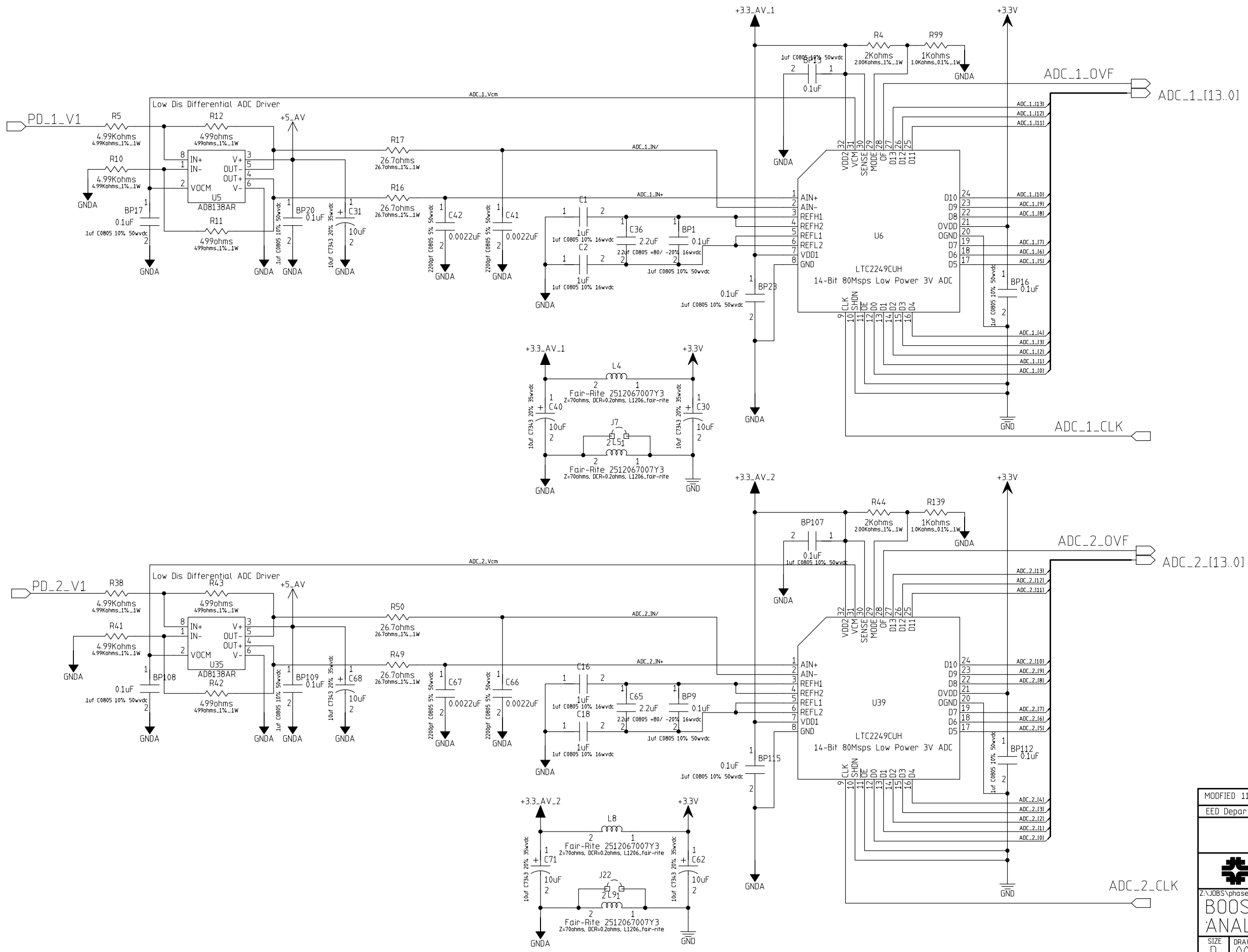

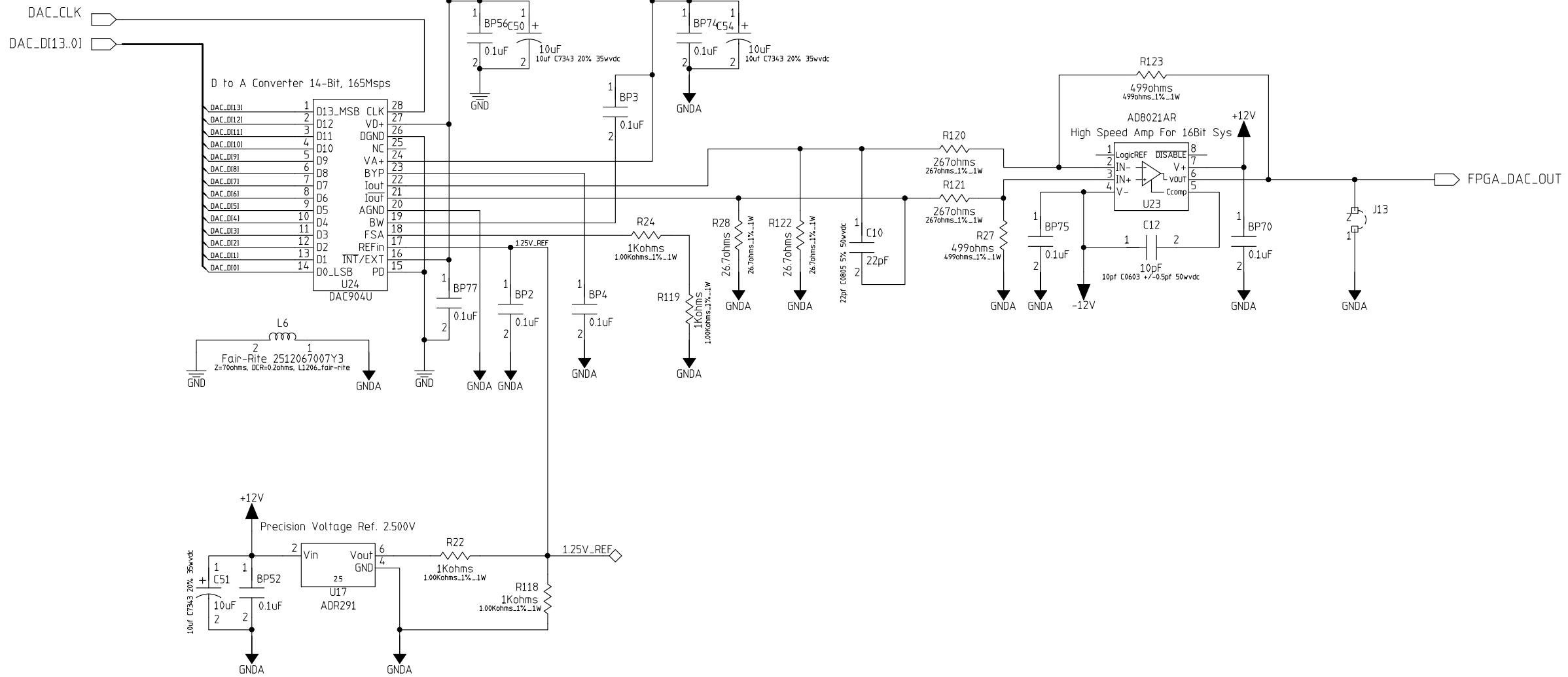



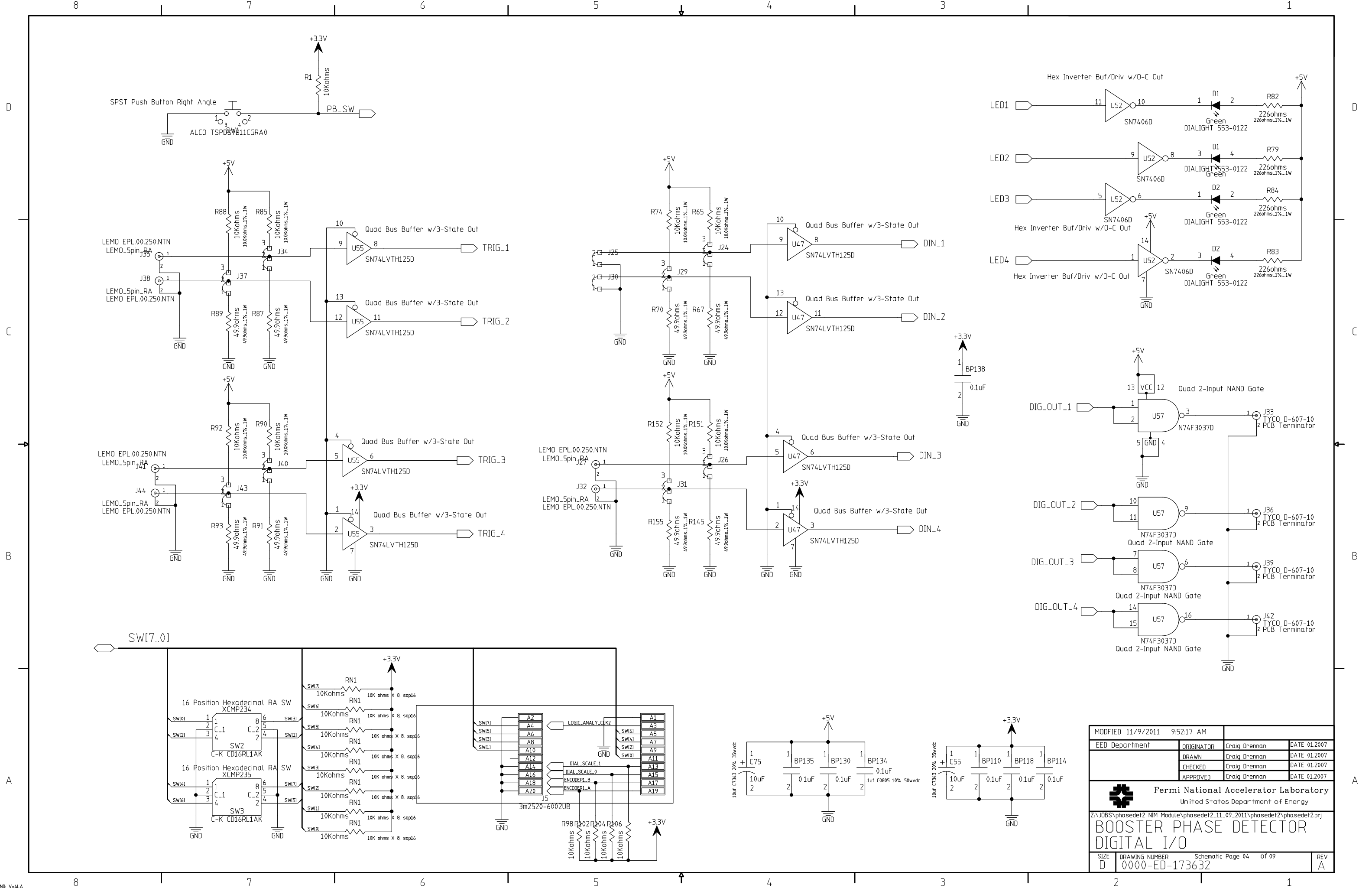
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PHASE DETECTOR POWER INPUT SECTION			
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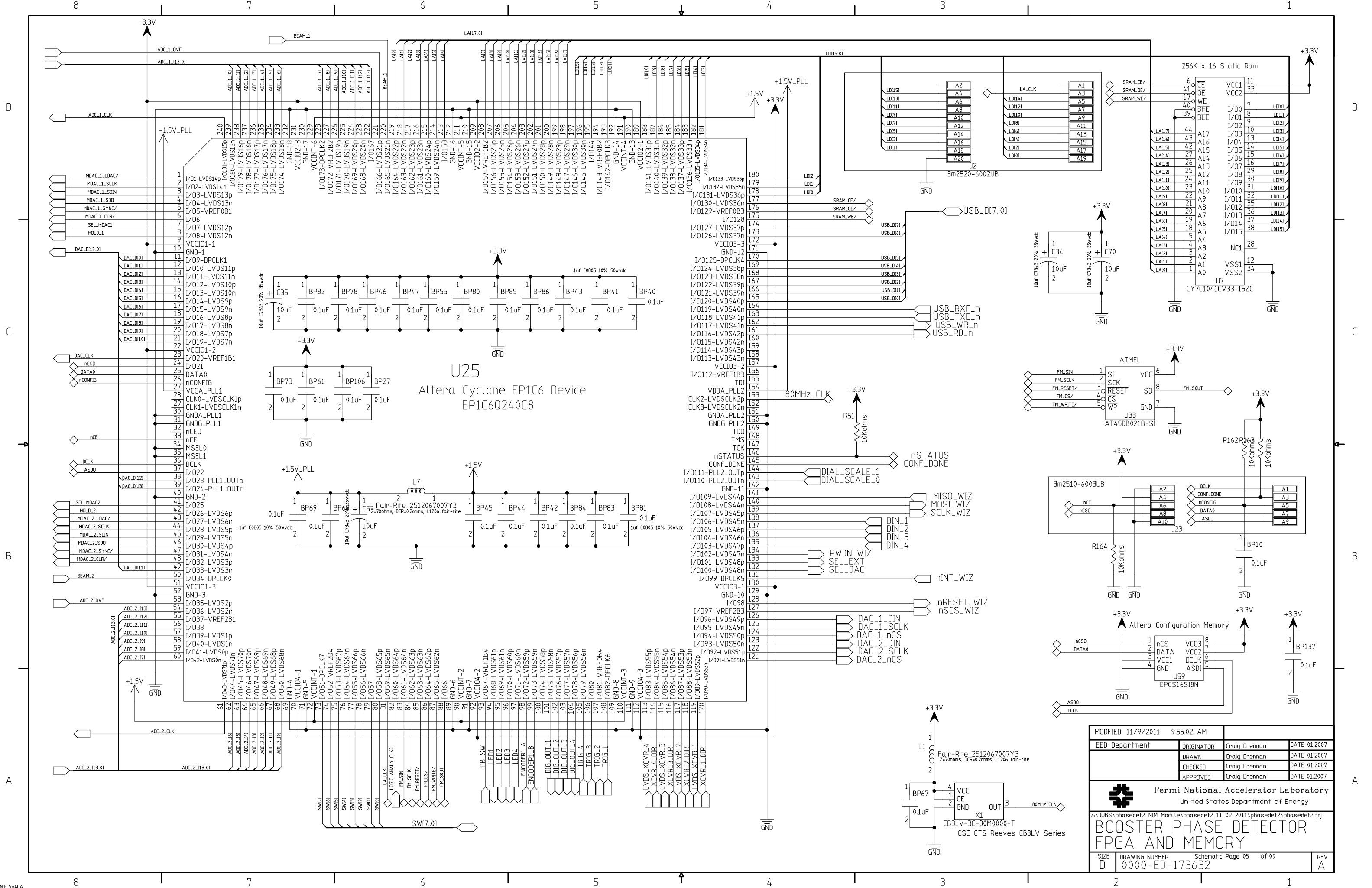
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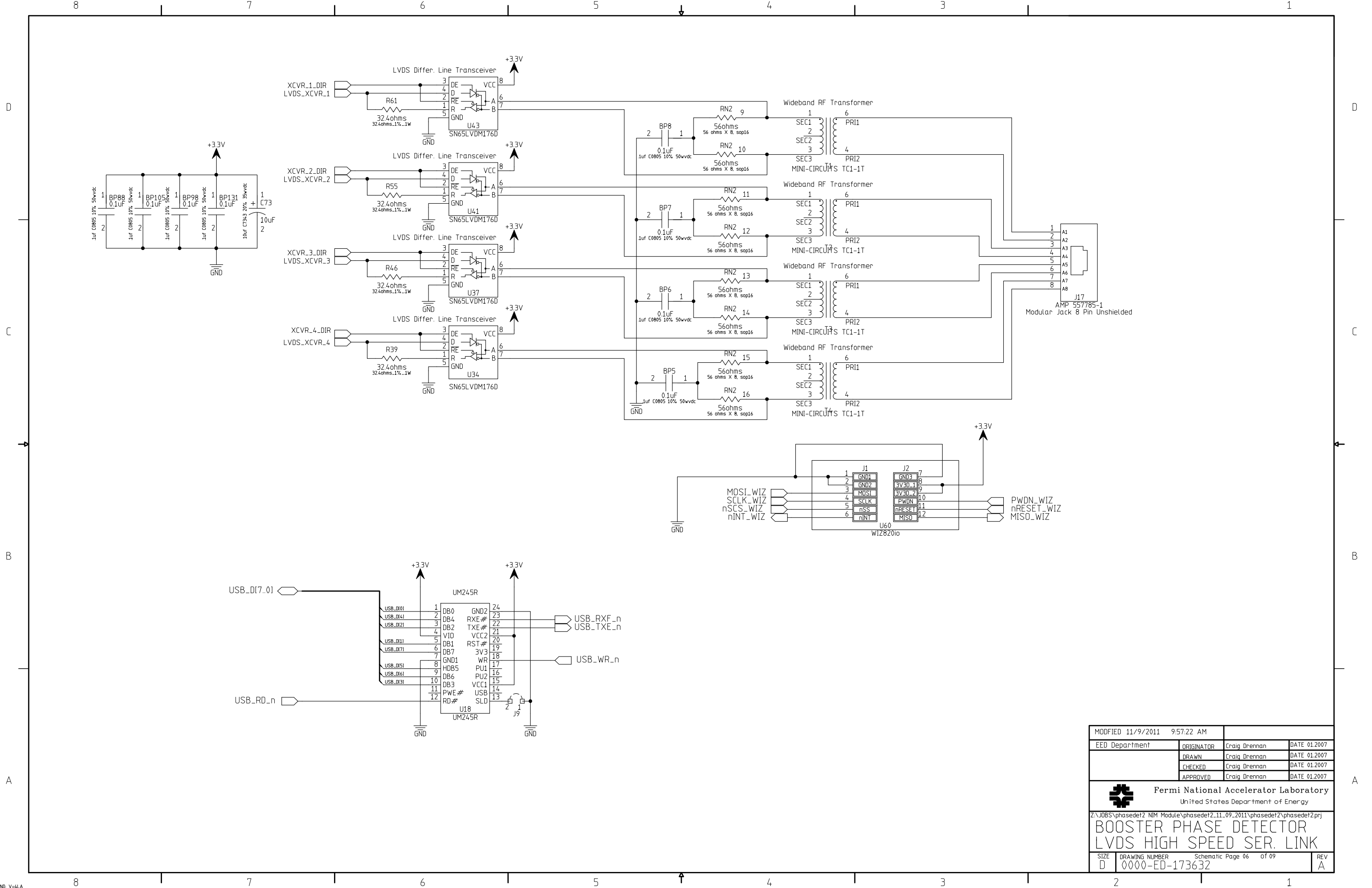
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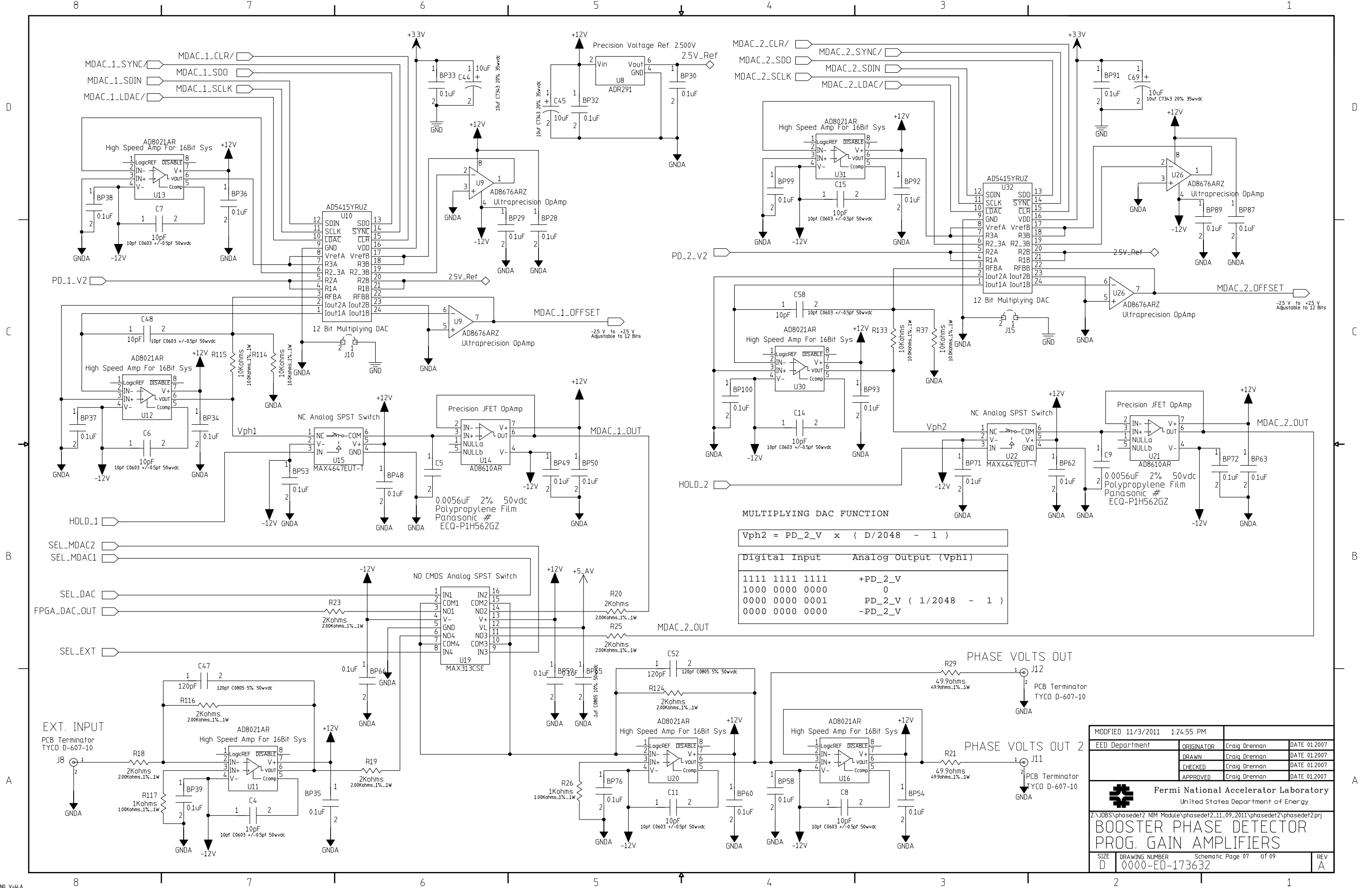
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BOOSTER PHASE DETECTOR DIGITAL I/O		
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Fermi National Accelerator Laboratory United States Department of Energy Z:\JOBS\phasedef2 NIM Module\phasedef2.11.09.2011\phasedef2\phasedef2.prj BOOSTER PHASE DETECTOR FPGA AND MEMORY		
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MULTIPLYING DAC FUNCTION

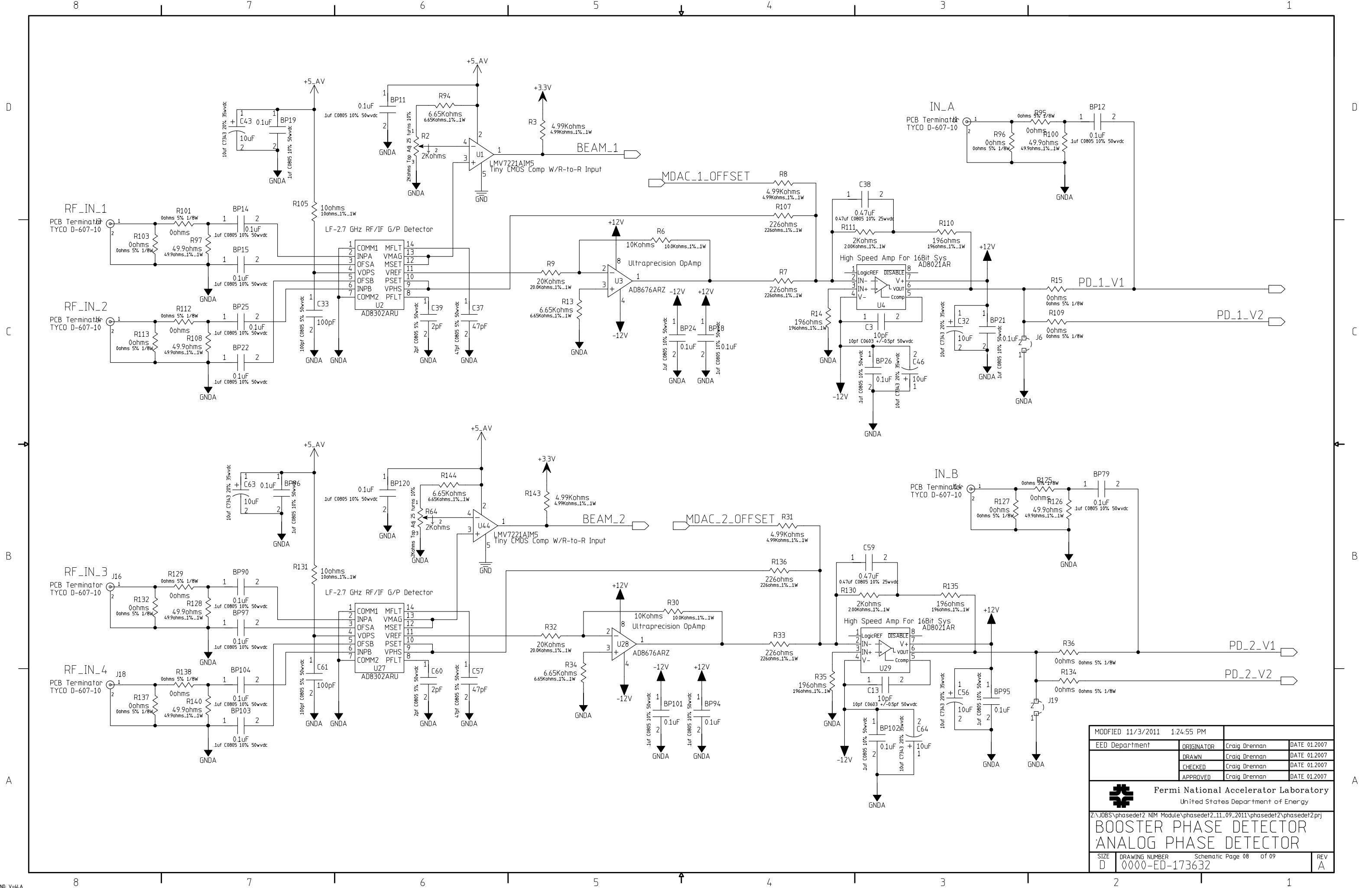
$$V_{ph2} = PD_2_V \times (D/2048 - 1)$$

Digital Input	Analog Output (Vph1)
1111 1111 1111	+PD_2_V
1000 0000 0000	0
0000 0000 0001	PD_2_V (1/2048 - 1)
0000 0000 0000	-PD_2_V


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BOOSTER PHASE DETECTOR
PROG. GAIN AMPLIFIERS

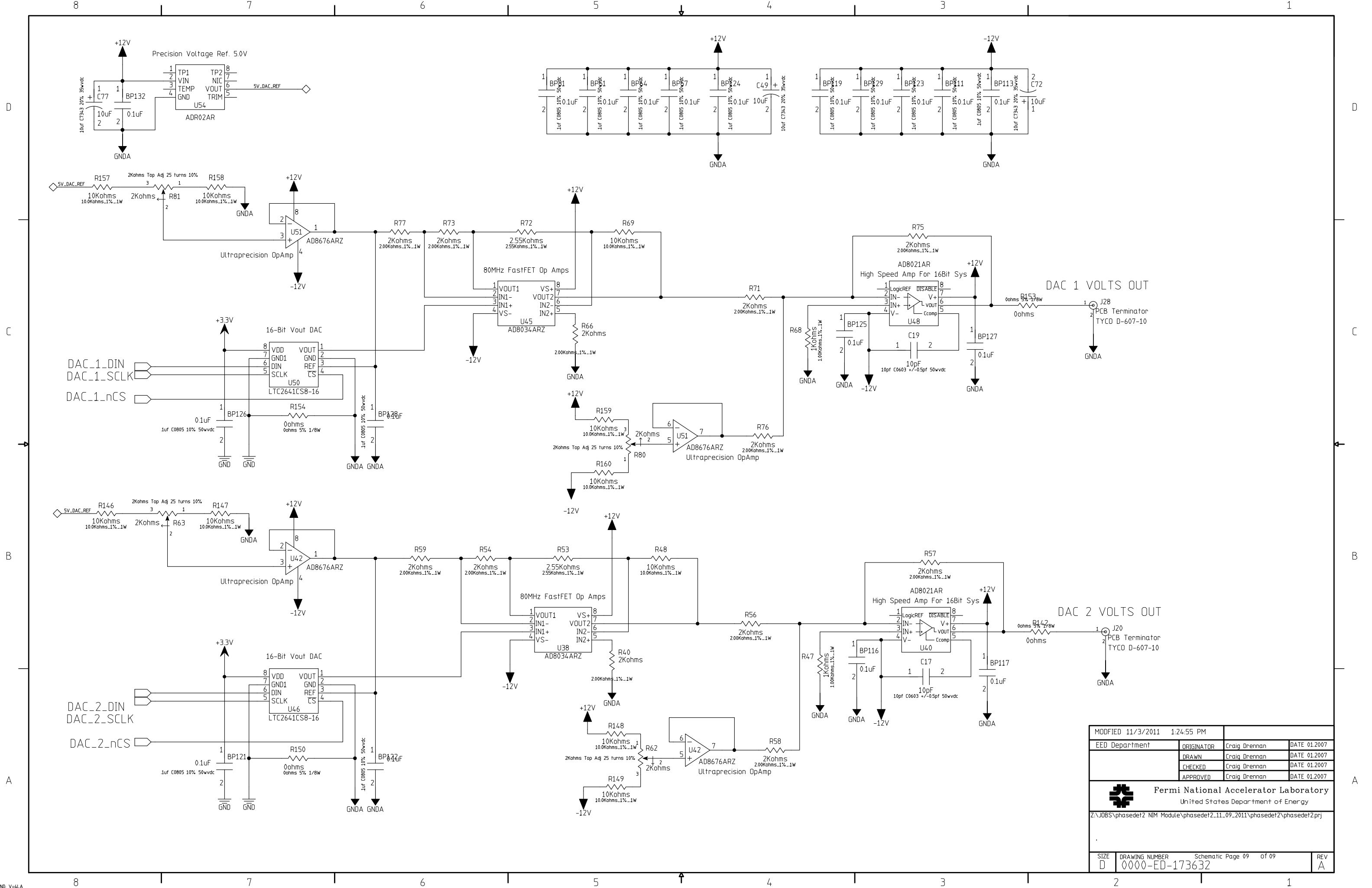
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BOOSTER PHASE DETECTOR
ANALOG PHASE DETECTOR

SIZE	DRAWING NUMBER	Schematic Page 08 of 09	REV
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