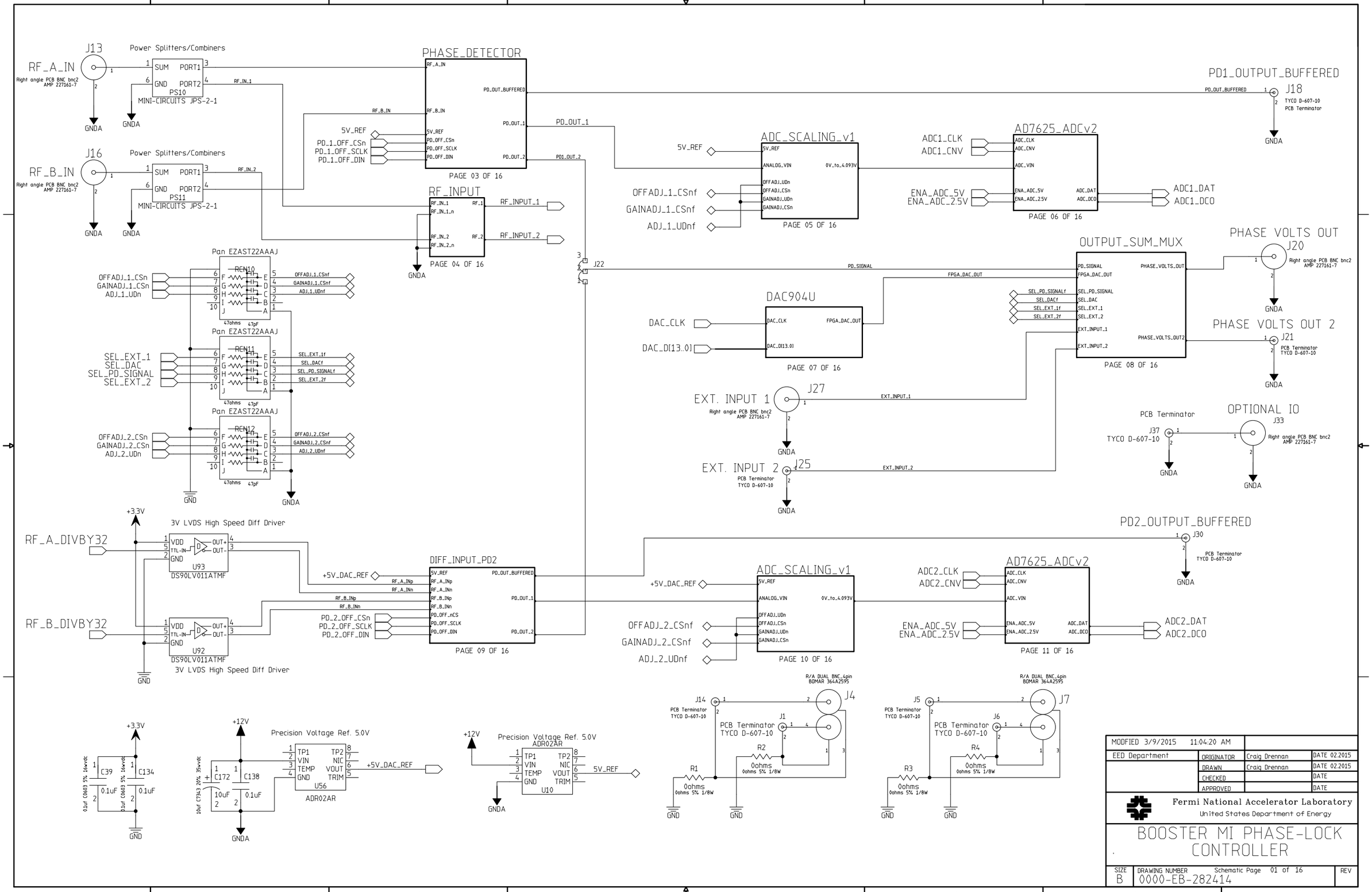
RF_A_IN
J13
Right angle PCB BNC bnc2 AMP 227161-7
Power Splitters/Combiners
SUM PORT1
GND PORT2
PS10
MINI-CIRCUITS JPS-2-1
RF_IN_1
GNDA
RF_B_IN
J16
PS11
RF_IN_2
PHASE_DETECTOR
RF_A_IN
RF_B_IN
5V_REF
PD_1_OFF_CSn
PD_1_OFF_SCLK
PD_1_OFF_DIN
PD_OUT_BUFFERED
PD_OUT_1
PD_OUT_2
PD1_OUT_2
PAGE 03 OF 16
RF_INPUT
RF_IN_1
RF_IN_1_n
RF_IN_2
RF_IN_2_n
RF_1
RF_2
RF_INPUT_1
RF_INPUT_2
PAGE 04 OF 16
PD1_OUTPUT_BUFFERED
J18
TYCO D-607-10
PCB Terminator
ADC_SCALING_v1
ANALOG_VIN
0V_to_4.093V
OFFADJ_UDn
OFFADJ_CSn
GAINADJ_UDn
GAINADJ_CSn
OFFADJ_1_CSnf
GAINADJ_1_CSnf
ADJ_1_UDnf
PAGE 05 OF 16
AD7625_ADCv2
ADC_CLK
ADC_CNV
ADC_VIN
ENA_ADC_5V
ENA_ADC_2.5V
ADC_DAT
ADC_DCO
ADC1_CLK
ADC1_CNV
ADC1_DAT
ADC1_DCO
PAGE 06 OF 16
Pan EZAST22AAJ
RCN10
RCN11
RCN12
47ohms
47pF
OFFADJ_1_CSn
GAINADJ_1_CSn
ADJ_1_UDn
SEL_EXT_1
SEL_DAC
SEL_PD_SIGNAL
SEL_EXT_2
OFFADJ_2_CSn
GAINADJ_2_CSn
ADJ_2_UDn
GND
J22
PD_SIGNAL
FPGA_DAC_OUT
DAC904U
DAC_CLK
DAC_D[13..0]
PAGE 07 OF 16
OUTPUT_SUM_MUX
PHASE_VOLTS_OUT
PHASE_VOLTS_OUT2
SEL_PD_SIGNALf
SEL_DACf
SEL_EXT_1f
SEL_EXT_2f
EXT_INPUT_1
EXT_INPUT_2
PAGE 08 OF 16
PHASE VOLTS OUT
J20
PHASE VOLTS OUT 2
J21
EXT. INPUT 1
J27
EXT. INPUT 2
J25
OPTIONAL IO
J33
J37
PD2_OUTPUT_BUFFERED
J30
+3.3V
3V LVDS High Speed Diff Driver
RF_A_DIVBY32
RF_B_DIVBY32
VDD
TTL-IN
GND
OUT+
OUT-
U93
U92
DS90LV011ATMF
DIFF_INPUT_PD2
+5V_DAC_REF
RF_A_INp
RF_A_INn
RF_B_INp
RF_B_INn
PD_OFF_nCS
PD_2_OFF_CSn
PD_2_OFF_SCLK
PD_2_OFF_DIN
PAGE 09 OF 16
ADC_SCALING_v1
OFFADJ_2_CSnf
GAINADJ_2_CSnf
ADJ_2_UDnf
PAGE 10 OF 16
AD7625_ADCv2
ADC2_CLK
ADC2_CNV
ADC2_DAT
ADC2_DCO
PAGE 11 OF 16
R/A DUAL BNC_4pin BOMAR 364A2595
J14
J1
J4
J5
J6
J7
R1
R2
R3
R4
0ohms
0ohms 5% 1/8W
C39
C134
C172
C138
0.1uF
10uF
+12V
Precision Voltage Ref. 5.0V
TP1
VIN
TEMP
GND
TP2
NIC
VOUT
TRIM
U56
ADR02AR
U10
5V_REF
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EED Department
ORIGINATOR Craig Drennan DATE 02.2015
DRAWN Craig Drennan DATE 02.2015
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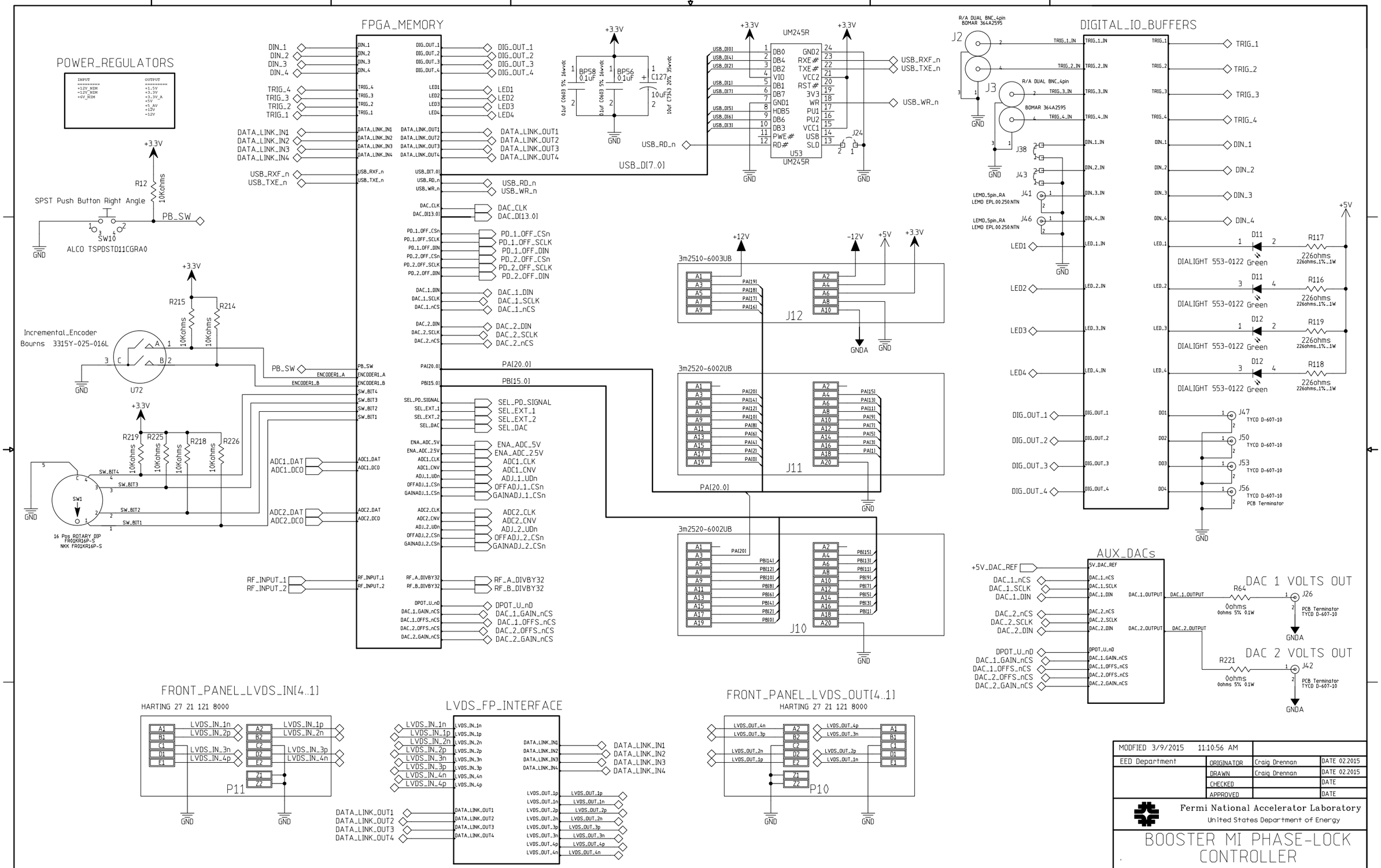
Fermi National Accelerator Laboratory
United States Department of Energy
BOOSTER MI PHASE-LOCK CONTROLLER
SIZE B
DRAWING NUMBER 0000-EB-282414
Schematic Page 01 of 16
REV
H=8ND; V=4LA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FPGA_MEMORY
DIGITAL_IO_BUFFERS
AUX_DACs
FRONT_PANEL_LVDS_IN[4..1]
LVDS_FP_INTERFACE
FRONT_PANEL_LVDS_OUT[4..1]
SPST Push Button Right Angle
ALCO TSPDSTD11CGRA0
Incremental_Encoder
Bourns 3315Y-025-016L
16 Pos ROTARY DIP
NKK FR01KR16P-S
UM245R
3m2510-6003UB
3m2520-6002UB
3m2520-6002UB
HARTING 27 21 121 8000
HARTING 27 21 121 8000
DIALIGHT 553-0122 Green
DAC 1 VOLTS OUT
DAC 2 VOLTS OUT
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EED Department
ORIGINATOR Craig Drennan DATE 02.2015
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Fermi National Accelerator Laboratory
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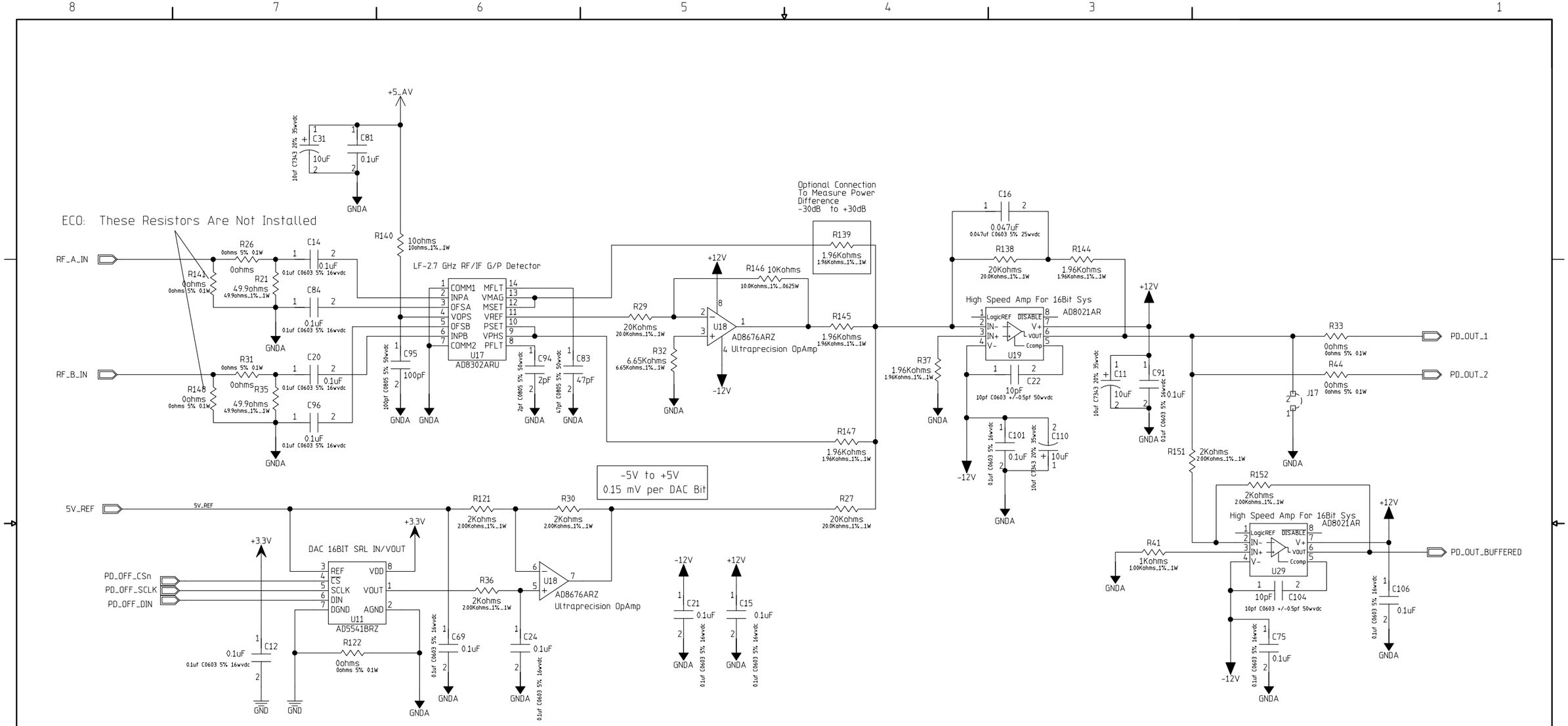
BOOSTER MI PHASE-LOCK CONTROLLER
SIZE B
DRAWING NUMBER 0000-EB-282414
Schematic Page 02 of 16
REV



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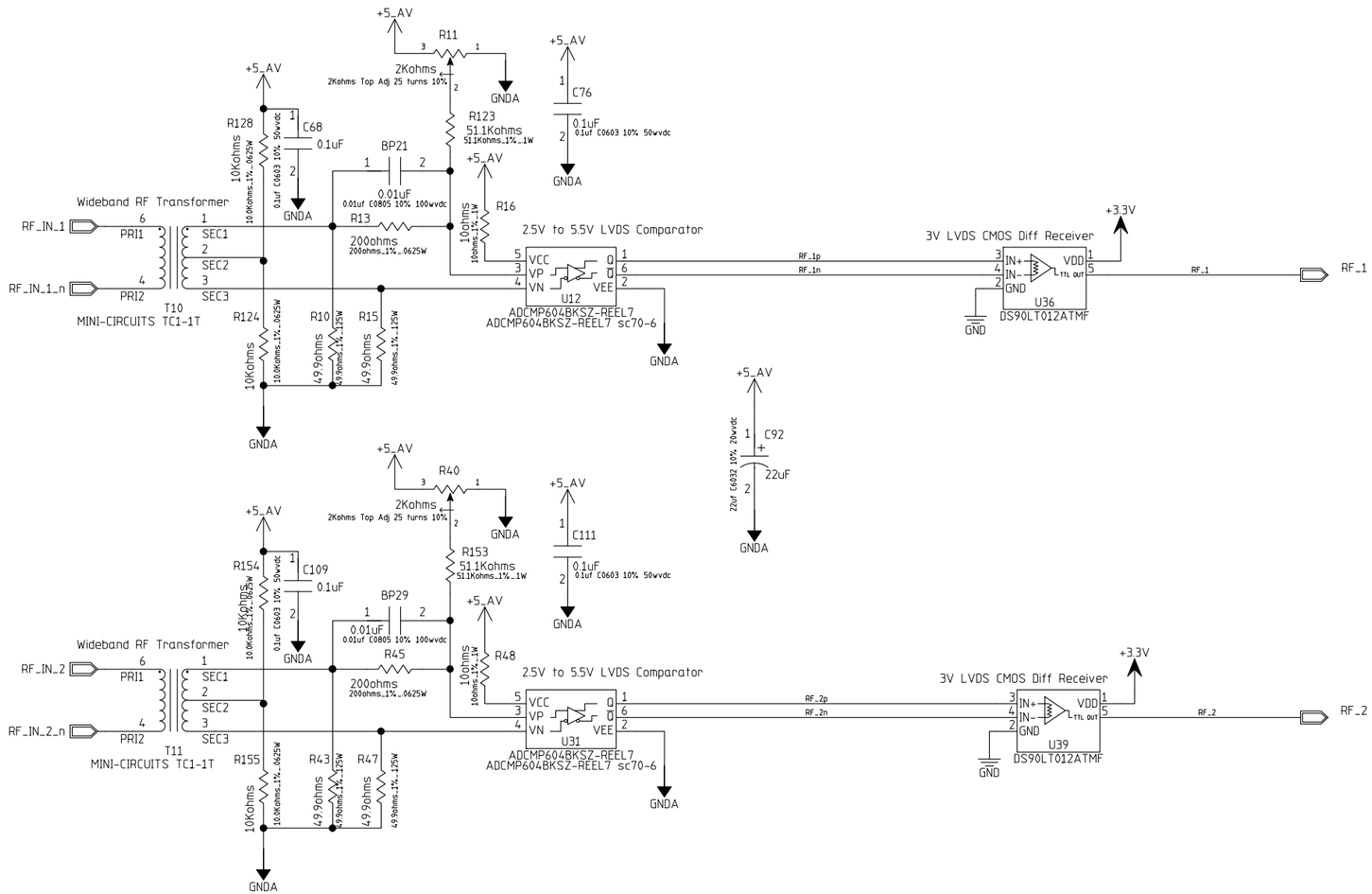
BOOSTER MI PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER		REV
B	0000-EB-282414	Schematic Page 03 of 16	

H=8ND; V=4LA



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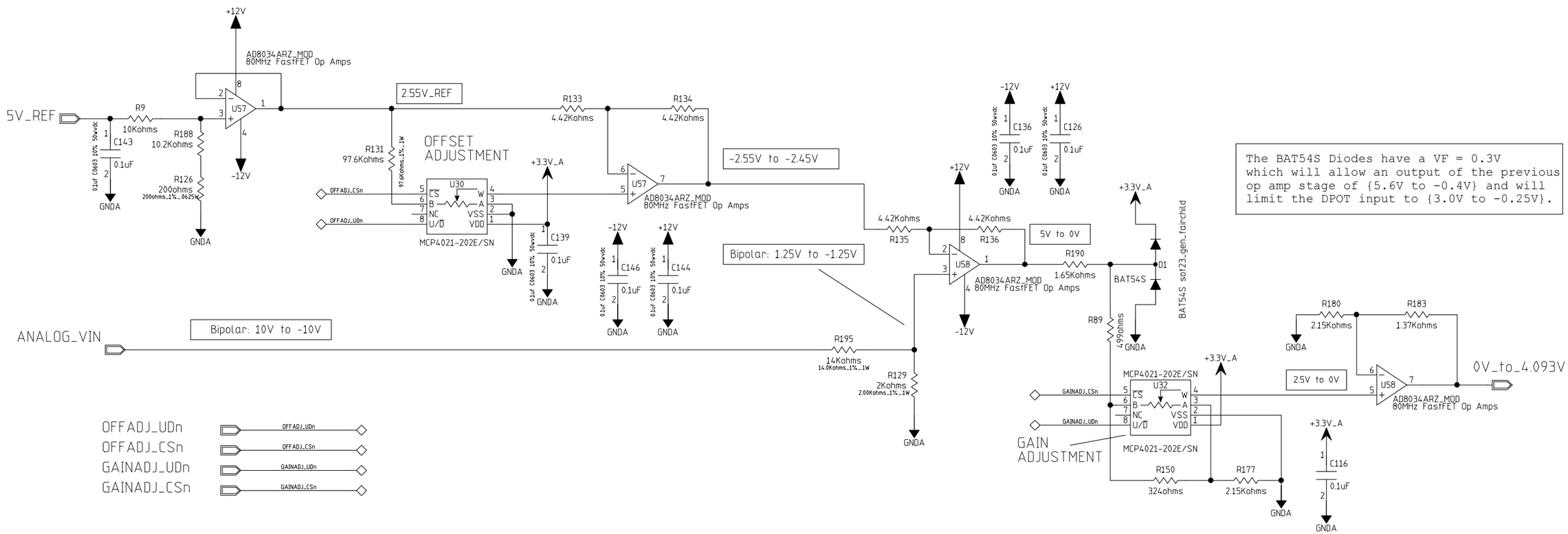
BOOSTER MI PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER		REV
B	0000-EB-282414	Schematic Page 04 of 16	

H=8ND; V=4LA



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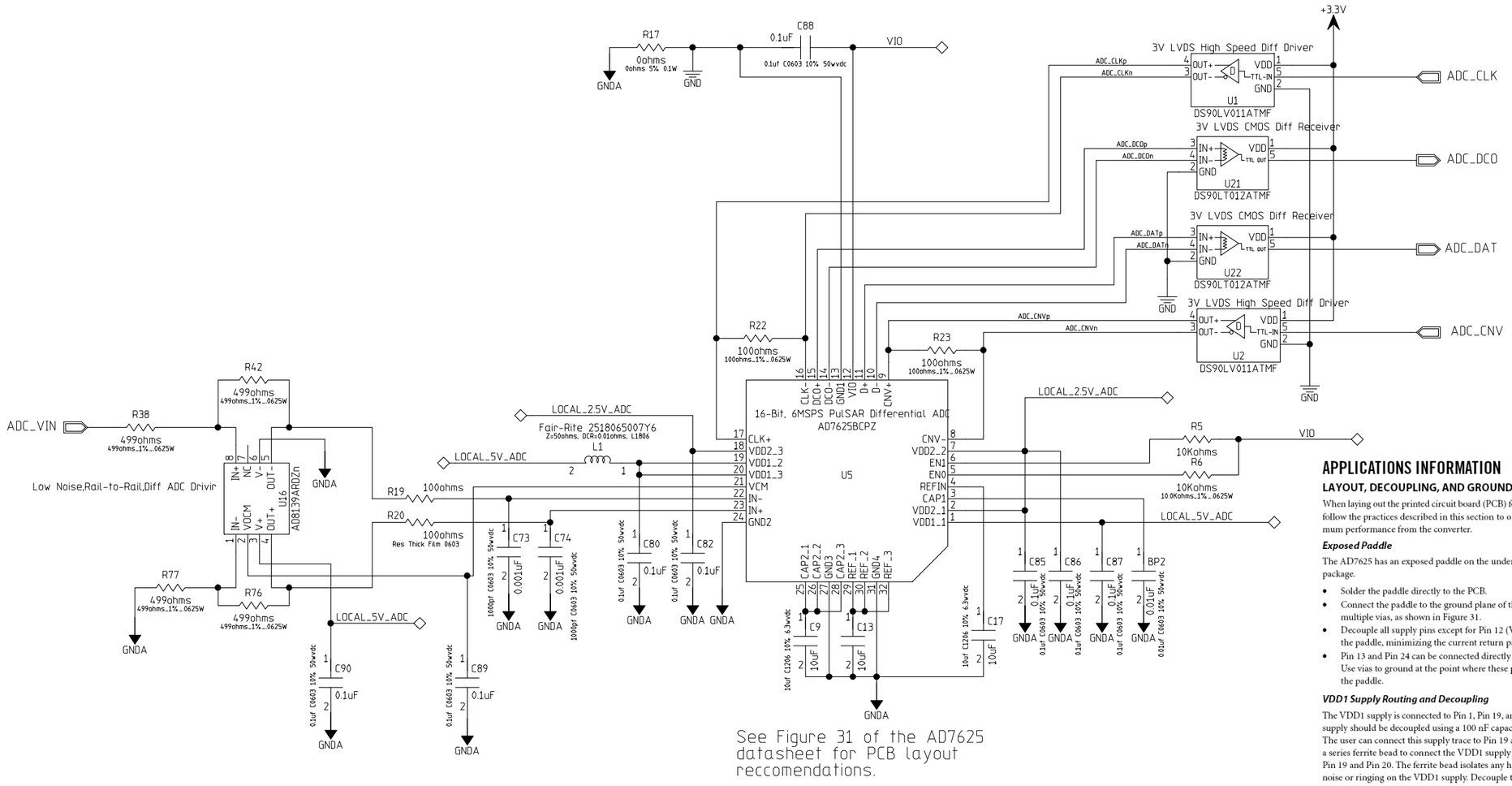
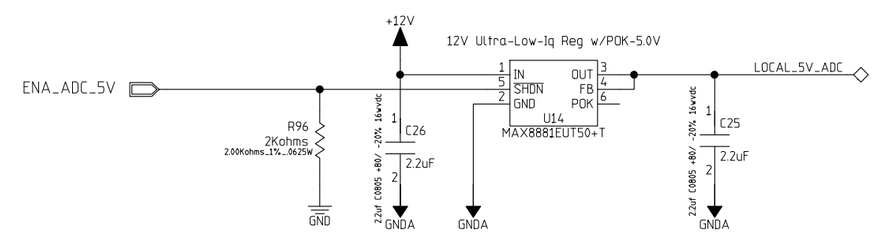
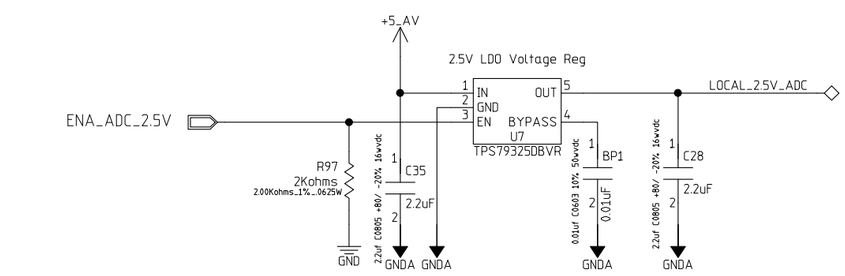
BOOSTER MI PHASE-LOCK CONTROLLER

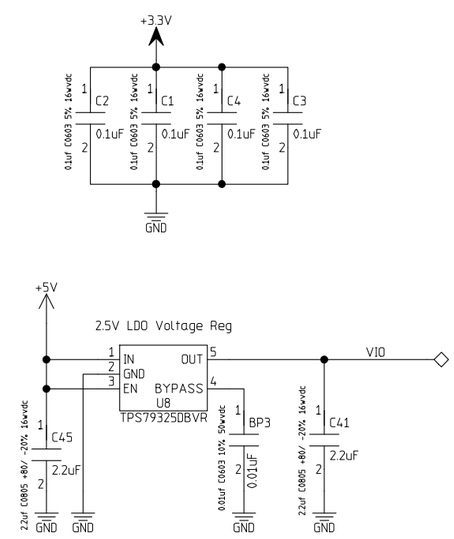
SIZE	DRAWING NUMBER		REV
B	0000-EB-282414	Schematic Page 05 of 16	

H=8ND; V=4LA









APPLICATIONS INFORMATION

LAYOUT, DECOUPLING, AND GROUNDING

When laying out the printed circuit board (PCB) for the AD7625, follow the practices described in this section to obtain the maximum performance from the converter.

Exposed Paddle

The AD7625 has an exposed paddle on the underside of the package.

- Solder the paddle directly to the PCB.
- Connect the paddle to the ground plane of the board using multiple vias, as shown in Figure 31.
- Decouple all supply pins except for Pin 12 (VIO) directly to the paddle, minimizing the current return path.
- Pin 13 and Pin 24 can be connected directly to the paddle. Use vias to ground at the point where these pins connect to the paddle.

VDD1 Supply Routing and Decoupling

The VDD1 supply is connected to Pin 1, Pin 19, and Pin 20. The supply should be decoupled using a 100 nF capacitor at Pin 1. The user can connect this supply trace to Pin 19 and Pin 20. Use a series ferrite bead to connect the VDD1 supply from Pin 1 to Pin 19 and Pin 20. The ferrite bead isolates any high frequency noise or ringing on the VDD1 supply. Decouple the VDD1 supply to Pin 19 and Pin 20 using a 100 nF capacitor to GND. This GND connection can be placed a short distance away from the exposed paddle.

VIO Supply Decoupling

Decouple the VIO supply applied to Pin 12 to ground at Pin 13.

Layout and Decoupling of Pin 25 to Pin 32

Connect the outputs of Pin 25, Pin 26, and Pin 28 together and decouple them to Pin 27 using a 10 µF capacitor with low ESR and low ESL.

Reduce the inductance of the path connecting Pin 25, Pin 26, and Pin 28 by widening the PCB traces connecting these pins.

A similar approach should be taken in the connections used for the reference pins of the AD7625. Connect Pin 29, Pin 30, and Pin 32 together using widened PCB traces to reduce inductance. In internal or external reference mode, a 4.096 V reference voltage is output on Pin 29, Pin 30, and Pin 32. Decouple these pins to Pin 31 using a 10 µF capacitor with low ESR and low ESL.

Figure 31 shows an example of the recommended layout for the underside of the AD7625 device. Note the extended signal trace connections and the outline of the capacitors decoupling the signals applied to the REF pins (Pin 29, Pin 30, and Pin 32) and to the CAP2 pins (Pin 25, Pin 26, and Pin 28).

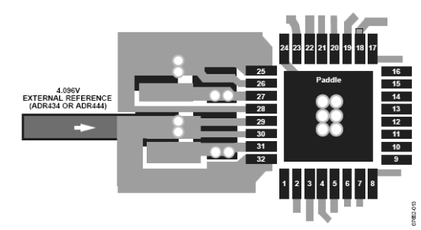


Figure 31. PCB Layout and Decoupling Recommendations for Pin 24 to Pin 32

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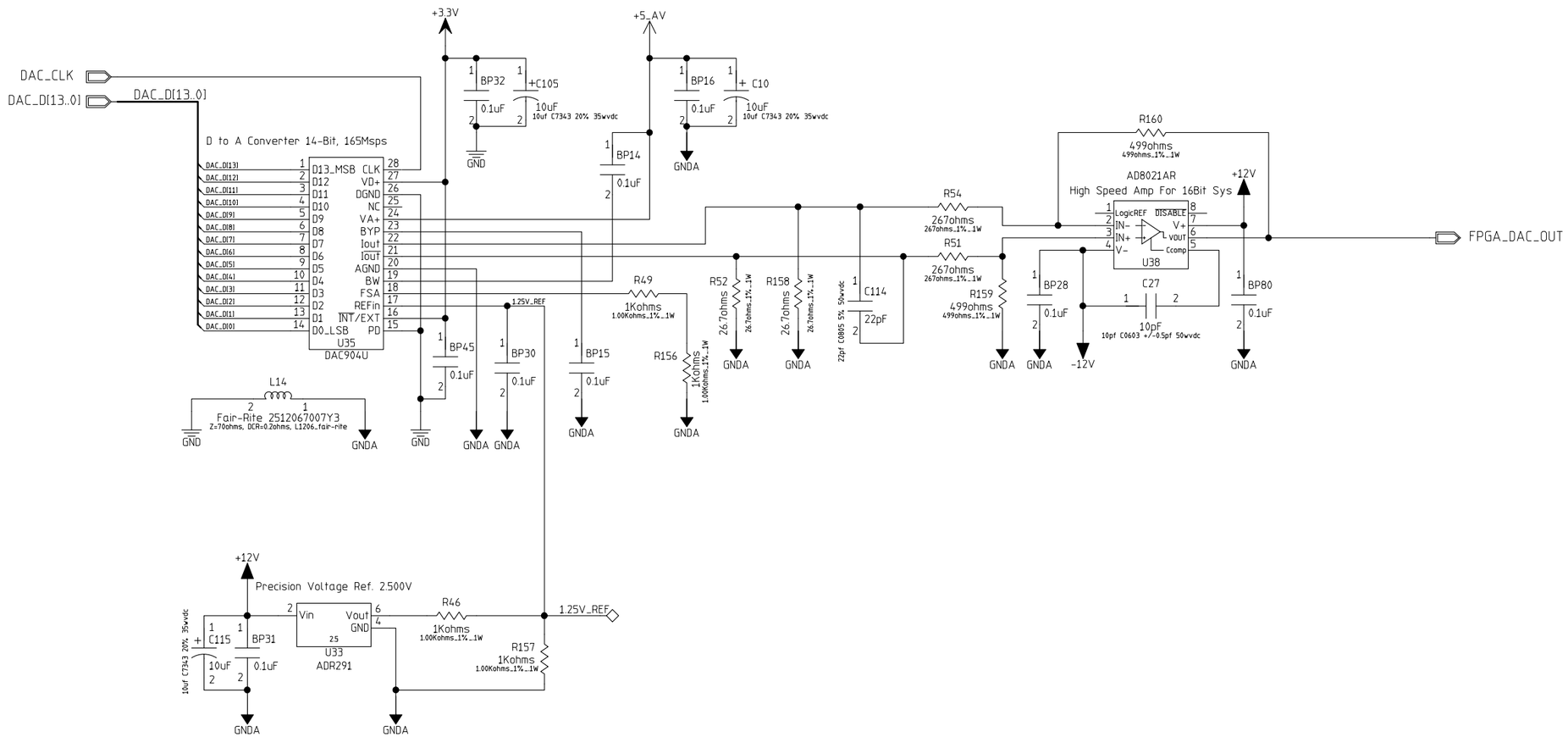
BOOSTER MI PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER		REV
B	0000-EB-282414	Schematic Page 06 of 16	

H=8ND; V=4LA



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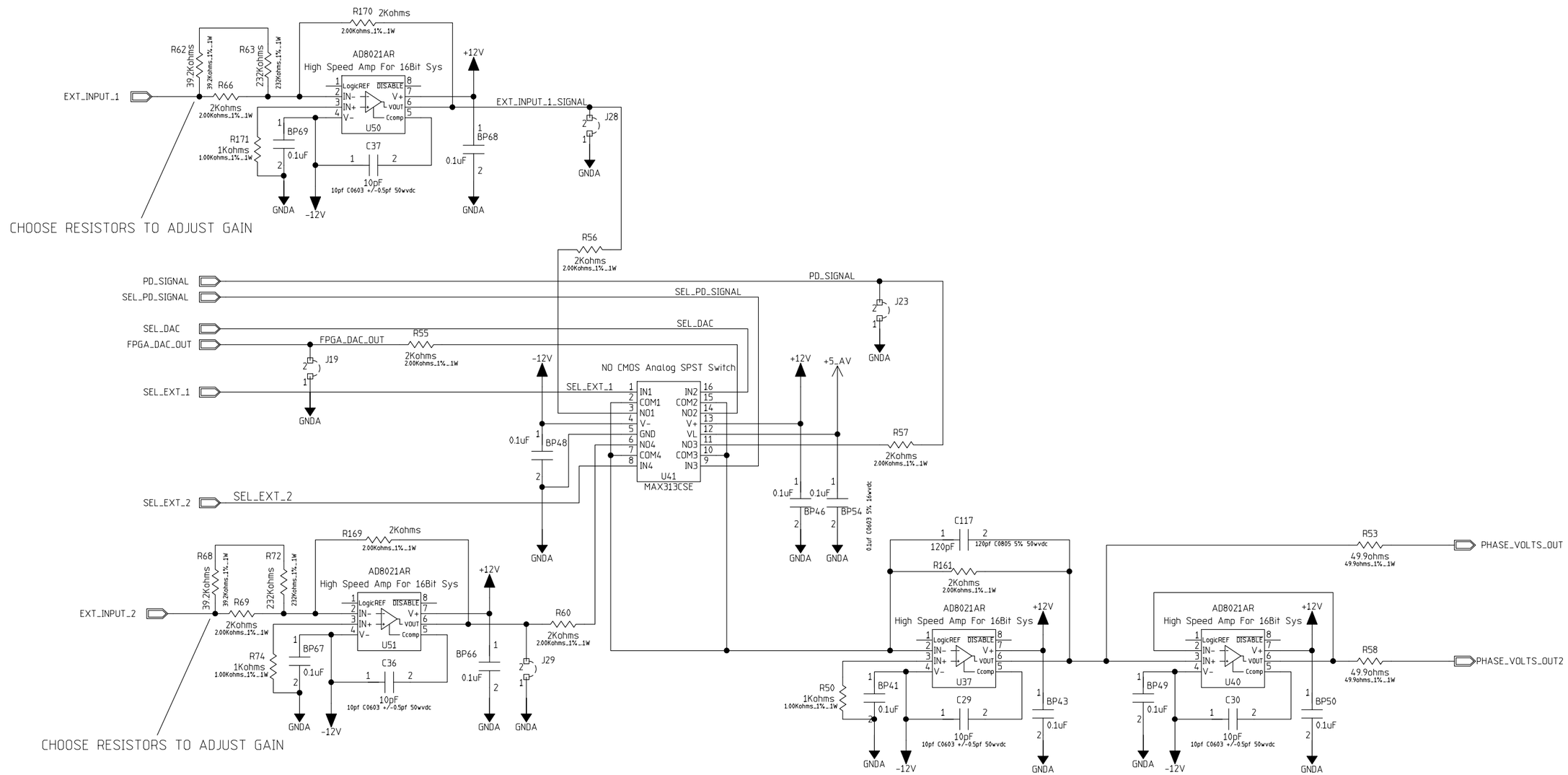
BOOSTER MI PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER		REV
B	0000-EB-282414	Schematic Page 07 of 16	

H=8ND; V=4LA



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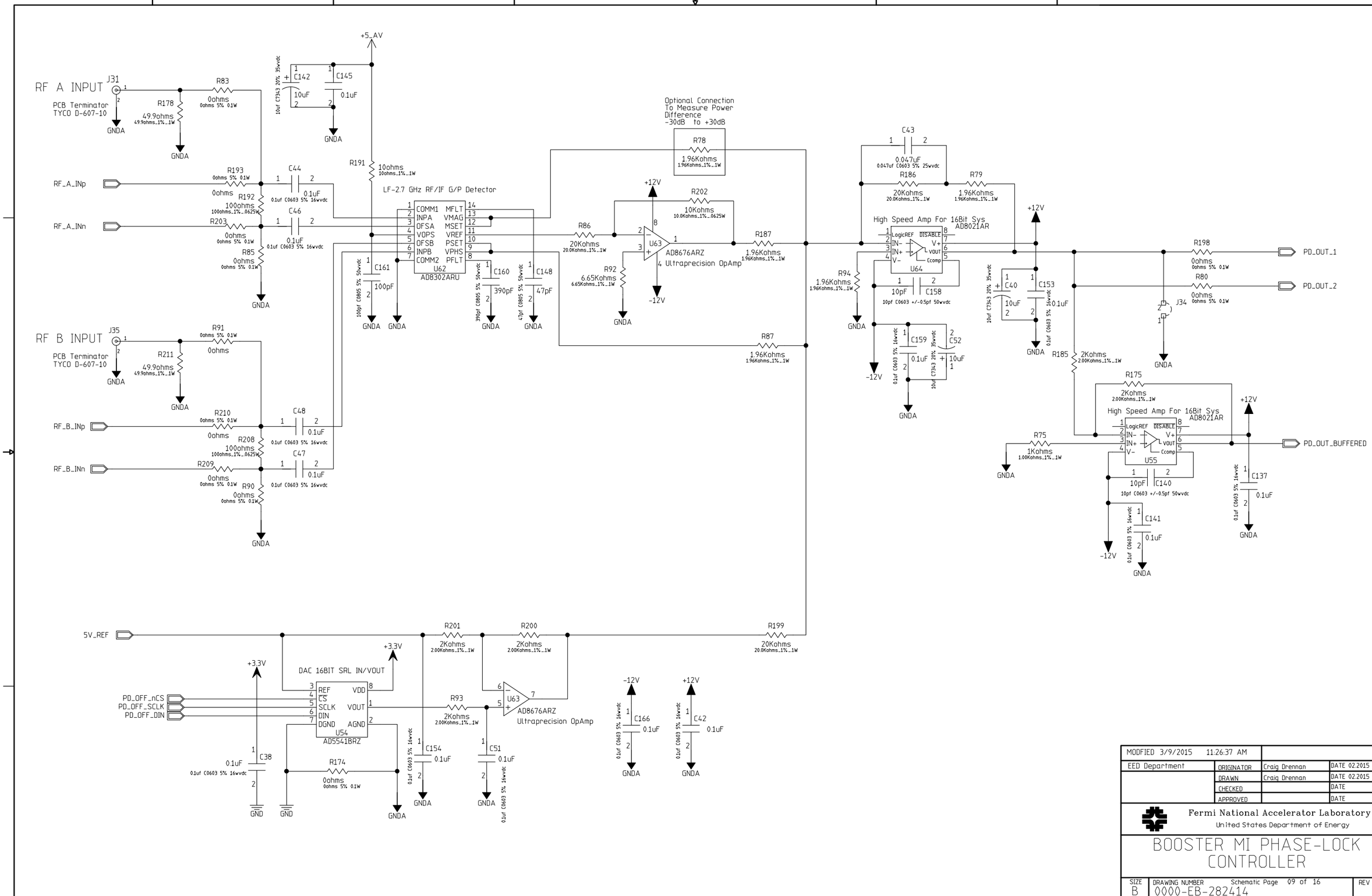
BOOSTER MI PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER		REV
B	0000-EB-282414	Schematic Page 08 of 16	

H=8ND; V=4LA



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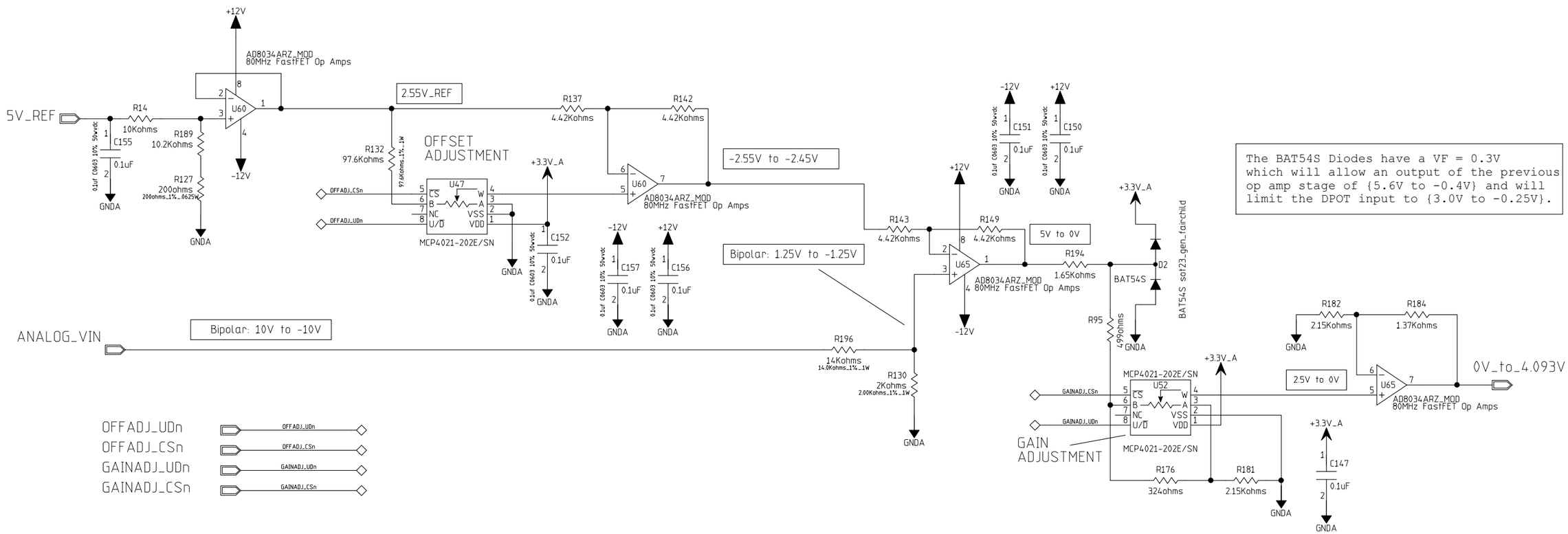
BOOSTER MI PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER		REV
B	0000-EB-282414	Schematic Page 09 of 16	

H=8ND; V=4LA



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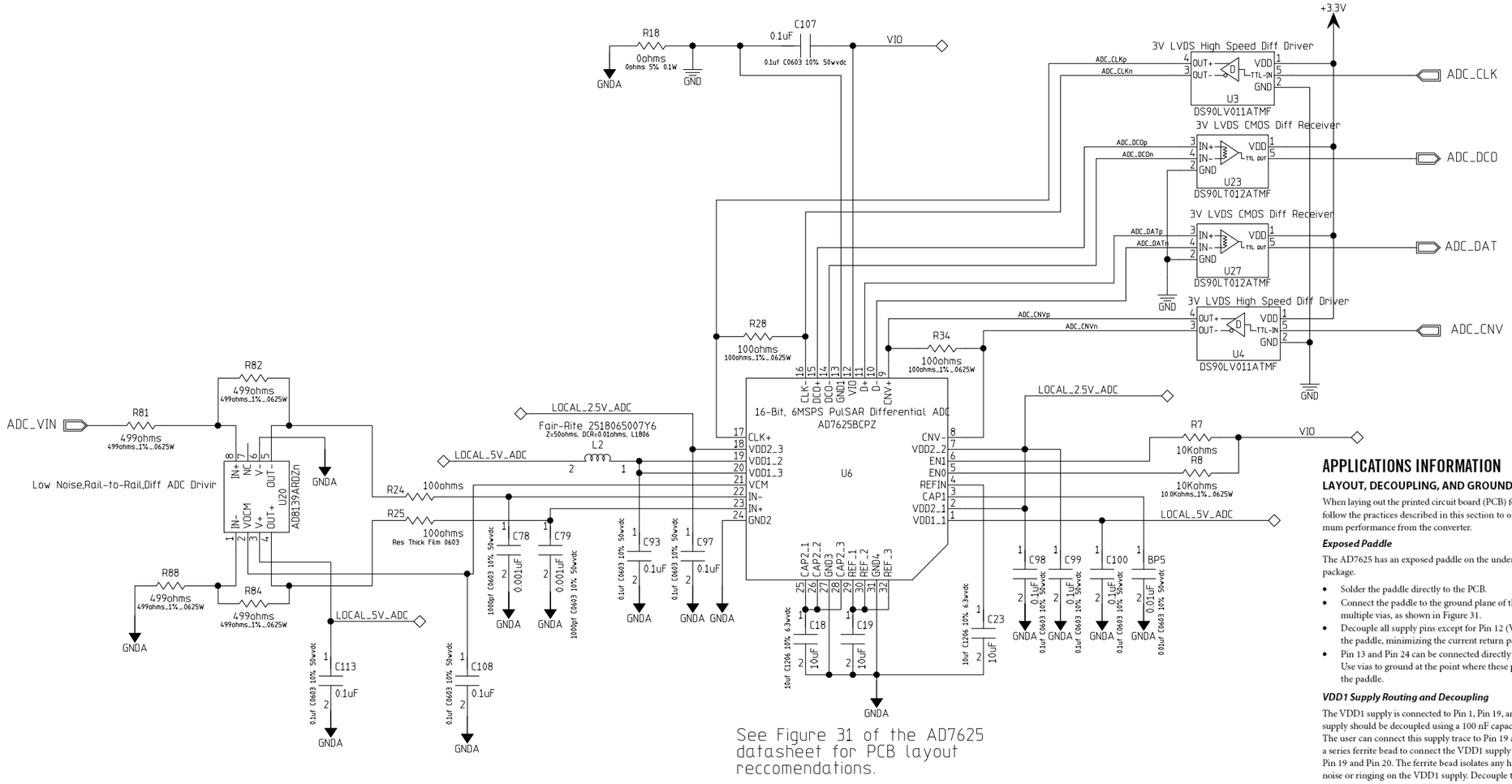
	DRAWN	Craig Drennan	DATE 02.2015
	CHECKED		DATE
	APPROVED		DATE

Fermi National Accelerator Laboratory
United States Department of Energy

BOOSTER MI PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER		REV
B	0000-EB-282414	Schematic Page 10 of 16	

H=8ND; V=4LA



APPLICATIONS INFORMATION

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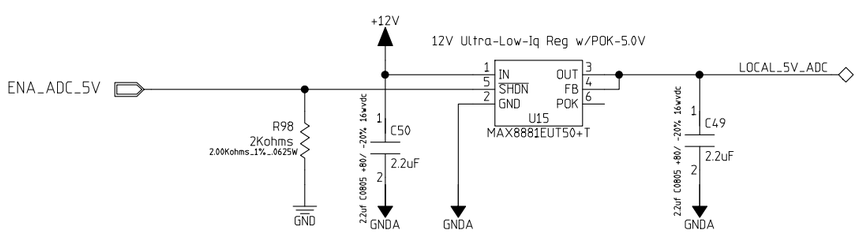

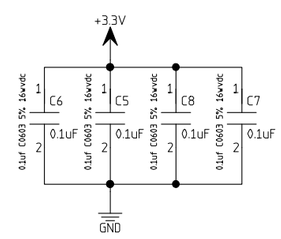

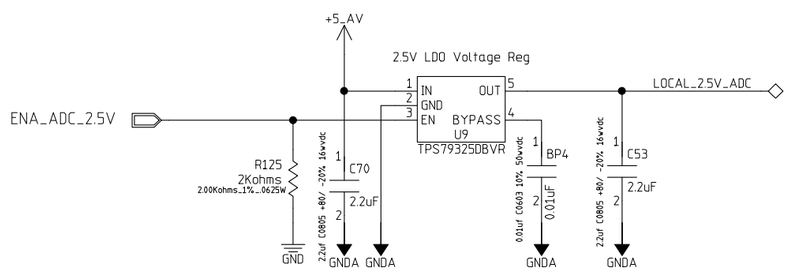

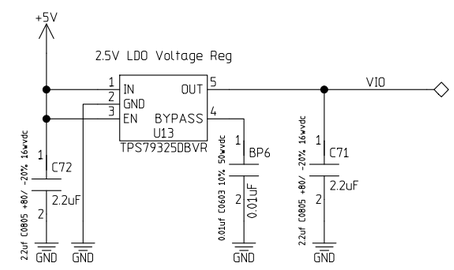

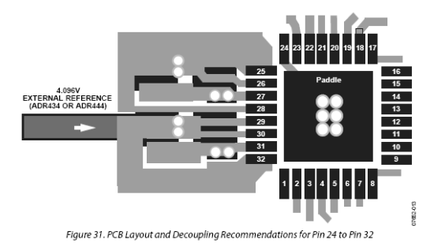

Figure 31. PCB Layout and Decoupling Recommendations for Pin 24 to Pin 32

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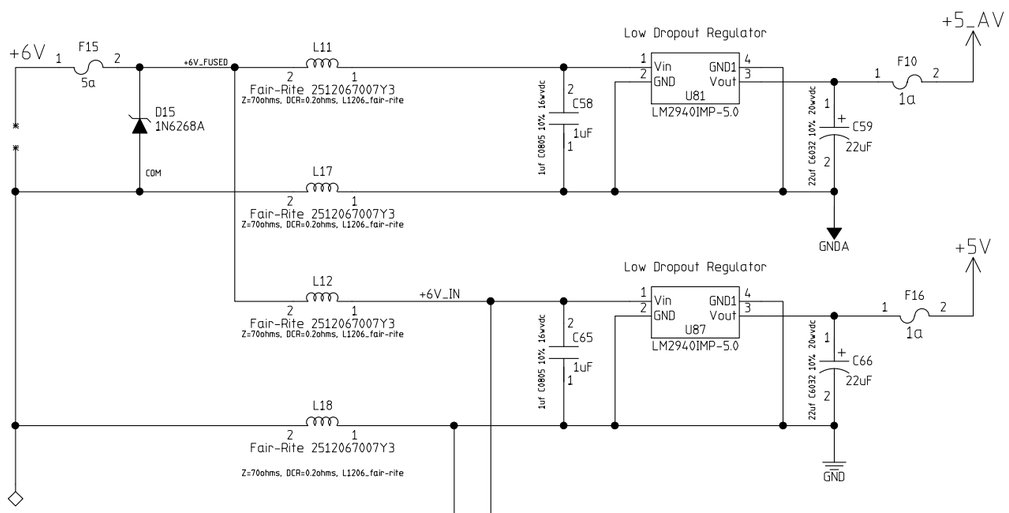
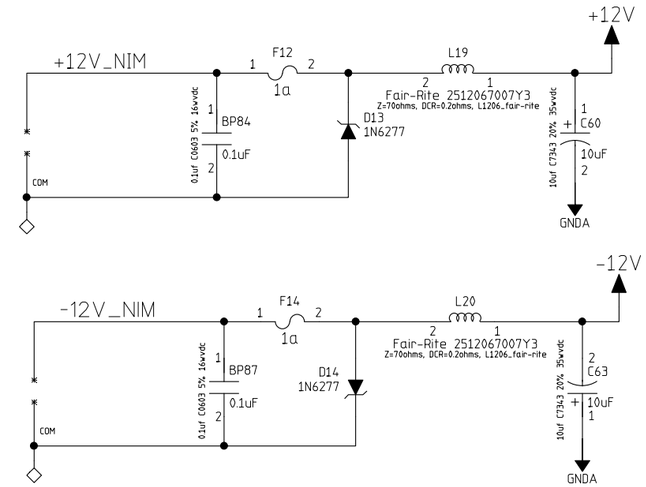
Fermi National Accelerator Laboratory
United States Department of Energy

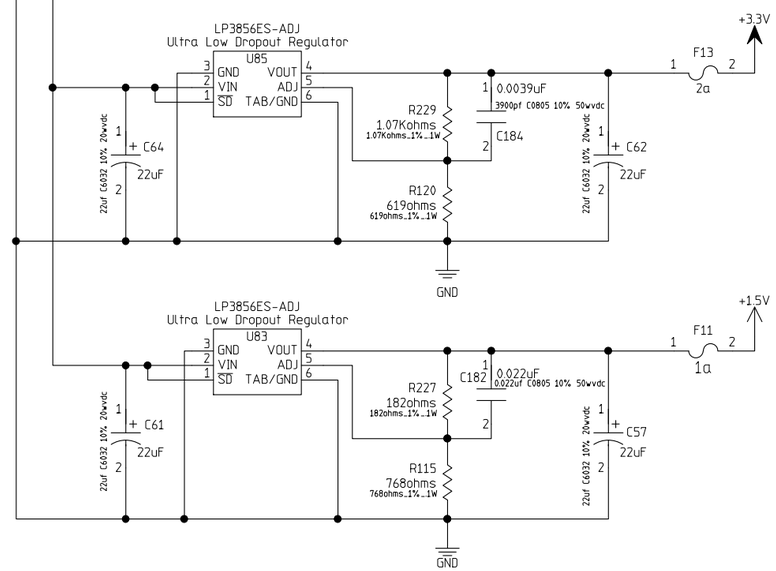
BOOSTER MI PHASE-LOCK CONTROLLER

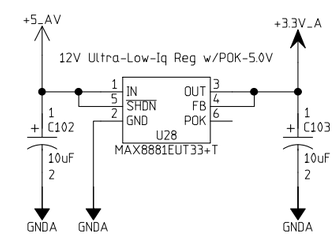
SIZE	DRAWING NUMBER		REV
B	0000-EB-282414	Schematic Page 11 of 16	

H:8ND; V:4LA









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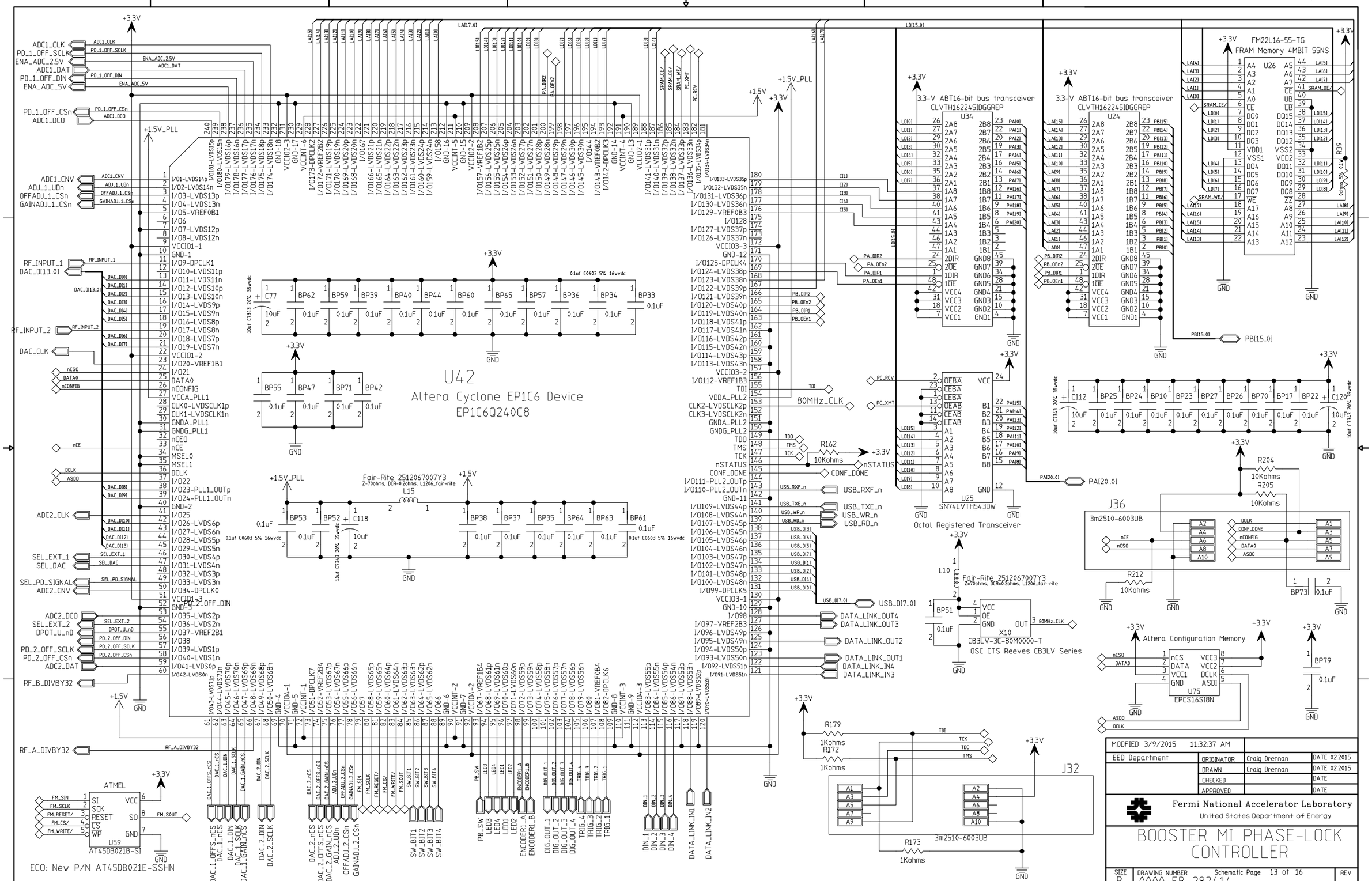
BOOSTER MI PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER		REV
B	0000-EB-282414	Schematic Page 12 of 16	

H=8ND; V=4LA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CLVTH162245IDGGREP
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U26
FM22L16-55-TG
FRAM Memory 4MBIT 55NS
U25
SN74LVTH543DW
Octal Registered Transceiver
U59
ATMEL
AT45DB021B-SI
ECO: New P/N AT45DB021E-SSHN
U75
EPCS16SI8N
Altera Configuration Memory
X10
CB3LV-3C-80M0000-T
OSC CTS Reeves CB3LV Series
J36
3m2510-6003UB
J32
3m2510-6003UB
Fair-Rite 2512067007Y3
L15
L10
80MHz_CLK
R162
10Kohms
R204
10Kohms
R205
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R39
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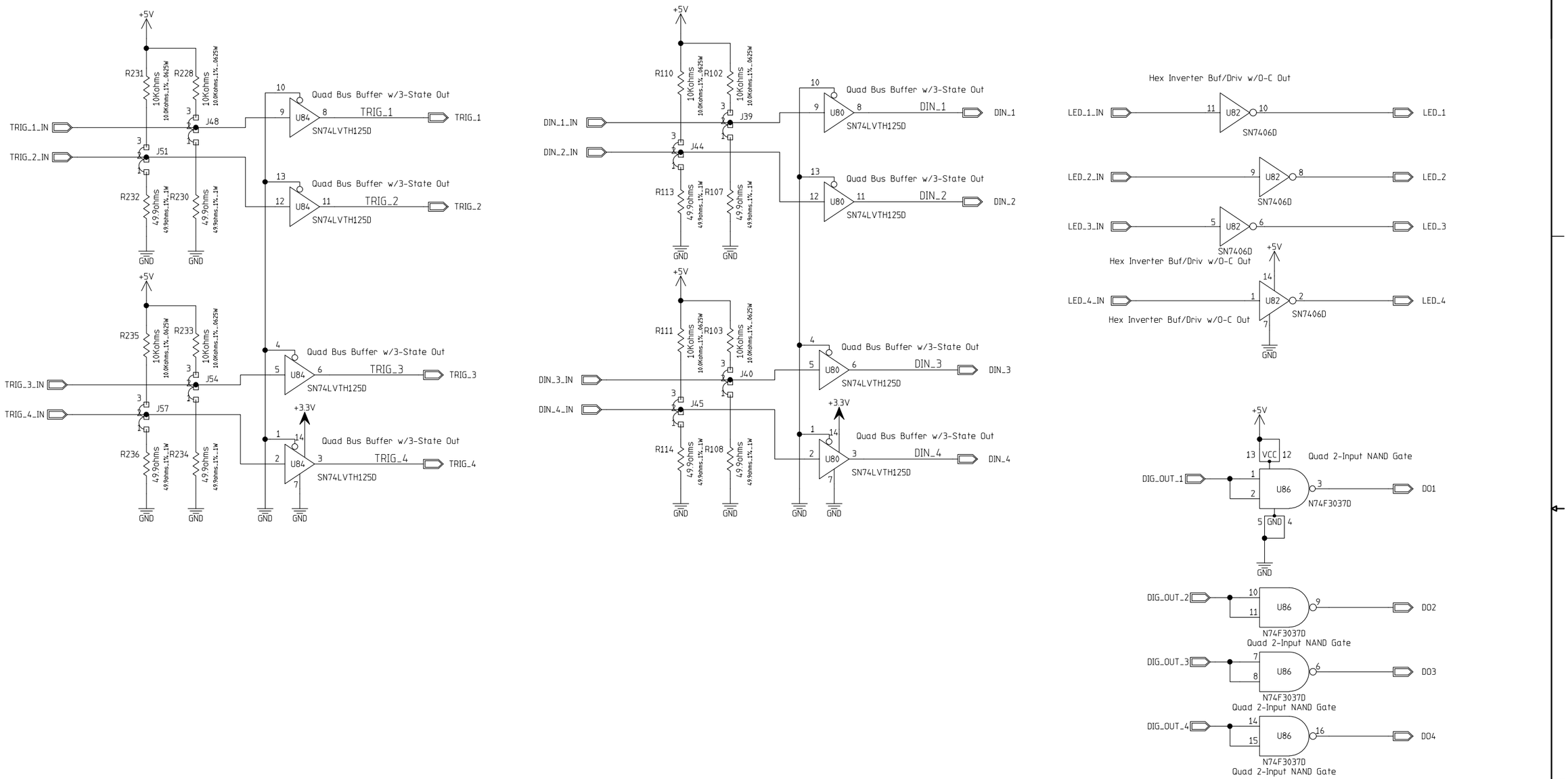
EED Department
ORIGINATOR Craig Drennan DATE 02.2015
DRAWN Craig Drennan DATE 02.2015
CHECKED DATE
APPROVED DATE
Fermi National Accelerator Laboratory
United States Department of Energy
BOOSTER MI PHASE-LOCK CONTROLLER
SIZE B
DRAWING NUMBER 0000-EB-282414
Schematic Page 13 of 16
REV



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	APPROVED		DATE

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BOOSTER MI PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER		REV
B	0000-EB-282414	Schematic Page 14 of 16	

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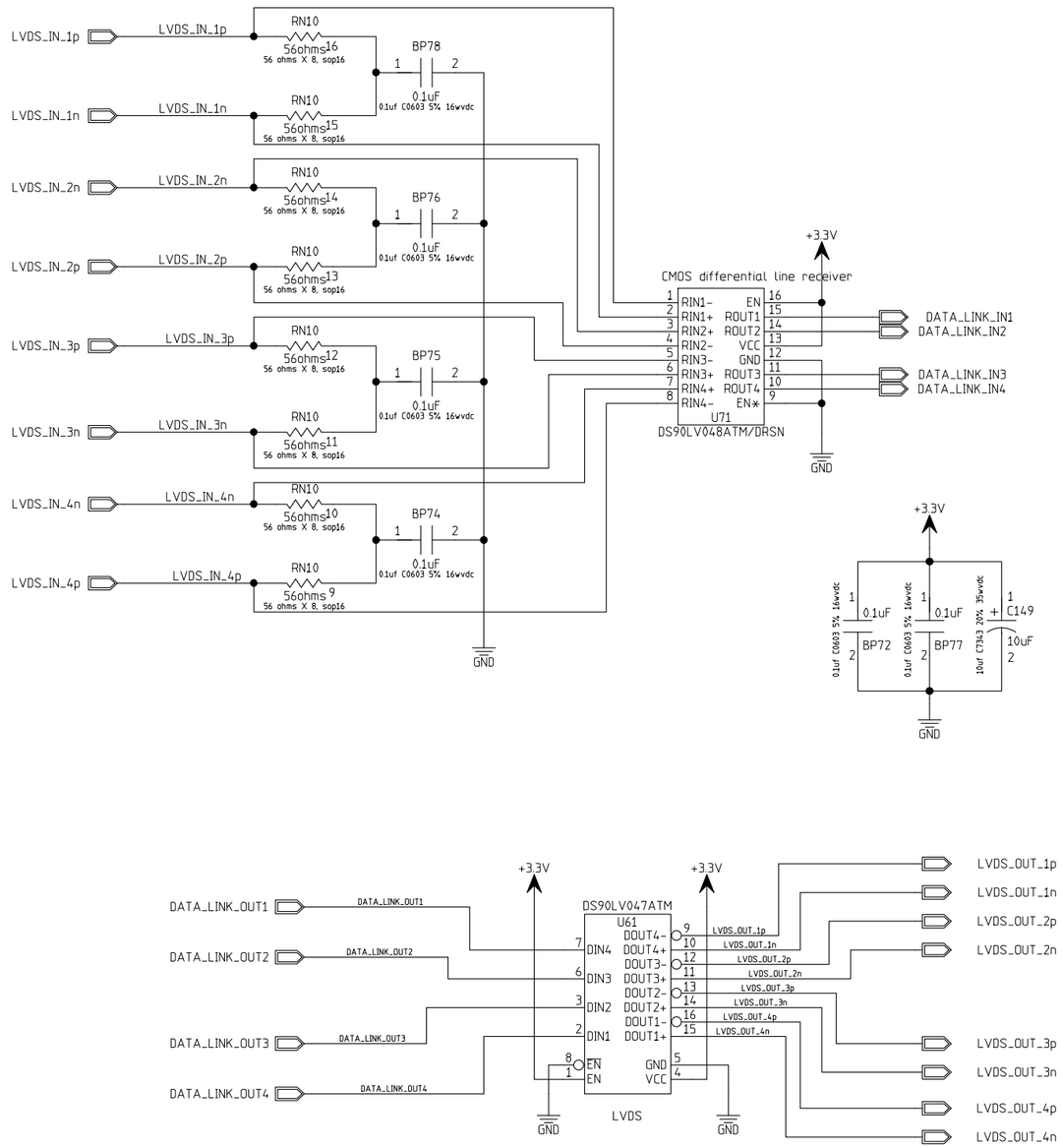

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	APPROVED		DATE

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BOOSTER MI PHASE-LOCK CONTROLLER

SIZE	DRAWING NUMBER	Schematic Page 15 of 16	REV
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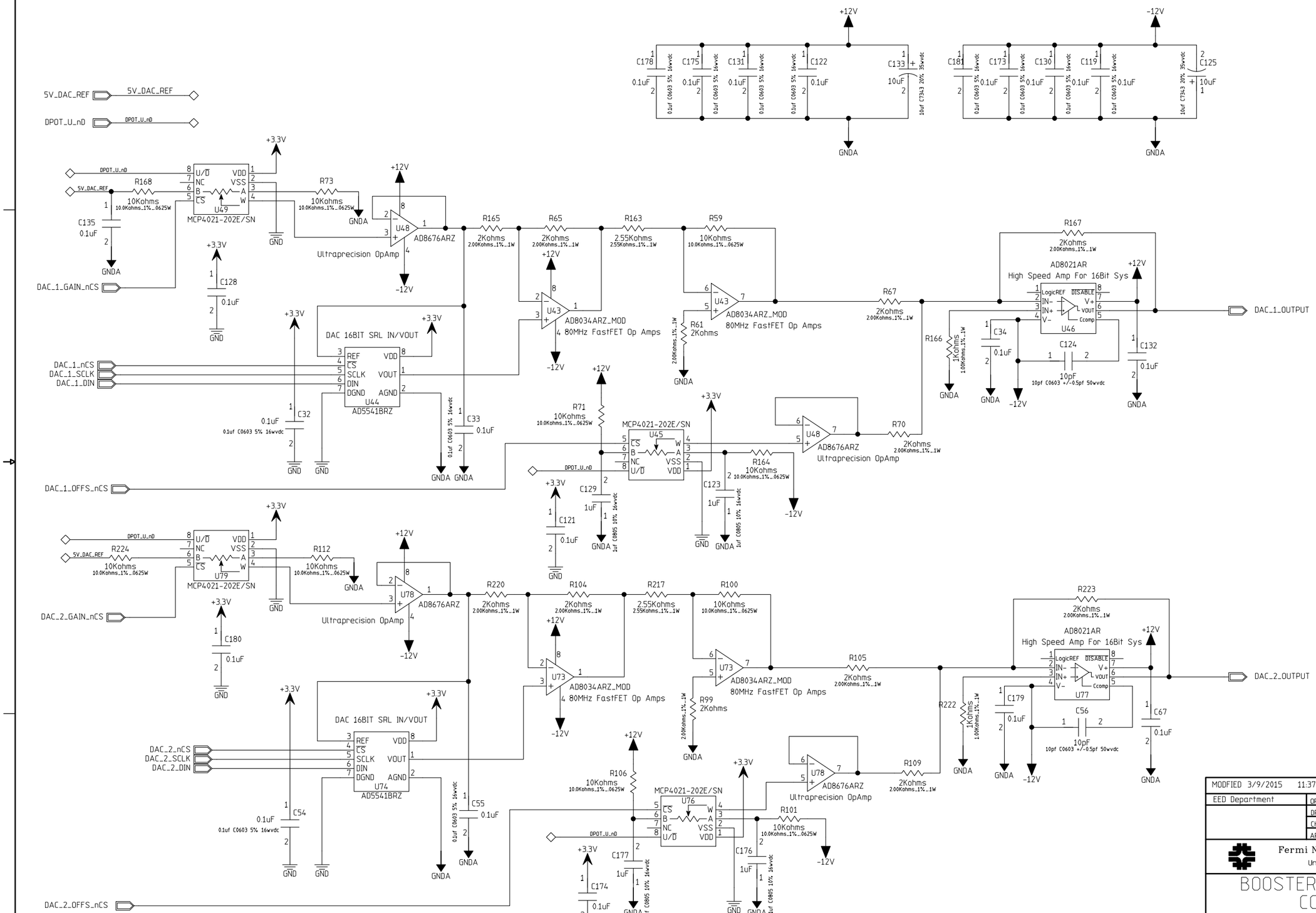
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DAC_1_OUTPUT
DAC_2_GAIN_nCS
DAC_2_nCS
DAC_2_SCLK
DAC_2_DIN
DAC_2_OFFS_nCS
DAC_2_OUTPUT
MCP4021-202E/SN
AD8676ARZ
Ultraprecision OpAmp
AD8034ARZ_MOD
80MHz FastFET Op Amps
DAC 16BIT SRL IN/VOUT
AD5541BRZ
AD8021AR
High Speed Amp For 16Bit Sys
+12V
-12V
+3.3V
GNDA
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DRAWN Craig Drennan DATE 02.2015
CHECKED DATE
APPROVED DATE
Fermi National Accelerator Laboratory
United States Department of Energy
BOOSTER MI PHASE-LOCK CONTROLLER
SIZE B
DRAWING NUMBER 0000-EB-282414
Schematic Page 16 of 16
REV
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