Design Notes Of The Regulated Current Arc Modulator For The FNAL H- Source

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Abstract

We describe in these notes the theory and implementation of the current regulated arc modulator used in the H- source. Our discussion includes the low current, high current and after boxing circuit tests of the modulator. We have made several interesting "kludges" to the circuit in the boxed configuration in order for it to function properly. We will also discuss the test results after the modulator is connected to the H- source.

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I. INTRODUCTION

The H- source at FNAL has always operated with a voltage regulated arc modulator. BNL (Brookhaven National Laboratory) has operated their H- source with a current regulated arc modulator for decades and has communicated to us that the H- source runs "better" with a current regulated arc modulator when compared to a voltage regulated arc modulator. The reason for the source running "better" with a current regulated modulator is that the output beam current is intimately related to the arc current. A better regulated arc current means that the H- current is more stable.

Our initial intent was to build an identical version here. However, after obtaining a set of design notes from BNL we found that they were written in Russian and were quite cryptic as to what they did. It took us a long time to decipher them but, even with a fair amount of effort, we did not completely understand their implementation. And thus, we decided to design our own circuit, but based on their design, so that we could understand our own implementation. Also, as part of the re-design process, we replaced the obsolete components used in BNL's current regulated modulator with modern ones.

We have written in these notes the theory of the current feedback loop and the measurements that we have done at low power, high power and after the circuit has been boxed and connected to a H- source. We will also discuss the interesting "kludges" that we have used in order for the boxed version to work properly. Finally, we connected our modulator to the H- source and tested it with more kludges to make it work.

II. THEORY

The basic feedback loop that forms the basis of the regulated constant current arc modulator design is shown in Fig. 1. The user sets the current I_v going through the H- source impedance, Z_s, by setting V^+. We can prove that the current, I_v flowing through Z_s is independent of it, and is only dependent on V^+ and Z_f. The proof is as follows:

From Ohm's law and Kirchoff's equations, we have the following equations

$$I_f = \frac{V_o - V^-}{Z_f} \tag{1}$$

$$I^- = I_f + I_v \tag{2}$$

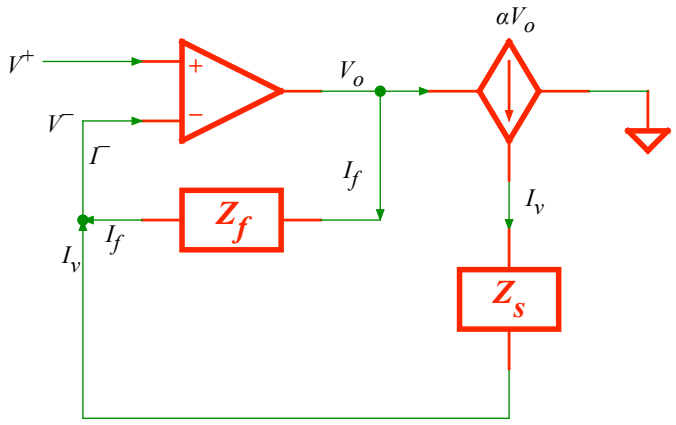

FIG. 1. This is the feedback loop that forms the basis for the entire regulated constant current arc modulator. Z_f represents the feedback "resistor" which can be complex. Z_s is the H- source impedance which can also be complex. In fact, not only is Z_s time dependent, it can also be a source of current. See section II A for the analysis.

If we assume that the opamp is ideal,[1] then we must have

$$V^+ = V^- \quad \Rightarrow \quad I_f = \frac{V_o - V^+}{Z_f} \tag{3}$$

$$I^- = 0 \quad \Rightarrow \quad I_v = -I_f \tag{4}$$

We can use the above two equations to obtain

$$I_v = \frac{V^+ - V_o}{Z_f} \tag{5}$$

But, the size of I_v is determined by the V_o. The relationship between I_v and V_o is

$$I_v = \alpha V_o \tag{6}$$

where α is the voltage to current conversion factor (and can be thought of as the transconductance of the voltage to current converter). Thus, we can substitute Eq. 6 to Eq. 5 to get

$$I_v = \frac{V^+ - I_v/\alpha}{Z_f} \tag{7}$$

And clearly when $\alpha \to \infty$, we have

$$\boxed{\lim_{\alpha\to\infty} I_v = \frac{V^+}{Z_f}} \tag{8}$$

which is independent of Z_s. This is, of course, what we require — that no matter how the source impedance Z_s changes, the current, I_v, through it remains constant.

A. H- source producing a back current

For completeness, we have to also consider the case where the H- source produces a back current I_s that flows back into the basic feedback loop. The addition of I_s to the basic feedback loop is shown in Fig. 2.

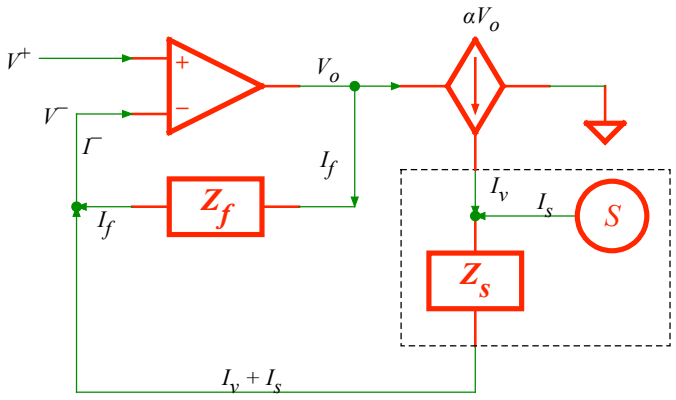

FIG. 2. We have added a current I_s that flows from the H- source back into the basic feedback loop.

The analysis is the same as before, and we find that the current flowing through Z_s is given by

$$(I_v + I_s) = \frac{V^+ - I_v/\alpha}{Z_f} \tag{9}$$

We can solve for I_s to get

$$I_s = -\frac{I_v}{\alpha Z_f} + \frac{V^+ - I_v Z_f}{Z_f} \tag{10}$$

and therefore

$$(I_v + I_s) = \frac{\alpha V^+ - I_v}{\alpha Z_f} \tag{11}$$

We have in the limit where $\alpha \to \infty$

$$\boxed{\lim_{\alpha\to\infty}(I_v + I_s) = \frac{V^+}{Z_f}} \tag{12}$$

which is the same result as before (Eq. 8). This means that even when the H- source has any back current, the basic feedback loop will compensate for it to always keep the current flowing through it to be exactly V^+/Z_f.

B. Stepping down I_v

We have to step down the current I_v because it is in the amp range while opamps can only handle current in the milliamp range. The way we step down I_v is to add a shunt resistor R_p to the basic feedback loop shown in Fig. 3.

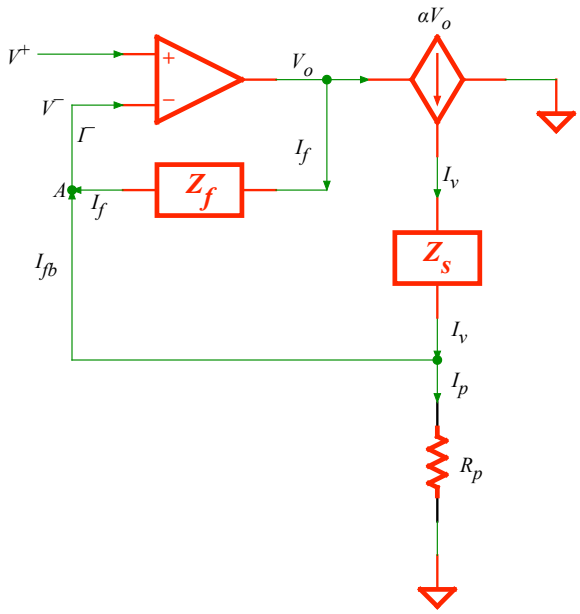

FIG. 3. We can step down I_v by adding a shunt resistance R_p to the basic feedback loop.

We can calculate the relationship between I_v and I_f as follows. Again, for an ideal opamp,

$$I^- = I_f + I_{fb} = 0 \qquad \Rightarrow \qquad I_{fb} = -I_f \tag{13}$$

and it is also obvious that the potential difference at the node labelled "A" and ground is $V^- = V^+$ and thus the voltage across R_p must also be V^+. Therefore, the current flowing through R_p is given by

$$I_p = \frac{V^+}{R_p} \tag{14}$$

and thus

$$I_v = I_p + I_{fb} \tag{15}$$

$$= \frac{V^+}{R_p} - \frac{V_0 - V^+}{Z_f} \tag{16}$$

$$= \frac{V^+}{R_p} - \frac{I_v/\alpha - V^+}{Z_f} \tag{17}$$

In the limit where $\alpha \to \infty$, we have

$$\boxed{\lim_{\alpha\to\infty} I_v = V^+ \left(\frac{1}{R_p} + \frac{1}{Z_f}\right) \approx \frac{V^+}{R_p} + I_f} \tag{18}$$

where I have made the approximation that $I_f = V^+/Z_f$ as long as $V_0 \ll V^+$.

The above equation shows us how the "step down" occurs. If R_p is a small shunt, and for illustration, let us suppose $R_p = 0.1\ \Omega$, $V^+ = 1$ V, and $Z_f = 1$ kΩ, then we get $I_f = 1$ mA and $I_v \approx 10$ A. Hence, the "step down" is 10^4 from I_v to I_f.

We can, in fact, make a further approximation to get a relationship between the regulated current I_v flowing into the source impedance Z_s and V^+ set by the user. We have, from Eq 18 for $I_f \ll I_v$

$$I_v \approx \frac{V^+}{R_p} \quad \text{when } I_f \ll I_v \tag{19}$$

The above is a useful approximation for calculating the amount of regulated current flowing through the source.

1. Negative current through Z_s

The feedback loop shown in Fig. 3 has a positive current I_v flowing through Z_s. For the H- source, we need a negative current flowing into it. In order to achieve this requirement, we have to modify our feedback loop slightly. Our modification takes Z_s out from its location shown in Fig. 3 and places it at its new location shown in Fig. 4. In effect, I_v, flows from ground back to the voltage to current converter, which means that a "negative" current flows into Z_s. The relationships that we have found in section II B still applies for this new circuit.

III. SPICE MODEL

The spice model of the feedback loop is shown in Fig. 4. It can be divided into three parts:

- low current loop.
- transition between low and high current loops.
- high current loop.

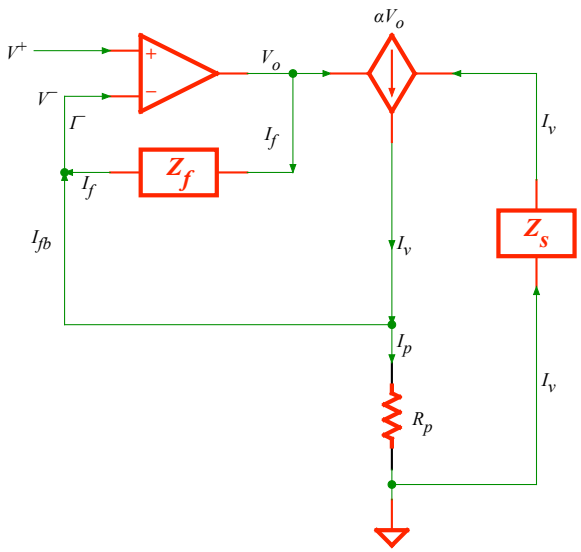

FIG. 4. This circuit shows how we modified the feedback loop so that I_v flows from ground back to the voltage to current converter. In effect, a "negative" current flows through Z_s.

The voltage to current converter consists of an opamp configured to be a positive high gain amplifier connected to an IGBT (insulated gate bipolar transistor) that acts as a gate for controlling the current flowing out of the high current (and voltage) power supply. Notice that the power supply is "floating", i.e. it is not directly connected to the ground reference.

The SPICE model can be used to test the feedback loop for different values of the components. However, we have found that SPICE *can* produce unstable results (and therefore erroneous results) that meet specifications! Therefore, at best, it is only a guide as to whether the circuit is viable or not.

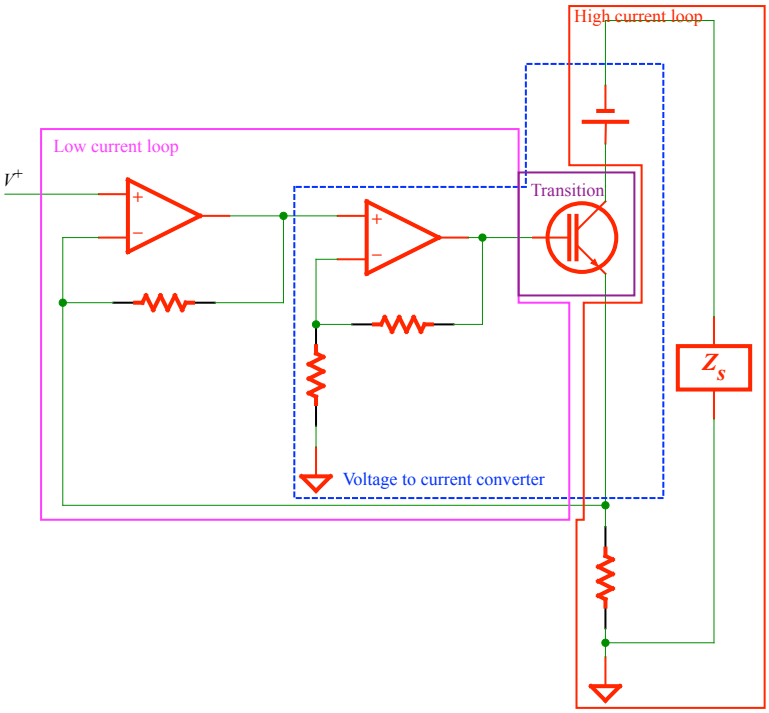

FIG. 5. This is the spice model of the feedback loop. It can be divided into 3 parts: (a) a low current loop, (b) the transition between the low current and high current loops and (c) the high current loop. The voltage to current converter consists of one opamp configured as a positive high gain amplifer connected to an IGBT that acts as a controlled gate for the high voltage source.

IV. IMPLEMENTATION

The required specifications of the regulated current arc modulator is shown in Table I.

TABLE I. **Specifications**

Parameter	**Value**	**Units**
Pulse width	100 – 300	μs
Rise and fall times	< 20	μs
Regulated current range	1–20	A
Current ripple amplitude	< 1	%

A. Low current implementation and test

The low current loop as implemented for a performance test is shown in Fig. 6. The upstream opamp is a Linear Technology LT1226 [2] that has a 1 GHz gain bandwidth product (GBP). There are a few considerations that will be discussed in section IV B when using this opamp in this (and perhaps other) applications. It is necessary to use such a fast opamp because of the required specifications shown in Table I.

For low current testing, the downstream opamp is an OP27 [3] that has an 8 MHz GBP. In the first prototype, we had used the LT1226 in place of the OP27. However, the LT1226's pre-disposition to self oscillation did not make it a good choice for this stage. We will show from our measurements that despite the manufacturer's OP27 GBP specifications, it handles the $\sim$100 μs pulses very well.

Note: It is important to note that the OP27 is not a panacea from self-oscillations. We found that during our high current tests, the OP27 oscillates as well. See Fig. 8. These oscillations went away when we replaced the OP27 with the LT1226.

Finally, the IGBT is an IXYS GenX4 high voltage IGBT [4]. It handles up to 650 V and 160 A at 25°C and thus meets our specifications if properly cooled.

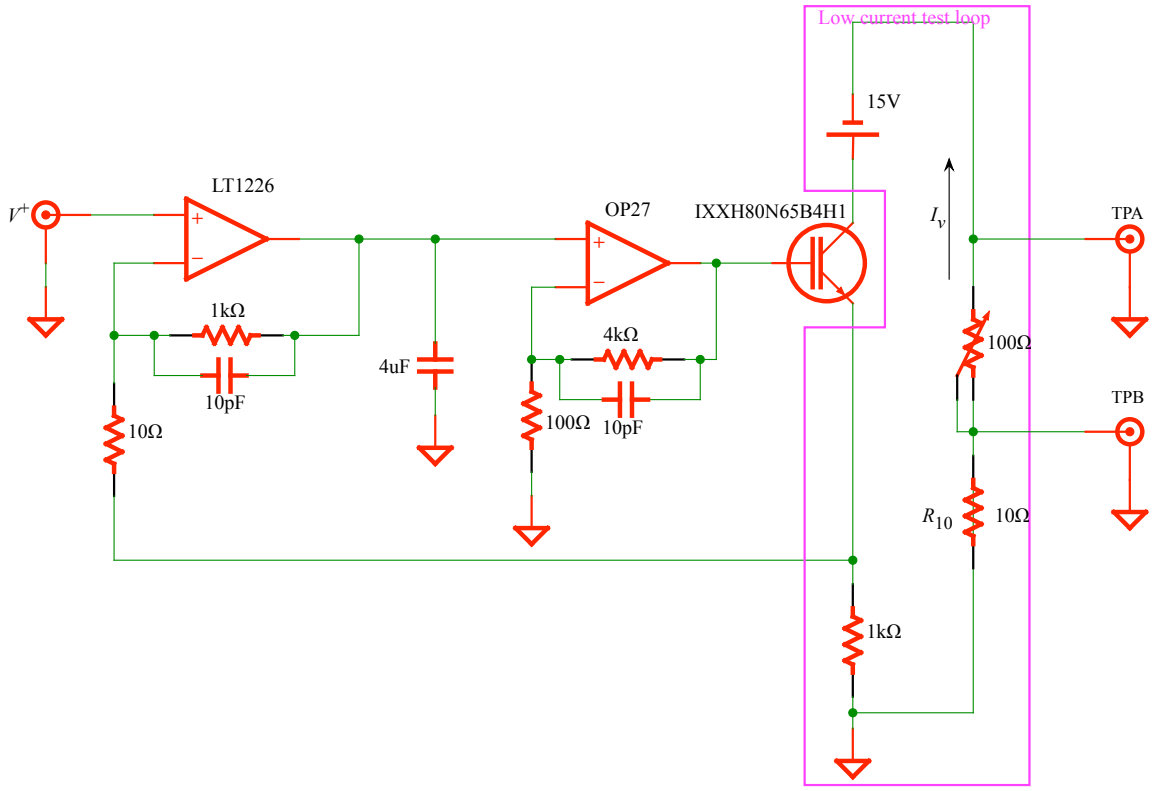

FIG. 6. This is the low current circuit used to test the basic feedback loop. Z_s has been replaced with a 10 Ω and a 100 Ω variable resistor in series. R_p is set to 100 kΩ to limit the current in the low current test loop to < 10 mA. The 4 μF capacitor at the output of the LT1226 is necessary to short the sine waves from the self oscillation of the LT1226 to ground.

B. LT1226 considerations

The LT1226 has a pre-disposition to self-oscillate. See Fig. 7. We tried the following to stop these oscillations:

- Addition of a ground plane. This removes a modulation on top of the oscillation.
- Addition of input power bypass capacitors, 0.1 μF and 1 μF connected in parallel, for every opamp.
- Addition of a 10 pF in parallel with the 1 kΩ feedback resistor. This is recommended in the LT1226 datasheet.

Unfortunately, we were unable to eliminate the oscillations with the above standard practice methods. Our crude solution is to add a 4 μF capacitor to short these oscillations to ground.

This solution, unfortunately, means that current continuously flows out of the LT1226 and thus it gets hot. A heatsink has been added to cool it.

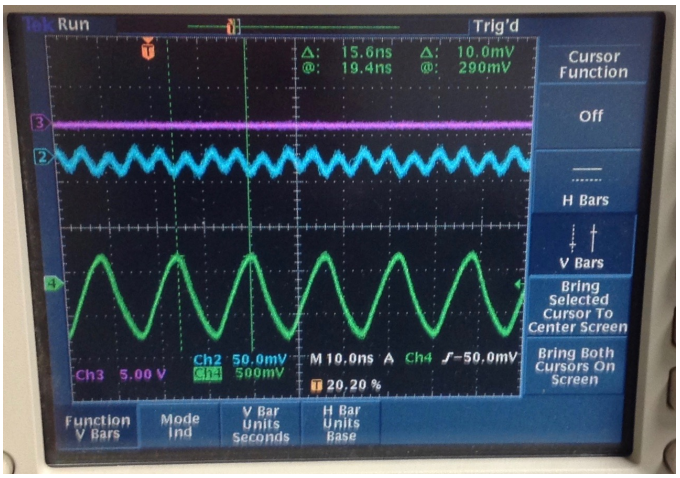

FIG. 7. The green trace is the oscillogram at the output of the LT1226 when the inputs of the opamp are grounded. It self oscillates at 64 MHz.

C. Results

We have set up the oscilloscope to measure the voltages across the test points TPA and TPB shown in Fig. 6. We chose these test points because the current I_v flowing through both the 100 Ω variable resistor and the fixed 10 Ω resistor is given by

$$I_v = V_{\mathrm{TPB}}/R_{10} = V_{\mathrm{TPB}}/(10[\Omega]) \tag{20}$$

where V_{TPB} is the voltage across the 10 Ω resistor R_{10}. Therefore, if the current feedback loop works, the voltage across TPB and ground will remain unchanged while the voltage aross TPA will change when we change the 100 Ω variable resistor. This is in contrast to the case when the feedback loop does not work — in this case, we expect the voltage across TPB and ground will change because of Ohm's law.

In all the following measurements, V^+ is from a signal generator that has been set to produce a pulse with a width of 100 μs that repeats at 15 Hz.

1. *Current regulation with load variations*

We show how I_v varies as a function of the total load resistance R_s which is made up of the 100 Ω variable resistor in series with the fixed 10 Ω resistor in Fig. 9. It is clear that current feedback loop works. (Well, at least for low voltages.)

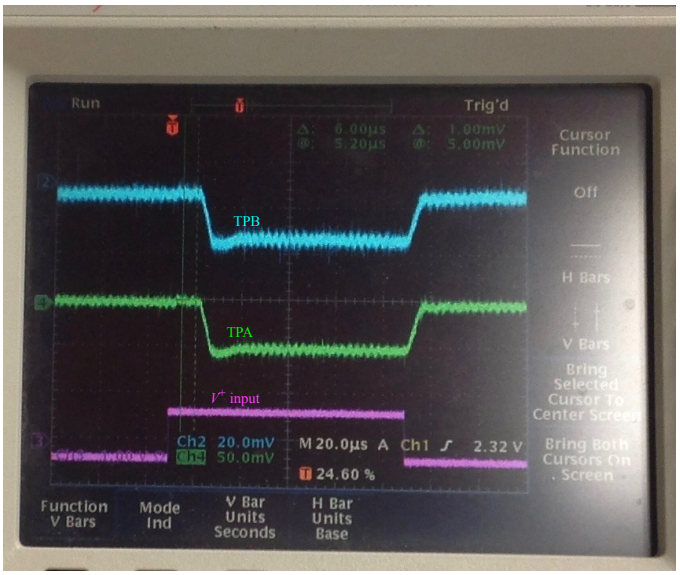

FIG. 8. This is the oscillogram at various points of the feedback loop. TPA is the test point across both the 100 Ω variable resistor and the fixed 10 Ω resistor. TPB is only across the fixed 10 Ω resistor. V^+ is the user input into the feedback loop. There are small ripples on both test point signals. These ripples can be traced to the OP27 self oscillating.

The change in the regulated current I_v through R_s when the user changes V^+ is shown in Fig. 10. There is a current offset in the circuit because when $V^+ = 0$, $I_v \neq 0$. If we really need to correct this offset, we can add an adjustment pot to the final circuit. The linear fit to the data is

$$I_v(V^+) = (-0.49 \pm 0.02) + (-1.99 \pm 0.01)V^+ \tag{21}$$

The slope from the fit above can be compared to the theoretical slope given by Eq. 19 which is

$$\text{Theoretical slope} = -\left(\frac{1}{R_p} + \frac{1}{Z_p}\right) = -\frac{2}{10^3[\Omega]}\ \text{A/V} = -2\ \text{mA/V} \tag{22}$$

where we have put in the negative sign by hand because I_v flows from ground back to the current source, and both $R_p = Z_p = 1$ kΩ in our low current test circuit. Therefore, we have found that our theory matches with experiment to within measurement error.

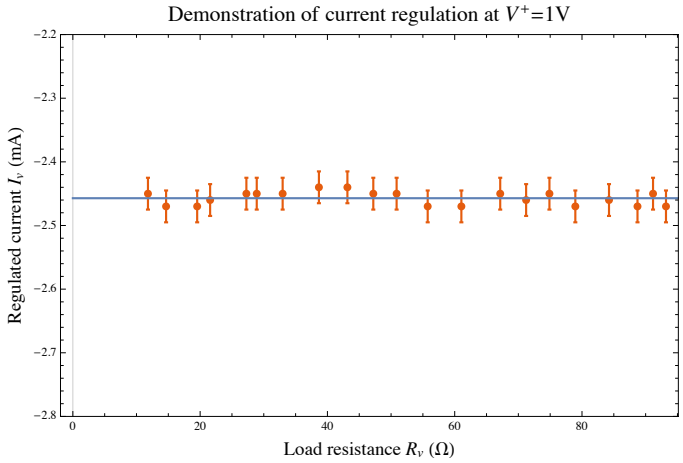

FIG. 9. This shows that current I_v is independent of the load resistance R_s which is made up of the 100 Ω variable resistor in series with the fixed 10 Ω resistor. The mean current for the entire range of R_s is (-2.46 ± 0.01) mA.

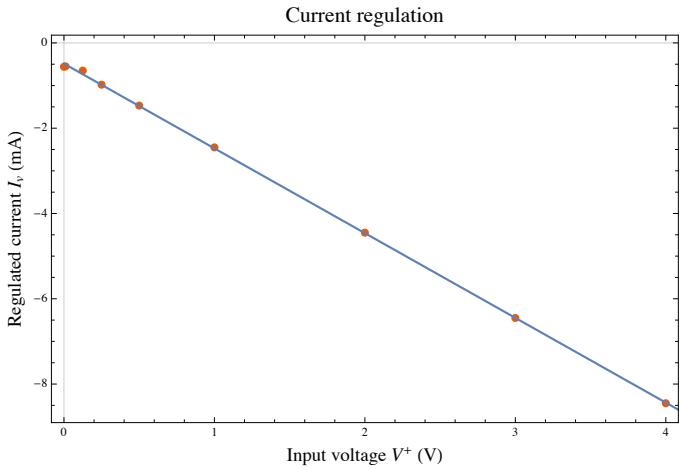

FIG. 10. The regulated current going through R_s is shown here. There is a current offset in the circuit. The offset can be removed with an adjustment of the "offset" pot in the final circuit.

2. Rise, fall times

The rise and fall times are between 7 to 8 μs. The measurements are shown in Fig. 11.

D. High current implementation and test

The high current implementation of the feedback loop is shown in Fig. 12. It is a modification of the low current circuit shown in Fig. 6. The main changes between them are:

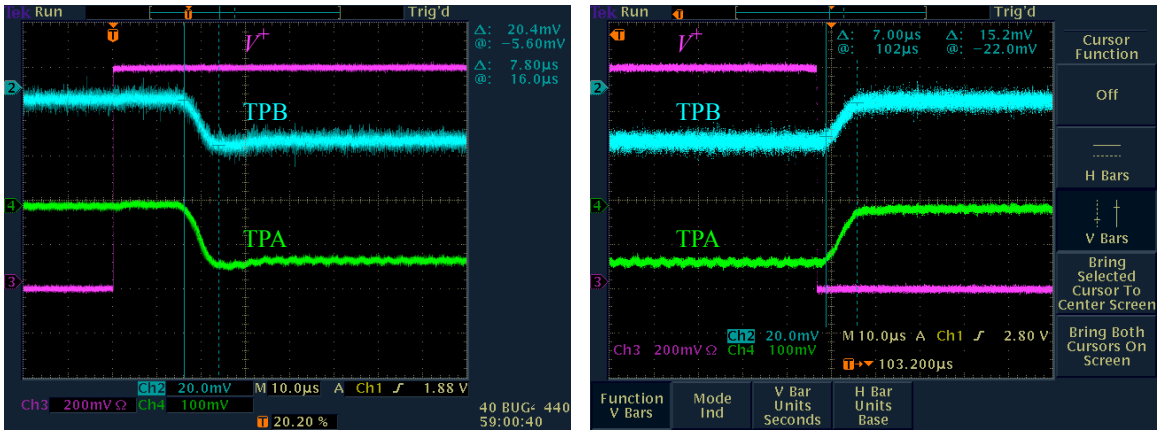

FIG. 11. The measured rise and fall times for the low current test circuit measured at TPA an TPB.

- R_p is a fixed resistor that we have replaced from 0.1 Ω to 1 kΩ so that different currents through R_s can be tested.
- R_s is a fixed resistor that we have replaced from 1 Ω to 100 Ω so that different loads can be tested.
- Replacement of the OP27 with another LT1226. Empirical studies show that with wires connecting the gate and collector of the IGBT and then back to the low current loop, the voltage across R_s has large oscillations. Replacing the OP27 with the LT1226 remedies this problem.
- The 15 V, 3 A power supply has been replaced with a 20 V, 10 A (TDK-Lambda ZUP20-10) power supply.
- All wires that carry high current have been replaced with heavy gauge wires.

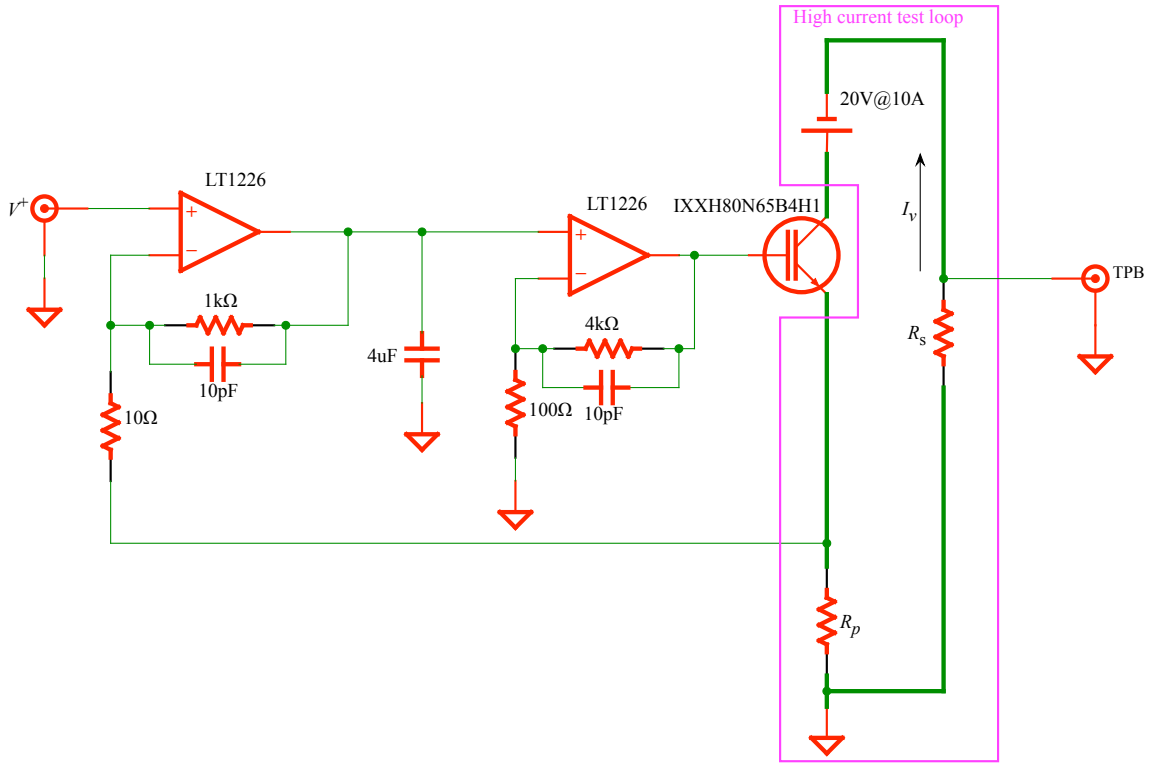

FIG. 12. This is the high current circuit used to test the basic feedback loop. The main differences are: (a) The downstream OP27 has been replaced with a LT1226 (b) fixed R_p resistors that range between 0.1 Ω to 1 kΩ (c) the floating supply has been replaced with a 20 V, 10 A supply (d) the variable resistor has been removed and replaced with fixed R_s resistors that range between 1 Ω to 100 Ω (d) heavier gauge wire has replaced the lower gauge wires (highlighted with dark green traces).

1. *Jitter*

FIG. 13. When the rise time of the signal generator is below 10 ns, the current pulse jitters (green trace). This jitter disappears when the rising edge is > 10 ns. The magenta trace is the sync pulse.

We found that there is a jitter in the falling edge of I_v in high current mode w.r.t. the rising edge of V^+, that can be as large as 14 μs. See Fig. 13. We found that the solution to this problem is to slow down the rising edge of V^+. When the rise time > 10 ns, the jitter disappears. For the rest of our tests, we have the rise time of V^+ greater than or equal to 100 ns.

E. 10 A test

We have set $R_p = 0.1\ \Omega$ (as marked on the resistor) and $R_s = 1\ \Omega$ in this test. This means that when $V^+ = 1$ V, there should be 10 A flowing across R_s. However, from the results of the measurement shown in Fig. 14, we found that when $V^+ = 2$ V, we see 10 A flowing across R_s. We can account for this factor of 2 from both the uncertainty of R_p and the wires that connect it to the feedback circuit. This means that, for $V^+ = 2$ V to give $I_v = 10$ A, we must have $R_p = 0.2\ \Omega$ from Eq. 19 because $I_f = 1\text{ mA} \ll I_v = 10$ A.

1. *Noise level*

The noise level measured within the pulse shown in Fig. 15(a) shows that it is < 50 mA for $I_v = 10$ A. This should be compared to the noise that is seen in the background picked

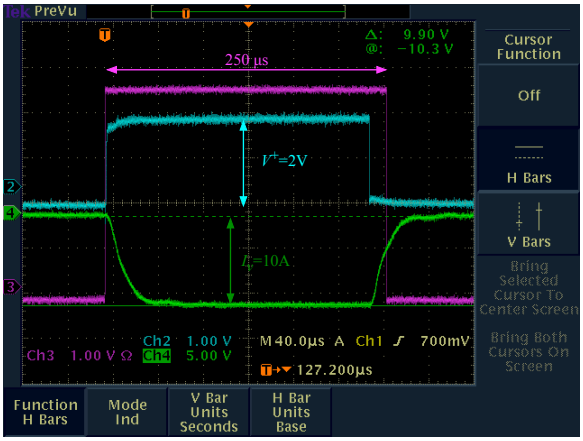

FIG. 14. The measured current through R_s is 10 A when the peak of $V^+ = 2$ V. The magenta trace is the sync pulse.

up by the oscilloscope shown in Fig. 15(b). The spikes are visible in both traces regardless of whether the circuit is powered. Therefore we will ignore the spikes and thus, in the worst case, the fraction of noise in the 10 A pulse is $0.05/10 = 0.5\%$ which meets our requirement shown in Table I.

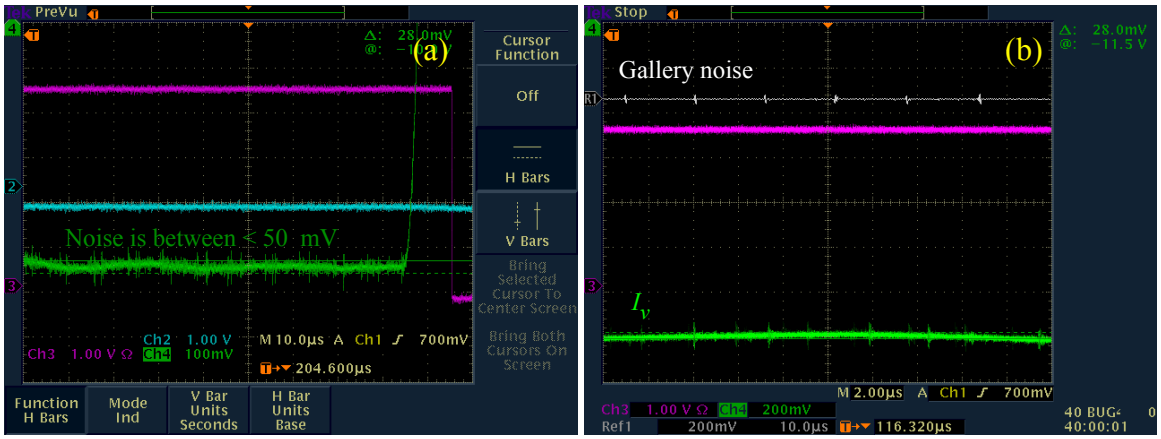

FIG. 15. (a) We zoomed the oscillogram shown in Fig. 14. The noise level is < 50 mV. The magenta trace is the sync pulse. (b) Noise is picked up by the oscilloscope when the circuit is turned off but with the signal generator turned on. The spikes in the reference come from the Linac gallery.

2. *Ripples*

There are also ripples at the falling edge of I_v shown in Fig. 16. We have found empirically that these ripples come from the inductance of R_p. For the final implementation, these ripples still exist because we did not find good replacements for these wire-wound resistors that have both low resistance and high power ratings.

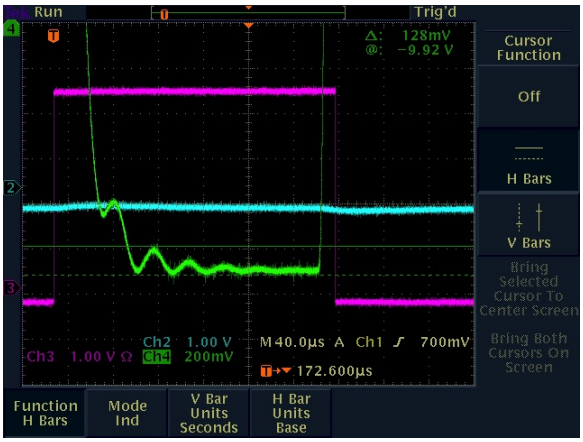

FIG. 16. The ripples at the start of of I_v (green trace) has been traced to the inductance of R_p. The magenta trace is the sync pulse.

3. *Fall and rise time*

The fall time with V^+ having a rise and fall time of 100 ns and $I_v = 10$ mA is shown in Fig. 17(a) and (b). The measured fall time of ~ 35 μs is much longer than the 7 μs to 8 μs what we found in the low current test that was discussed in section IV C 2. It is probably long wiring causing this because after we mounted the feedback circuit into a box and shortened most of the wiring, the rise and fall times came back to ~ 10 μs. See section V B. We made the 1 Ω load by wiring four 4 Ω high wattage resistors together in parallel shown in Fig. 17(c).

4. *Delay*

There is a delay of about 4 μs between the start of V^+ and the start of I_v. This delay is shown in Fig. 18.

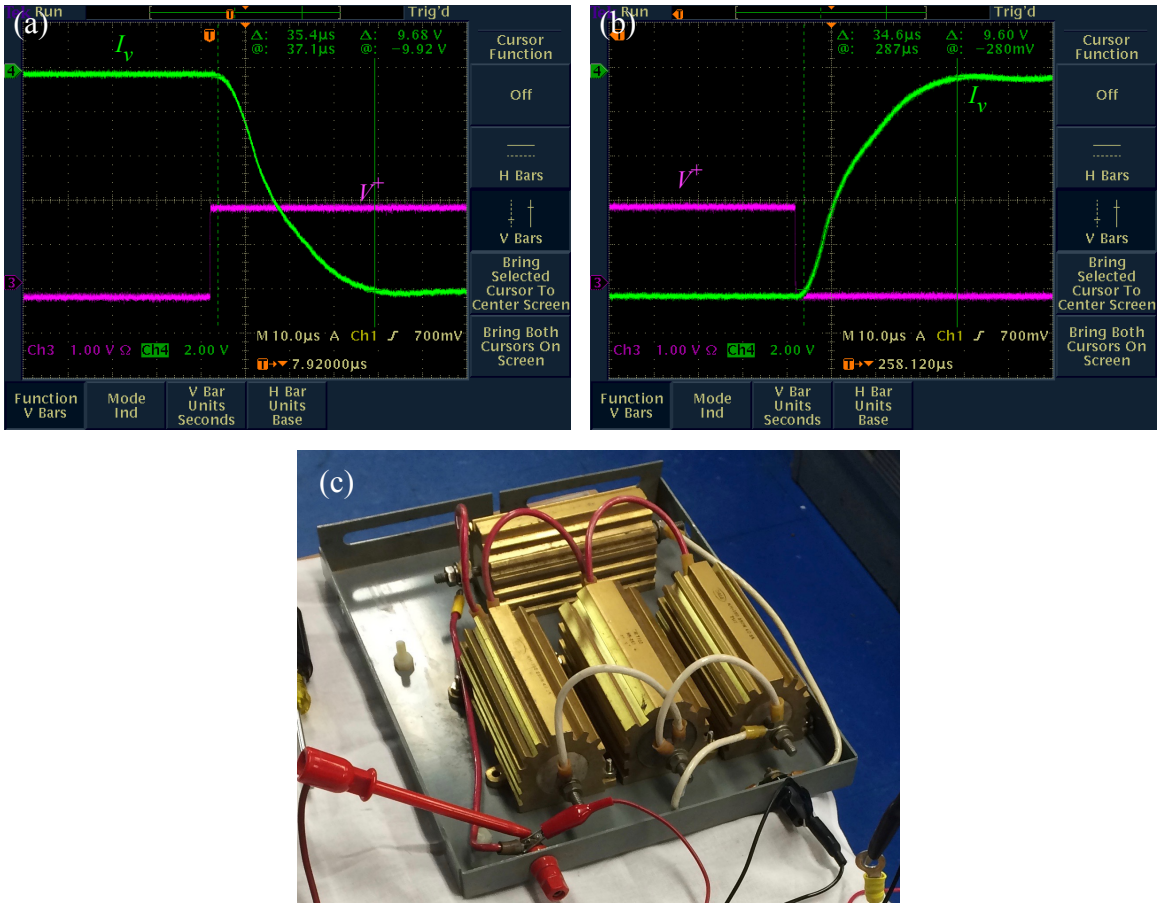

FIG. 17. The fall time for $I_v = 10$ A is about 35 μs (a) and the rise time ise also about 35 μs (b) going into a resistive load made up of four 4 Ω high wattage resistors in parallel (c).

V. MODIFICATIONS AFTER BOXING

We have installed the current feedback circuit in a box is shown in Fig. 19. There are some construction details that we have changed from the high current circuit that was discussed in section IV D. We have found that a simple transplant of the high current circuit board did not reproduce our high current test results!

We have found that I_v had periodic spikes that varied in both frequency and amplitude as V^+ and the voltage of the high voltage power supply are changed. Furthermore, the characteristic of these spikes depended on how the components are wired and mounted! The white trace in Fig. 20(a) shows I_v before the fix. Although not shown here, the amplitude of these spikes can grow as large as the desired I_v pulse simply by changing how the leads of the high voltage power supply and the IGBT are connected to the power filter circuit

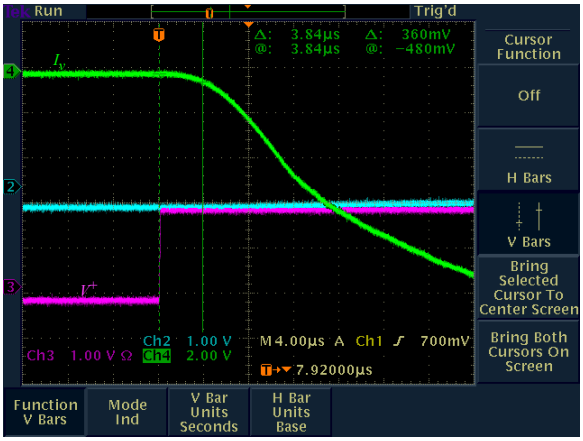

FIG. 18. The delay between the start of V^+ to the start of I_v is about 4 μs.

shown in Fig. 19(d). The spikes also show up when the IGBT is bolted to the case. This observation implies that there is capacitive coupling between the IGBT and ground. We have cured this coupling problem by mounting the IGBT on a ceramic standoff. When we do this, the case no longer functions as the heatsink for the IGBT, and so we have to use a fan cooled heat sink instead. The IGBT with its fan cooled heatsink is shown in Fig. 19(c).

A. Curing the I_v spikes

We have found from trial and error that the cure for the I_v spikes are as follows:

1. Mounting the IGBT away from the case backplane.

2. Increasing R_p from 0.1 Ω to 0.2 Ω.

3. Addition of long wires that series connect two 0.1 Ω resistors that form R_p together and to ground.

The remounting of the IGBT has already been discussed in the previous section and will not be repeated here.

The increase of R_p from 0.1 Ω to 0.2 Ω seems to reduce the size of the I_v spikes. The scaling that we have found in section IV E does not change with the increase of R_p — it is still -5 A/V. We attribute this result to the adding back of the resistance from the reduction of wires lengths used in the high current test.

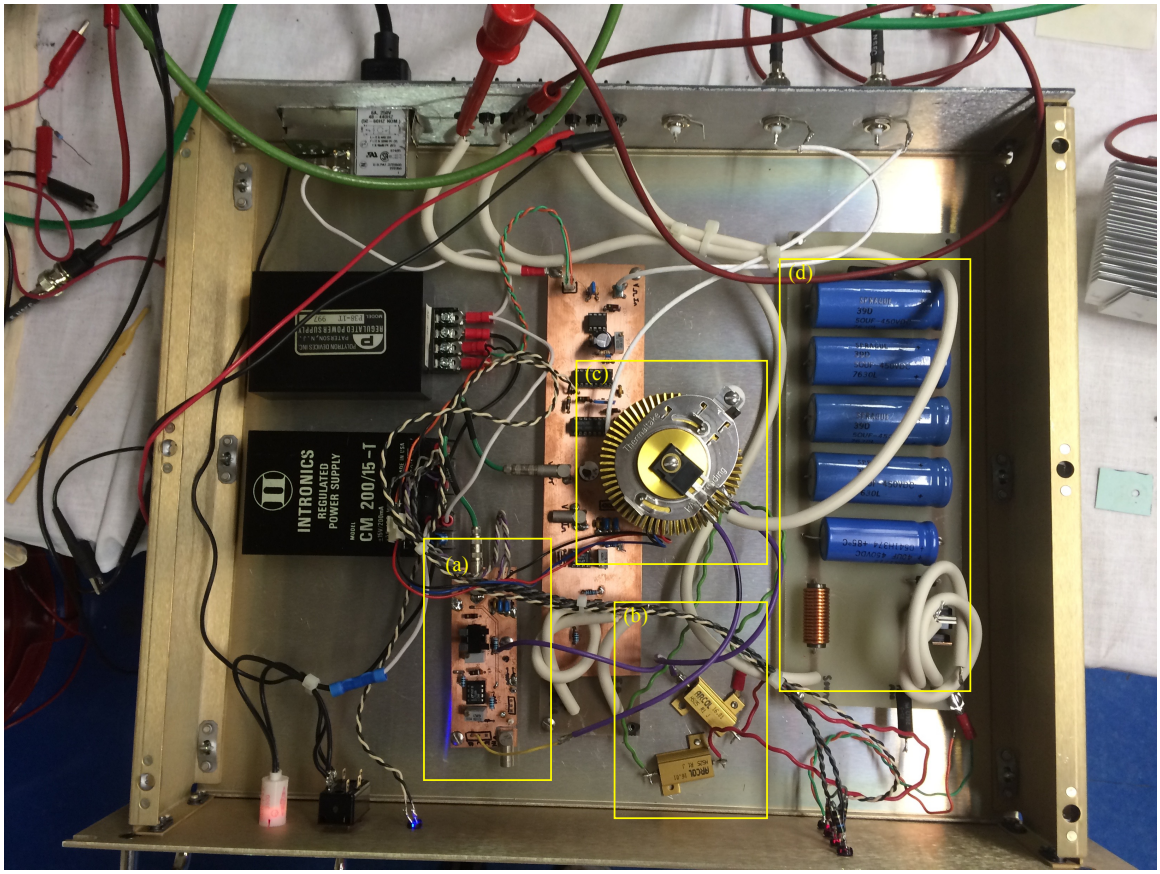

FIG. 19. (a) The feedback circuit mounted in a box. (b) R_p has been increased from 0.1 Ω to 0.2 Ω. Notice the length of the wires connecting the two resistors (red) and the wire that connects R_p to ground (green). (See also Fig. 20(a)). The reason for these long wires will be discussed in section V A. (c) The IGBT is mounted on ceramic standoff together with a heatsink with cooling fan. Originally, the IGBT was bolted to the case but this caused ringing in the feedback circuit. (d) The power filter circuit consists of 5 capacitors wired in parallel to give 450 μF and is series connected to a 4.9 μH inductor. The circuit diagram is shown in Fig. 22.

The third cure is a lot more mysterious. We have found that the spikes in I_v will go away when we use long lengths of wire (2 pieces of wire that are 6" each) that connect the 0.1 Ω in series and to ground. The only explanation we have at this time is that the wires have enough inductance to change the resonance of the LT1226. However, the inductance of 12" wire is only $\sim$300 nH, and thus, in our opinion, this is an unlikely explanation. But we'll live with not knowing exactly why for now.

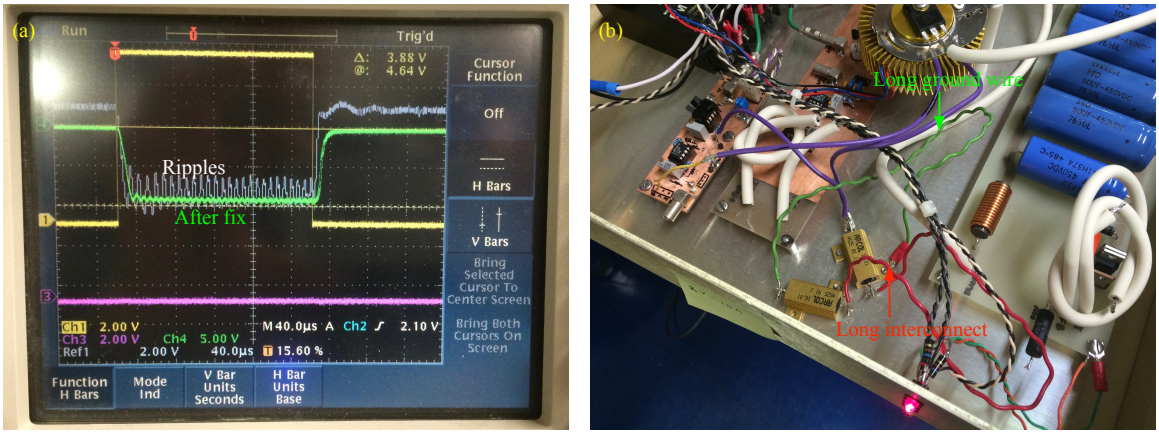

FIG. 20. (a) This is the oscillogram that shows the "before" and "after" applying the cures to fix the ripples. (b) R_p has been increased to 0.2 Ω form 0.1 Ω and long wires (6" each), have been used to connect the 0.1 Ω resistors in series and to ground. The circuit diagram is shown in Fig. 22.

B. Bench test results after boxing

Figure 21 summarizes all the measurements that have been done after boxing and testing on the bench with the load $R_s = 1\ \Omega$. The rise and fall times are about $\sim$11.4 μs, and the delay w.r.t. trigger is $\sim$1.6 μs. These numbers are similar to the numbers we have found with the low current test (section IV C) while the rise and fall times, and delay have been improved by a factor of 3 from the high current tests. Unfortunately, the ripple in I_v is now 7% at 10 A rather than 0.5% found in the high current test which means that we do not meet specifications here. We believe that the cure is to replace the wire wound resistors used to make up R_p with other types of resistors. We will do this when we can find good replacements.

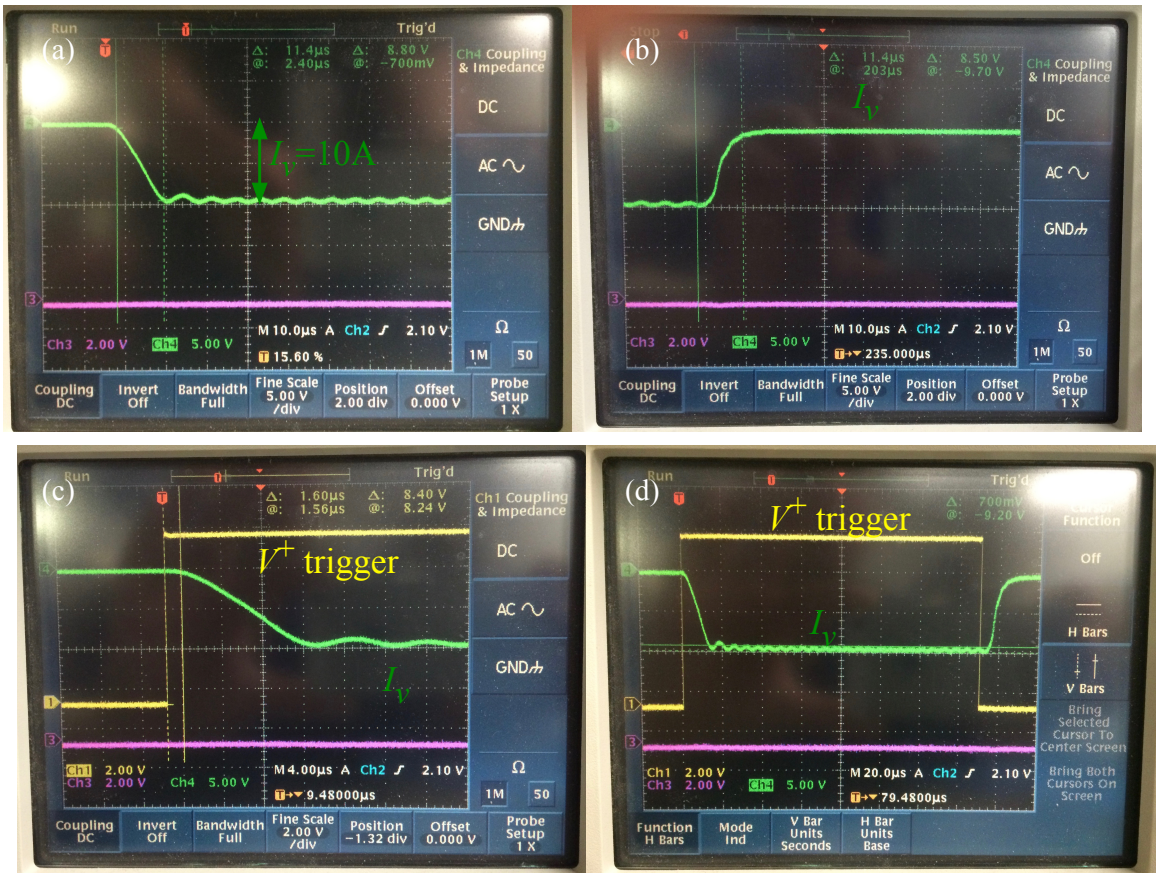

FIG. 21. (a) The fall time for $I_v = 10$ A is about 11.4 μs and (b) the rise time ise also about 11.4 μs. (c) The delay of the I_v from the V^+ trigger is about 1.6 μs. (d) The ripple amplitude is 0.7 V which translates to about 7% of the I_v amplitude.

VI. H- SOURCE TEST

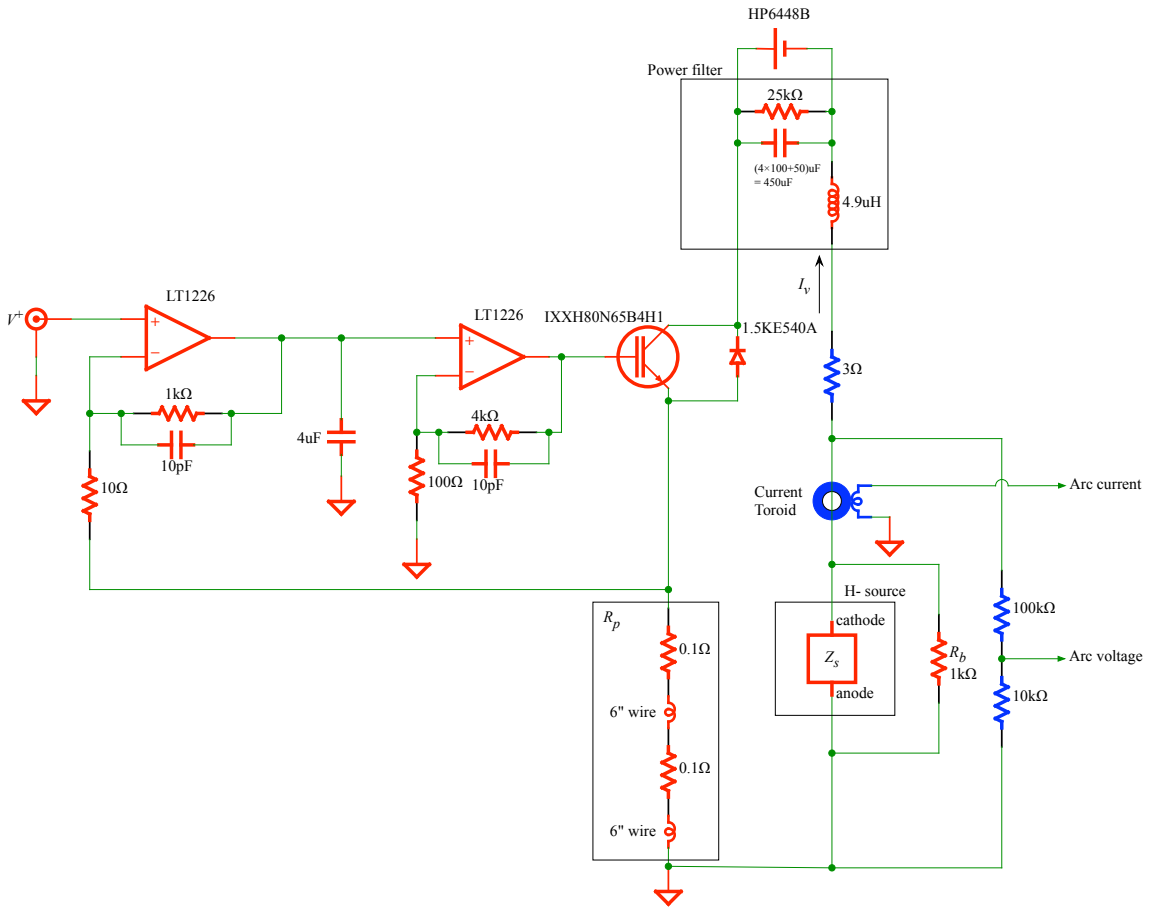

FIG. 22. This is the current feedback loop that is connected to the H- source for the performance test. The components that are drawn in blue are parts of the diagnostics of the H- source. The 6" wires used in R_p have been added to suppress I_v spikes. R_s is now Z_s because the source impedance can be both resistive and reactive. A transient voltage suppressor diode has been wired across the emitter and the collector of the LGBT. A bypass resistor, $R_b = 1$ kΩ has been wired across Z_s. The high voltage power supply is a HP6448B [5] that is specified to be able to output 600 V@1.5 A.

The H- source test circuit is shown in Fig. 22 where the feedback loop is connected to the H- source. The components drawn in blue are the parts of the diagnostics of the H- source. In this circuit, $R_s \rightarrow Z_s$ because the source impedance can be both resistive and reactive. A transient voltage suppressor diode [6] has been wired across the emitter and collector of the IGBT so as to protect the IGBT from sparks. A bypass resistor $R_b = 1$ kΩ, 2 W resistor

is wired across Z_s because when the H- source is first started, there is no plasma, and thus $Z_s = \infty$, i.e. open. The feedback loop cannot regulate with an "open" load and thus the R_b resistor temporary acts as the load. The action of the R_b load is discussed below. Note: Later tests with the H- source showed that R_b is unnecessary. See section VI D.

A. Input trigger tweaks

We found in this test with the control system's trigger pulse connected to V^+ that the IGBT is always "on" regardless of whether the trigger is on or off. We traced this problem to the residual 24 mV that the trigger circuit outputs even though it is in its "off" state. This voltage offset is enough, after going through 2 opamp stages, in the feedback loop to turn on the IGBT. The solution that we use is the addition of an opamp offset voltage adjustor that corrects the DC offset of the input trigger. We can then tweak this adjustable voltage to -24 mV to stop the IGBT from turning on when the trigger pulse is off. The circuit is shown in Appendix A.

B. R_b bypass resistor

When the H- source starts up, there is no plasma and thus $Z_s = \infty$, i.e. open. Since, Z_s is open, the current loop does not operate and the voltage across Z_s is identically zero. Herein, lies the chicken and the egg problem because for the source to start, the voltage across Z_s must be greater than 250 V. Our trick for solving this conundrum is to add a bypass resistor, $R_b = 1$ kΩ, in parallel with Z_s. When V^+ is pulsed to 2 V, i.e. we have set the current through the R_b resistor to 10 A pulsed, which is impossible because the required voltage across it must be 10 kV $\gg$ 300 V that the high voltage power supply is able to provide. Thus, although 10 kA is never reached, the voltage across R_b and Z_s is 300 V which is exactly what we want at start up.

Now, once the plasma starts, $|Z_s| \sim 10\ \Omega$, most of the current will now flow through Z_s instead of the R_b resistor because $|Z_s| \ll R_b$. Current regulation automatically starts without our intervention because the voltage required is $10\ \Omega \times 10$ A $= 100$ V < 300 V. This is what we want for normal H- source operations, i.e. the current through Z_s is now regulated.

1. *Power rating of the R_b resistor*

The maximum voltage that we have set on the high voltage power supply is 300 V and the duty factor 200 μs $\times$ 15 Hz and thus the maximum power through the resistor during source startup is

$$P_{\max} = \frac{300^2[\mathrm{V}^2]}{1[\mathrm{k}\Omega]} \times 200[\mu\mathrm{s}] \times 15[\mathrm{Hz}] = 0.27 \text{ W} \tag{23}$$

This means that the power rating of the R_b greater than the above value. We chose a 2 W resistor in our implementation to have a safety margin.

C. Test results with and without R_b

We will discuss the test results for the cases where we have R_b is used and disused. In the disused case, we also leave the voltage offset of 24 mV from the pulse trigger uncorrected so that there is always a potential difference at the high voltage supply voltage across Z_s. In all the tests below, the arc current and arc voltages are measured at the points shown in Fig. 22.

1. *R_b connected*

Figure 23 shows the both the arc current pulse, arc voltage pulse and the input trigger pulse when R_b is connected to the circuit and the 24 mV input offset is corrected. The arc current has been set to 15 A. From Fig. 23(a), we found that the arc current pulse is delayed by 51 μs after the trigger pulse (further experiments showed that this delays goes away with the arc current pulse getting wider after the source has conditioned and stabilized) and from Fig. 23(b), the arc voltage decays away slowly even when the arc current has gone to zero.

The delay from the start of the trigger is much longer than we had measured in section V and shown in Fig. 21(a). We found from later experiments (not in this configuration), that this delay can be adjusted using the offset circuit shown in Appendix A. The offset circuit is used to adjust the DC offset of the V^+ pulse. The arc current pulse increased in width and its falling width approached the rising edge of the trigger pulse. The rising edge remained at its original position. This indicates that the input pulse V^+ has a DC offset that prevents the current pulse from starting. See our test results in section VI D 1.

The long decay of the arc voltage after the arc current is apparently zero can be traced to the gas being pumped out. Even though the toroid shows that the arc current is zero, it probably is not and there is still a small amount of current flowing as the gas is being pumped out. This explanation will have to be tested later.

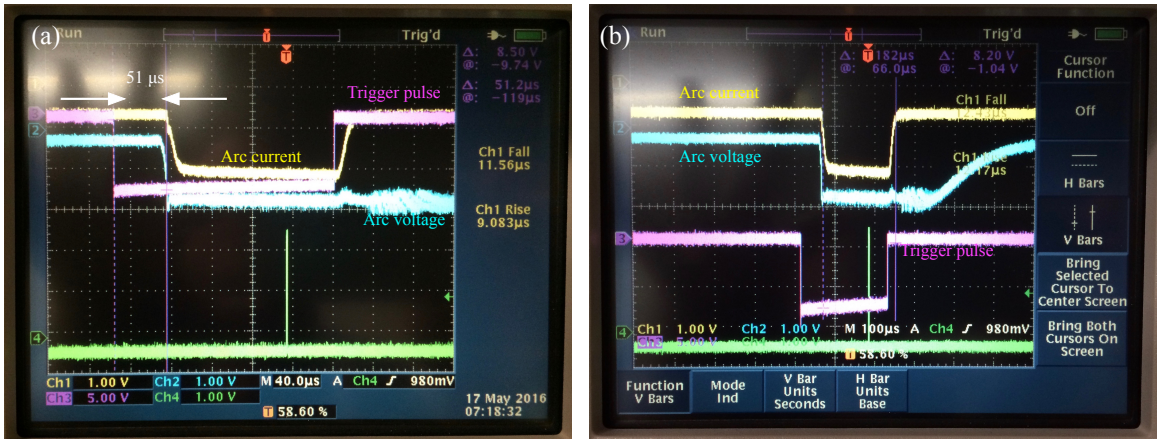

FIG. 23. (a) The arc current pulse is delayed by about 51 μs from the start of the trigger pulse (See text). (b) The arc voltage does not turn off immediately even though the arc current apparently has gone to zero.

The performance of this setup can be seen in Fig. 24. On our first inspection, it looks like the current regulation is not working well. Sometimes after a spark the arc current jumps to a larger value. We believe the problem is with the bypass resistor R_b. This is a carbon resistor and whenever there is a spark, its value is slightly reduced. And from where the arc current is measured (shown in Fig. 22), a larger current will have to flow to compensate.

2. R_b disconnected

We decided from the previous test with R_b, that it would better to leave it out. Since R_b is left out, we have to also remove the 24 mV offset circuit as well so that on startup the arc voltage is not zero. We have set the high voltage power supply to 300 V and thus the potential difference across Z_s is 300 V at source start up.

Figure 25 shows both the arc current pulse and the arc voltage. The arc current is regulated by the current feedback loop and has been set to 15 A.

Figure 25(a) shows that there is a prepulse after the gas valve is opened (magenta curve).

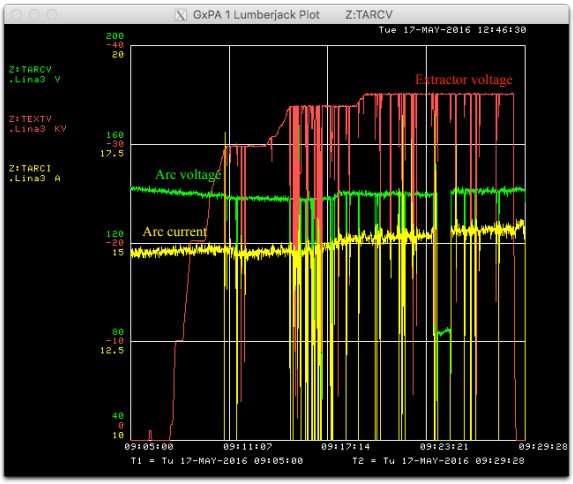

FIG. 24. This shows the behaviour of the arc current and voltage during the performance test. An indication of a spark is when the extractor voltage suddenly drops to near zero. The arc current seems to increase after some sparks.

The size of this prepulse can be adjusted with gas pressure. Once, there is sufficient ionization of the gas, the arc voltage climbs and there is probably a very small amount of arc current at this point. The trigger pulse then turns on and the arc current is regulated by the loop. The slope that is seen here goes away as the source warms up and the gas pressure adjusted. After the trigger pulse goes to zero, the arc current apparently goes to zero as well, but the arc voltage slowly decays away. The non-zero arc voltage at this time indicates that the gas is not completely pumped out. This is reminescent of the long decay time of the arc voltage that we had found in section VI C 1.

Figure 25(b) is the zoomed in view of (a). Although not shown here, the arc current pulse that we measure here does not have a long delay w.r.t. the input trigger pulse. This is different from what we had measured in section VI C 1 where the delay is 51 μs. The width of the pulse is 224 μs which is also the width of the input trigger pulse.

Figures 25(c) and (d) show the fall time (~ 14 μs) and the rise time (~ 13 μs) of the arc current pulse. These times are about the same as the rise and fall times that we had measured in section V B.

The behaviour of the arc current as a function of time is shown in Fig. 26. We can see that the arc current remains mostly constant even as the arc voltage makes large excursions. However, although V^+ has been set to regulate the arc current to 15 A when we start the

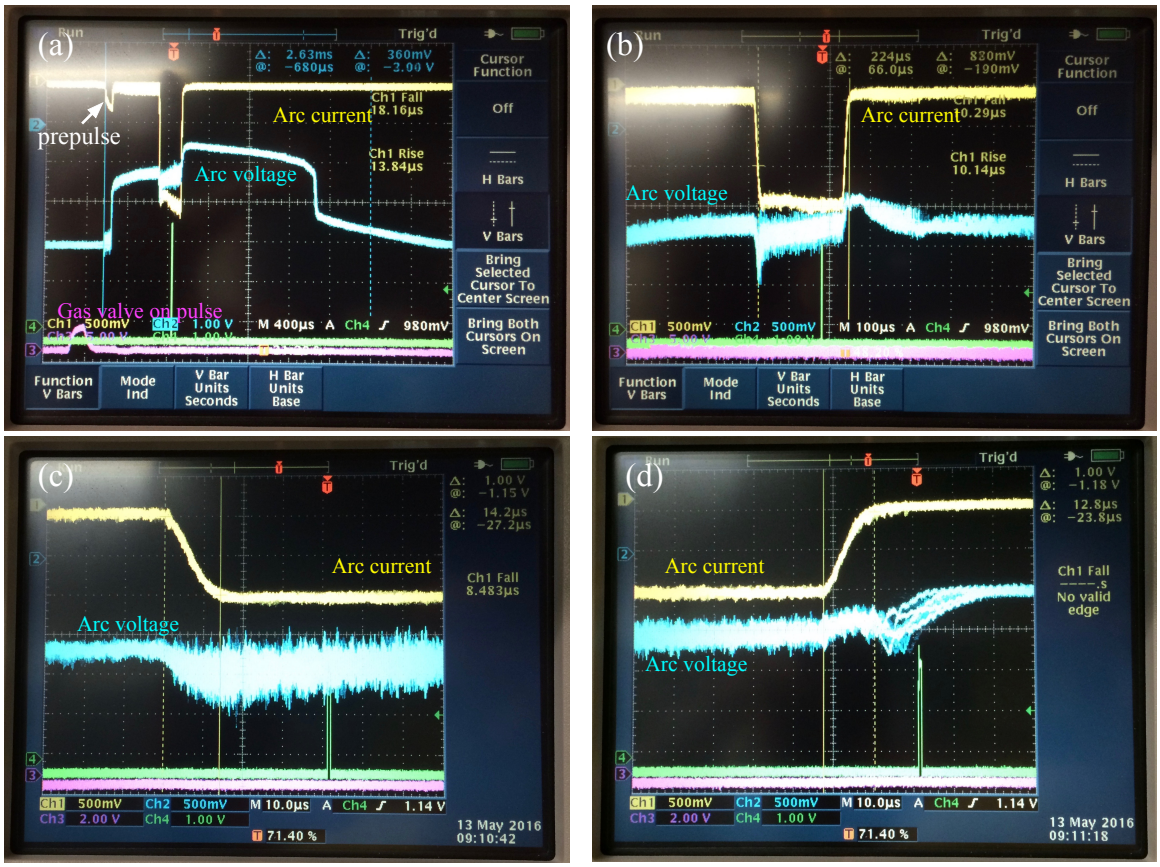

FIG. 25. (a) There is prepulse after the gas is let into the source. The arc voltage turns on after the gas is ionized and decays away after the arc current pulse apparently goes to zero. The long decay comes from the gas being pumped out.

source, the loop does not seem to be working because both the arc current and voltage track. But once the source stabilizes, current regulation works well.

D. Not quite final Improvements

We found from empirical studies that R_b is not necessary and there is sufficient voltage across the source during startup that the arc can start up without it. Therefore, R_b has been removed from the circuit.

During our studies, we found that even though V^+ is zero outside the voltage pulse, the arc voltage is only zero for a few ms before settling to the maximum high voltage output of 300 V. During this time the arc current I_v is essentially zero. We can trace the problem back to the feedback circuit which is attempting to regulate current through $Z_s \approx \infty$ during

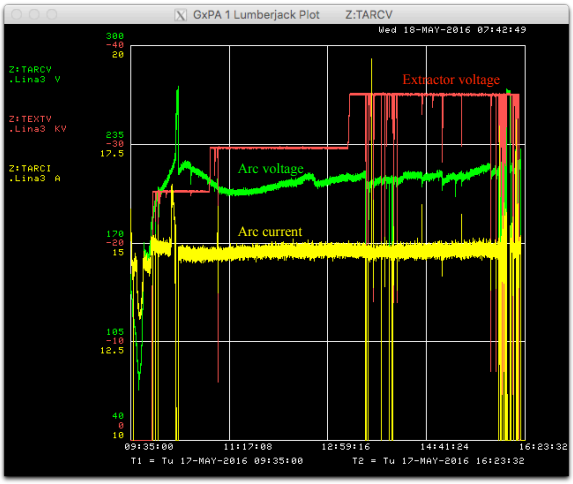

FIG. 26. This shows the behaviour of the arc current and voltage during the performance test. An indication of a spark is when the extractor voltage suddenly drops to near zero. The arc current stays nearly constant during arc voltage excursions. There is, however, some weird arc current excursions when we start the source.

this time. This happens even though V^+ is supposedly zero. We can see from Ohm's Law that if the "required" current, I_v, is small but not zero, then

$$I_v = V_v/Z_s(\sim \infty) \tag{24}$$

where V_v, the voltage across Z_s, must approach infinity as well. This is why the arc voltage rails to the maximum high voltage supply voltage.

The solution that we have found for the above problem is to introduce a MOSFET, FQP30N06L [7], to act as a switch into our feedback circuit. See Fig. 27 . A TTL gate pulse (that has to be buffered with a TTL to MOSFET driver SN75372 [8]) only allows the feedback current into the opamp when $V^+ \neq 0$. We can see that when $V^+ = 0$ and with the MOSFET switch open, the output of the the opamp is zero and thus $I_v \equiv 0$. And hence $V_v = 0$, i.e. the arc voltage is zero that we require.

Also during our studies, we found that the IGBT would sometimes short circuit during start up of the source. We think that the problem is that during start up Z_s can go to zero. This means that $I_v \approx 300[\text{V}]/3[\Omega] = 100$ A (see Fig. 27) which is higher than the current rating of 80 A for the IGBT IXXH80N65B4H1. We replaced it with a higher current MOSFET for operations. Our current choice is the IXFN120N65X2 [9] which has a 108 A current rating. However, this rating is at 25°C. If the MOSFET gets hot and gets to

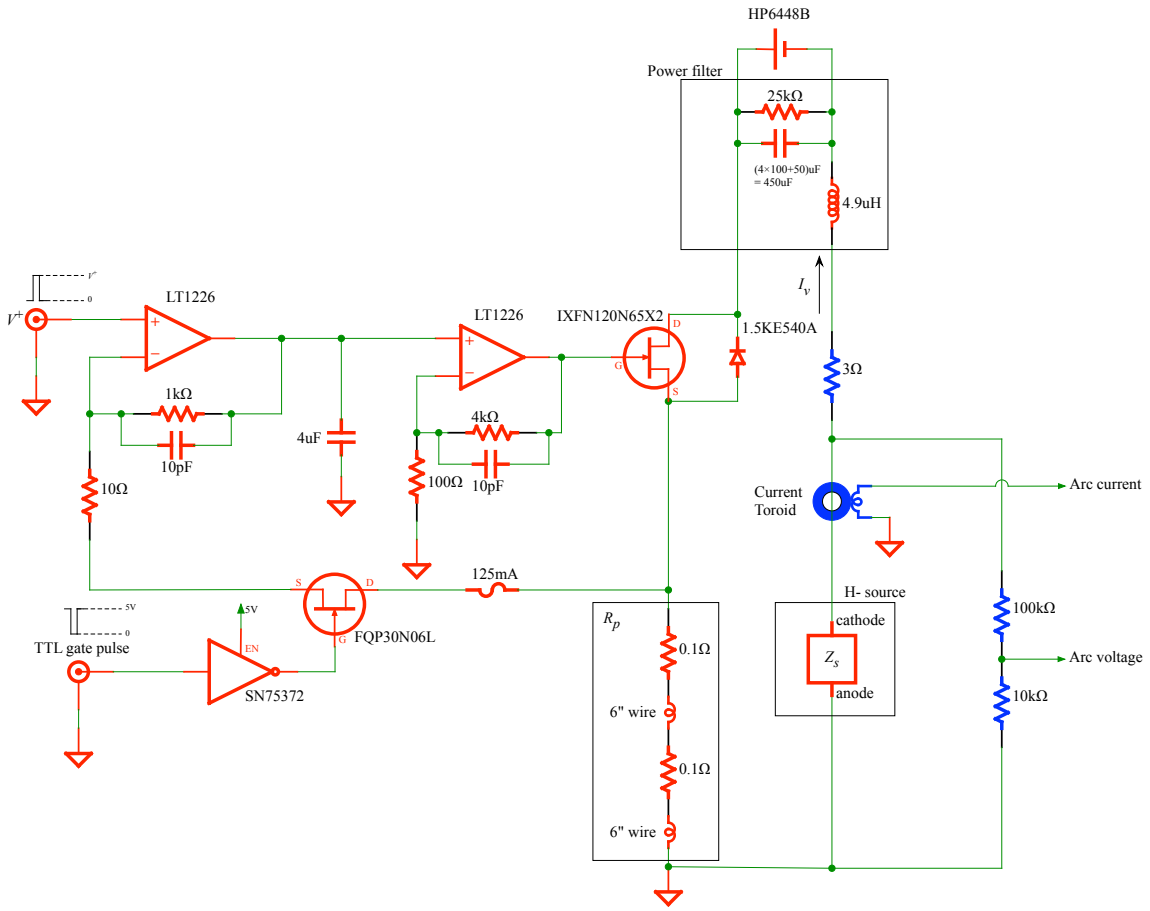

FIG. 27. We added a TTL gate to drive a MOSFET in the feedback loop to ensure that outside the V^+ pulse there is no arc voltage. We also replaced the IGBT with a MOSFET IXFN120N65X2. R_b has been removed. A 125 mA fuse has been added to the feedback loop to protect the low current components in case of castrophic failure of components in both the transition and high current sections of the circuit.

$>$ 100°C, its current carrying capability can be derated by as much 50%. Therefore, good cooling of the MOSFET is essential.

There was a catastrophic failure of the regulator when one of the 0.1 Ω resistors opened up during testing. This caused the high current to find a path to ground via the low current circuit. The high current destroyed every active component in this part of the circuit starting with the FQP30N06L to the last LT1226. In order to protect the low current circuit from future disasters, we added a 125 mA fuse into the feedback circuit.

The photograph of this design assembled into a box is shown in Fig. 28.

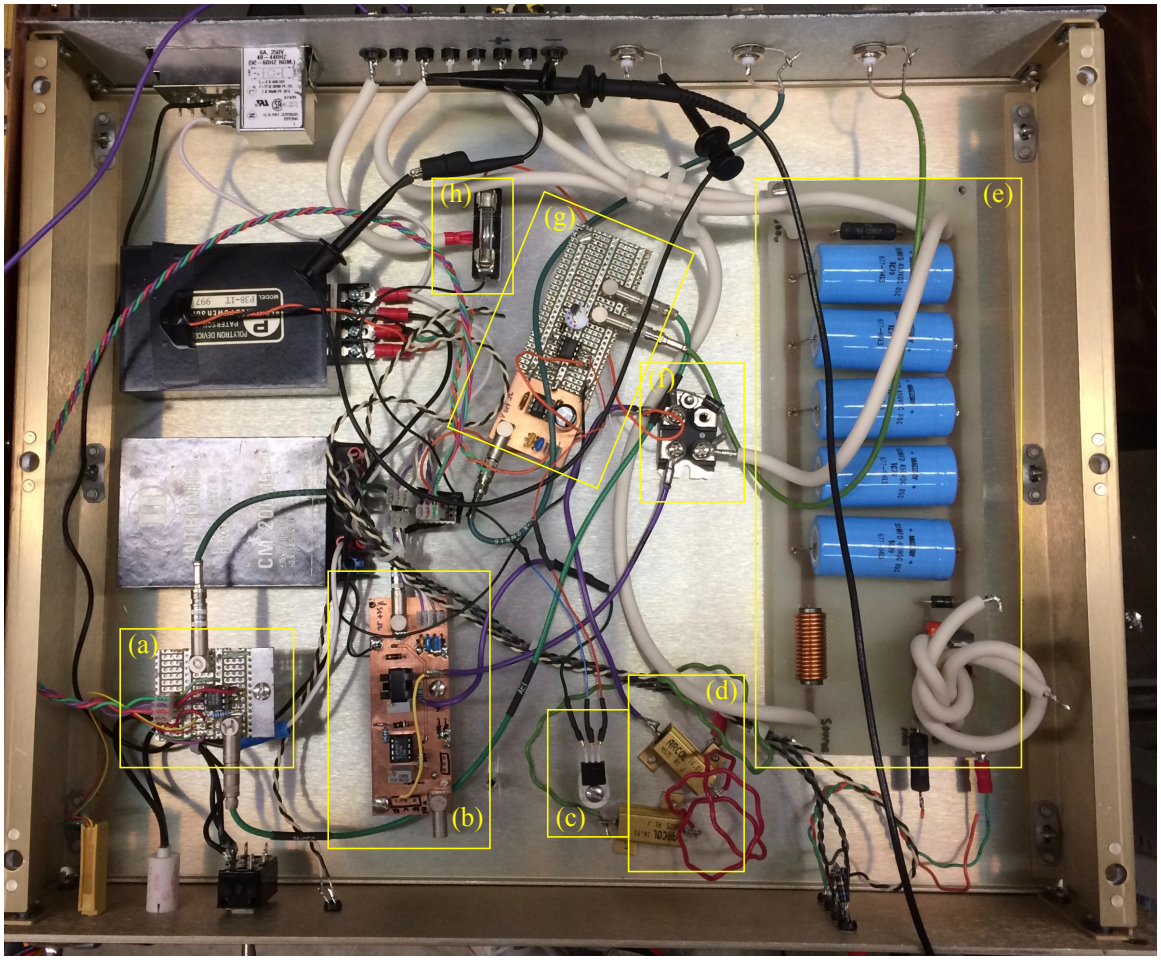

FIG. 28. Our "final" circuit is built in LEGO style. (a) The offset circuit that compensates for the 24 mV offset. See Appendix A. (b) The low current feedback part of the circuit. (c) The MOSFET switch FQP30N60L. (d) The two 0.1 Ω resistors that are in series and connected to the high current MOSFET and to ground. (e) Power supply filter. (f) The high current MOSFET IXFN120N65X2 and the transient suppression diode 1.5KE540A. (g) The trigger circuit that supplies V^+ and the gate pulse. (h) The 125 mA fuse.

1. *Performance*

The performance of this feedback configuration is shown in Fig. 29. We can see from Fig. 29(a) and (b) that the delay in the arc current pulse w.r.t. the trigger pulse improves from 43 μs to 6 μs after the V^+ DC offset is adjusted. Note: this delay was also observed earlier in section VI C 1. Both the rise and fall times of the arc current pulse are similar to those measured in the earlier sections. Therefore, the introduction of the MOSFET switch

into the feedback circuit does not affect its performance.

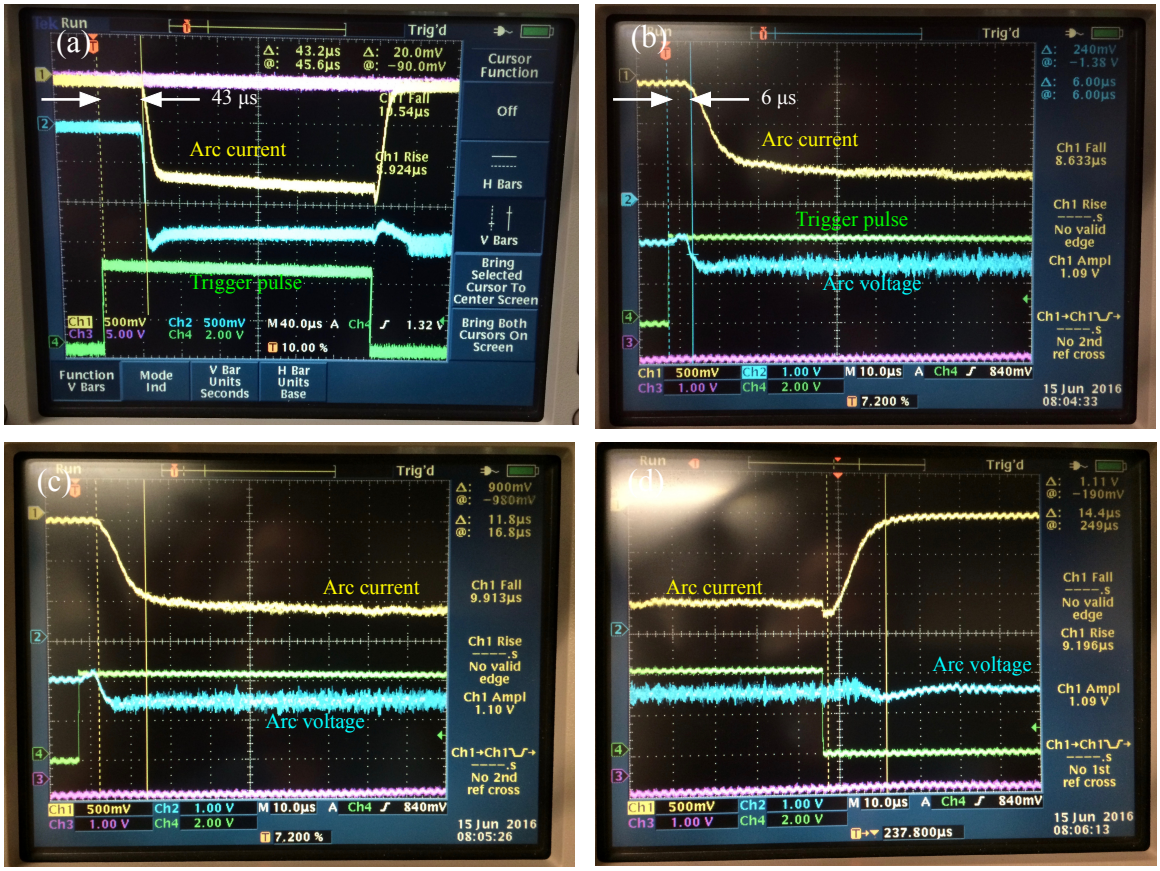

FIG. 29. (a) shows the delay of the arc current pulse during start up. It is about 43 μs w.r.t. the rising edge of the trigger (b) after adjusting the V^+ offset with the circuit shown in Appendix A, the delay is improved to 6 μs. (c) and (d) shows that the fall and rise time of the arc current is between 11 to 15 μs which is what we had measured earlier in our high voltage tests.

E. Final(?)

Unfortunately, we found that the MOSFET in the feedback loop kept dying after about 12 hours of operation. The MOSFET did not die from high voltage sparks because the extractor was off. Also high currents could not have been involved in its demise because the 125 mA did not blow. Rather than delve into the mysteries as to why it died, we decided to replace the MOSFET with a JFET switch, the DG191.[10] (This part is obsolete and will be replaced with a MAX319, CMOS analog switch[11] in final production). The circuit is shown in Fig. 30.

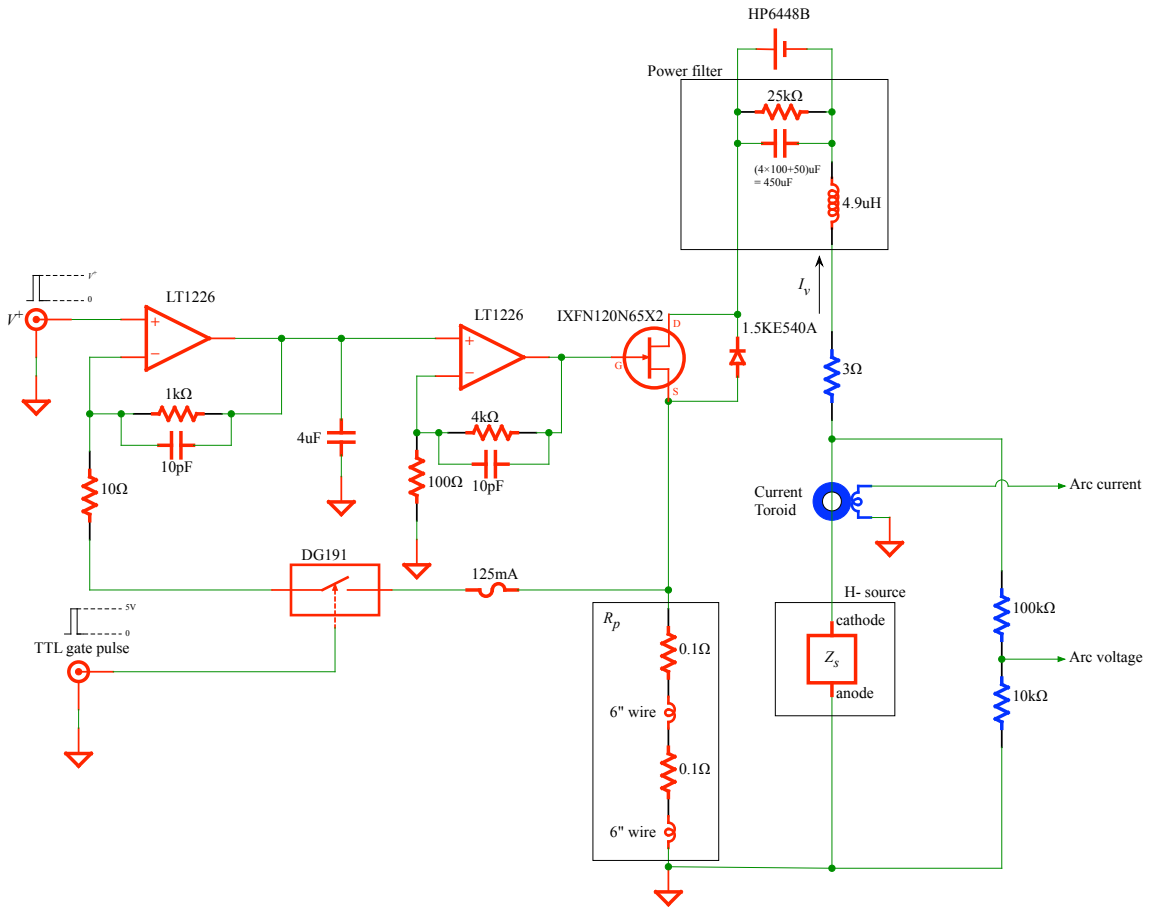

FIG. 30. The MOSFET in the feedback loop is removed because it kept dying. A JFET switch, DG191, is used instead.

1. *Performance*

The performance of the feedback loop and other monitored parameters are shown in Fig. 31. From the arc current shown in Fig. 31(a), we find that the regulation during periods of constant room temperature from 09 Jul 2016 23:56 hours to 10 Jul 2016 06:15 hours to be 15.34 ± 0.07 A, i.e. a regulation error of $\pm(< 0.5)\%$. However, although the data seems to show that that the arc current flucation correlates with the room temperature fluctuations, the results shown in 31(b) debunks this conclusion.

In Fig. 31(b), we changed the temperature of the room by 2.5°C, we found that there is a small drop in the arc current of about 0.1 A during this time. But this drop does not seem to be correlated with the temperature rise, especially since there is no corresponding rise when the room temperature is reduced. Therefore, at this time, we do not have an

explanation for the arc current fluctuation in Fig. 31(a).

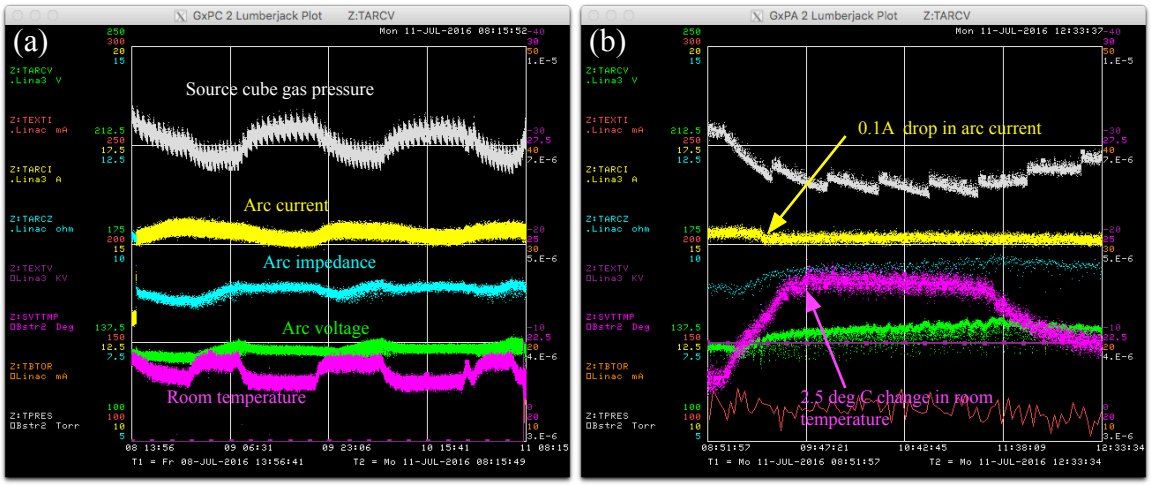

FIG. 31. (a) is the behaviour of the regulated arc current and other interesting parameters monitored over 3 days. It looks like the regulated arc current actually follows the temperature of the room but the results shown in (b) debunks this conclusion.

VII. CONCLUSION

Our current regulated feedback circuit for the arc modulator design has been tested and has been shown to work, although there are kludges that we have had to implement. The performance of the modulator will have to be tested on one of the operating sources to see if a current modulated arc modulator does, indeed, work "better" than a voltage regulated arc modulator.

VIII. ACKNOWLEDGEMENTS

We would like to thank the following people:

1. T. Len (BNL) for providing us with the design notes of their current regulated arc modulator.

2. A. Feld for building many versions of this circuit and his invaluable help in squashing noise that we found.

3. K. Koch for helping us modify the circuit during high voltage testing.

Appendix A: Offset correction circuit

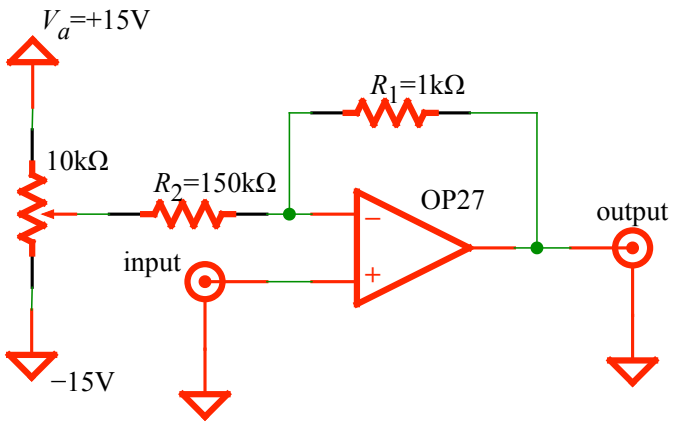

FIG. 32. The voltage offset correction circuit.

Figure 32 is the offset correction circuit. The correction range of the circuit is given by

$$\text{Voltage correction range} = \pm V_a \left(\frac{R_1}{R_2}\right) = \pm 15[V] \left(\frac{1[\text{k}\Omega]}{150[\text{k}\Omega]}\right) = \pm 0.1\text{V} \tag{A1}$$

and the gain of the circuit is

$$\text{gain} = 1 + \frac{R_1}{R_2} = 1 + \frac{1[\text{k}\Omega]}{150[\text{k}\Omega]} \approx 1 \tag{A2}$$

Appendix B: Failed circuit

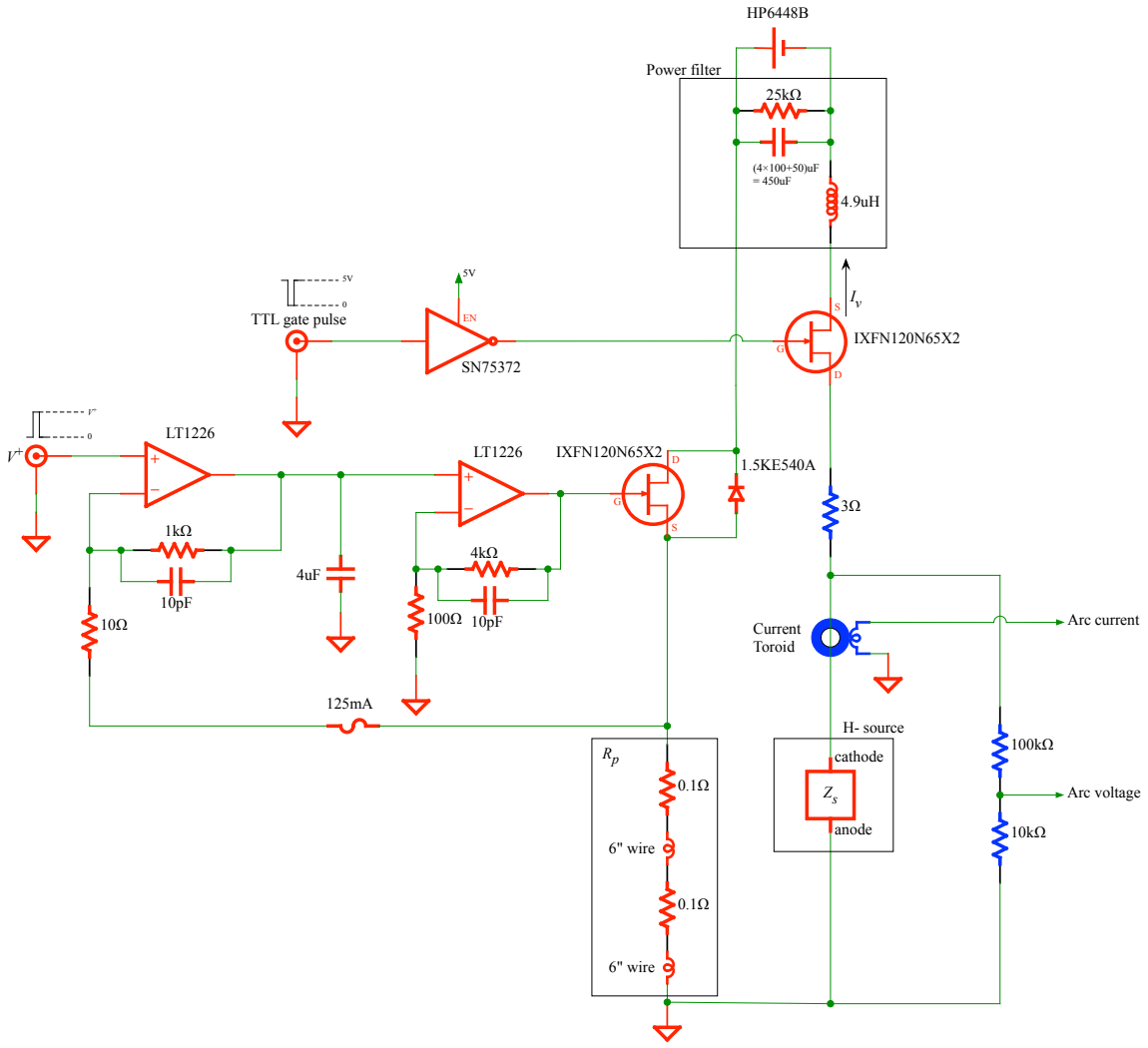

FIG. 33. The MOSFET in the feedback loop is removed because it kept dying. The high current MOSFET IXFN120N65X2 is added to the high voltage power supply. This switches the high voltage into the source only when it is required to be pulsed. Although this circuit works well when connected to a resistive load, it does not work when connected to the source. In fact, we can reproducibly short out MOSFET when we start the source.

We put a high current MOSFET IXFN120N65X2 into the positive leg or negative leg of the high voltage power supply. See Fig. 33 where we have connected the MOSFET to the negative leg of the high voltage supply. After we did this, we found that the circuit worked well when connected to a resistive load. However, when we connected it to the source, the MOSFET kept shorting out. We suspect that when we first turn on the high voltage supply,

the source some how looks like a short and enough current flows through the MOSFET to kill it.

For the other case, when the MOSFET is connected to the positive leg of the high voltage supply, the feedback circuit did not work.

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