Updated Design Notes Of The Regulated Current Arc Modulator For The FNAL H- Source

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Abstract

This document updates the feedback circuit shown in the document "Design Notes Of The Regulated Current Arc Modulator For The FNAL H- Source"

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I. UPDATE

We have redrawn the printed circuit board (PCB) for the circuit and cleaned up the ratsnest. This has helped fix all the noise problems that we have found in the earlier incarnations of our circuit. See Fig. 1.

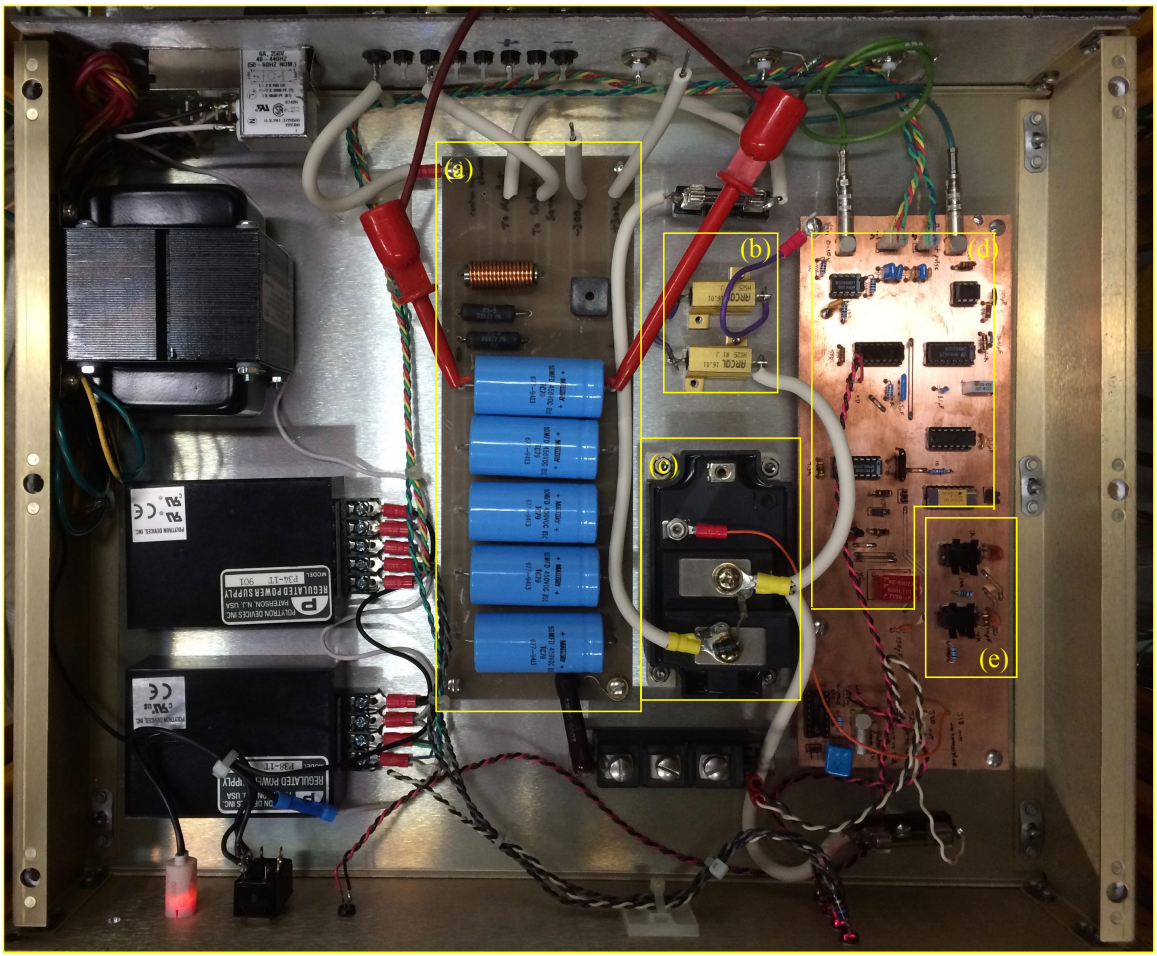

FIG. 1. Our "updated" circuit mounted in a case. (a) The power supply filter circuit (b) Two 0.1 Ω resistors are wired in series to form R_p. The extra inductances have been removed. (c) The high current IGBT MG300Q1US11 that replaced the MOSFET IXFN120N65X2. (d) The digital/analog part of the circuit that creates the V^+ pulse from the trigger and setting that comes from the control system. (e) The low current feedback part of the circuit.

The updated feedback circuit is shown in Fig. 2. Besides the improved layout of the PCB, other improvements to the circuit are as follows:

1. The MOSFET IXFN120N65X2[1] has been replaced with an IGBT MG300Q1US11[2].

The MG300 has a forward DC current rating of 300 A and a collector-emittance voltage of 1.2 kV. We needed to replace the IXFN with the MG300 because we found that during sparks, the 108 A rating of the IXFN is still insufficient because sparks can still cause it to short out.

2. The inductors that connect the 0.1 Ω in series have been removed. The new PCB layout fixed the noise problem that we saw earlier.

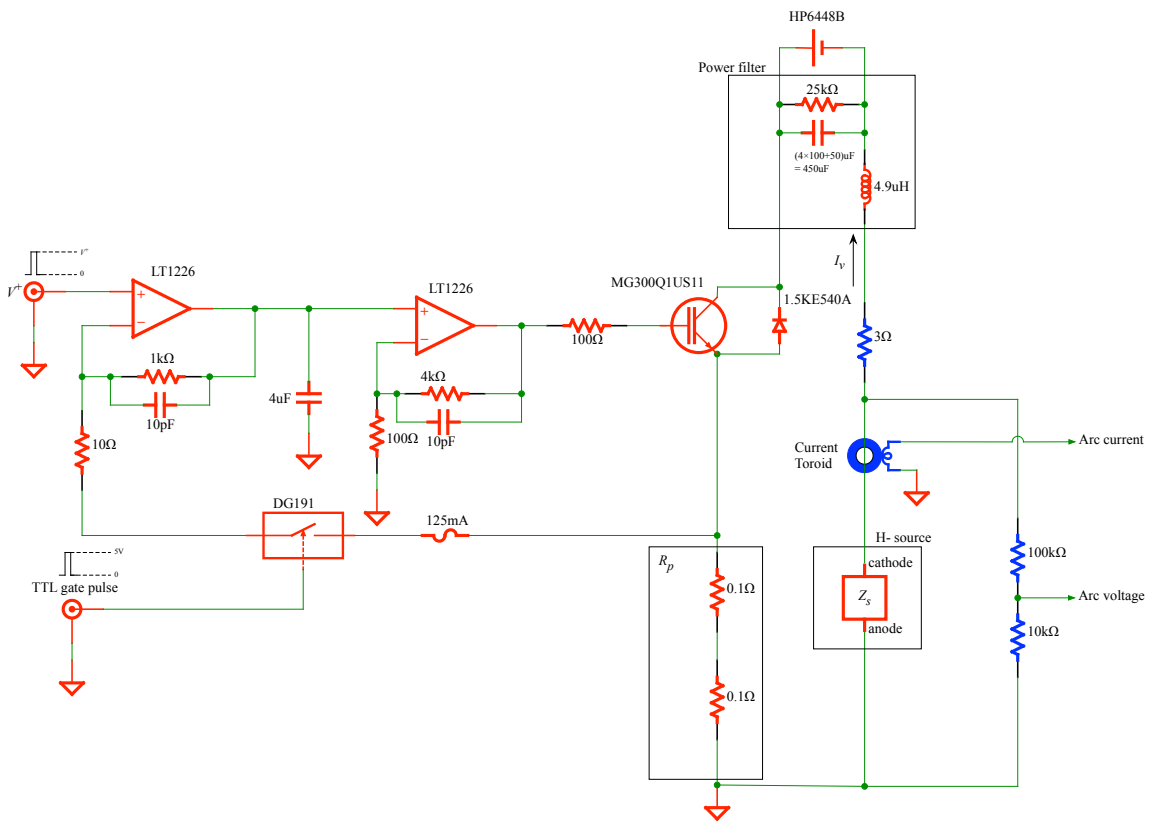

FIG. 2. The updated circuit diagram of the feedback loop.

II. PERFORMANCE

The performance of the feedback loop and other monitored parameters are shown in Fig. 3. We have an unexpected improvement in the fall and rise times of the arc current. Previously the fall and rise times were ∼11 to 15 μs, while in the new circuit the fall and rise times are ∼2 to 4 μs. This is a dramatic improvement! We attribute this improvement to the IGBT MG300Q1US11 which has a max fall time of 1.0 μs and a maximum rise time

of 0.5 μs. Note: Although all the IXYS Mosfets and IGBTs that we have used so far claim to have a rise and fall times < 1 μs, we have not seen this translate to faster rise and fall times in the arc current in practise.

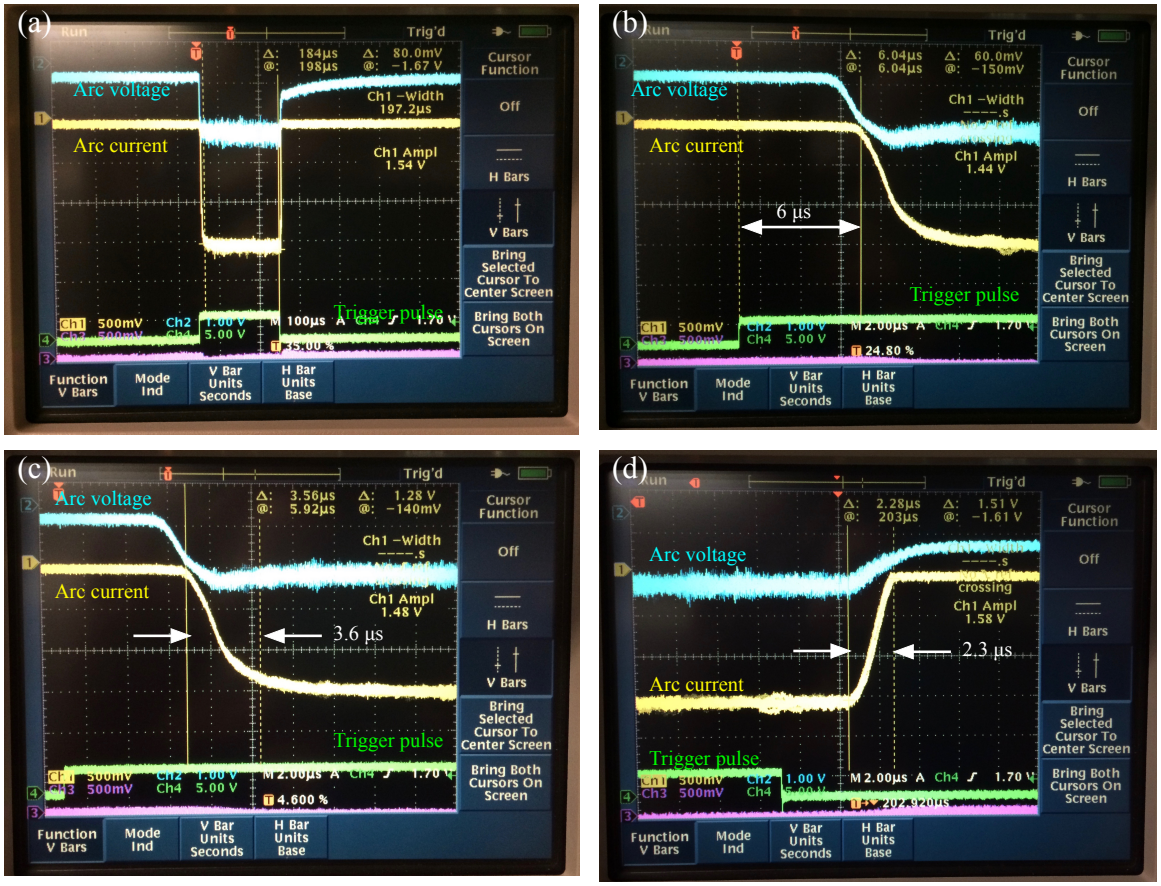

FIG. 3. (a) shows that the arc voltage still has a decay tail after the arc current is turned off. (b) The delay from the rising edge of the trigger pulse to the falling edge of the arc current is still about 6 μs as before. However (c) and (d) shows a dramatic improvement in the fall and rise time of the arc current from 11 to 15 μs to $\sim$2 to 4 μs.

Appendix A: The pulse circuit for creating V^+

The subcircuit that we have made for creating V^+ for the feedback loop is shown in Fig. 4. This circuit removes the need for a voltage offset circuit (that we had used in our prior circuits) because the single pole double throw (SPDT) analog switch, DG191[3], has one of its throws connected to ground. This then guarantees that ground is really ground.

We set the peak of the V^+ pulse with V_{set} that is at DC on another throw of the SPDT switch.

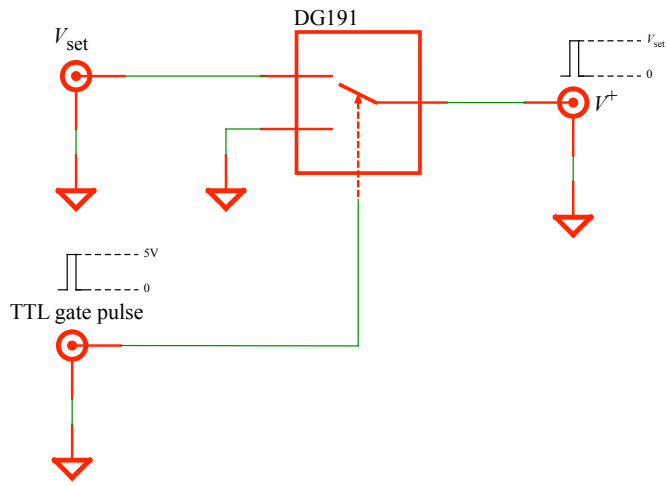

FIG. 4. The V^+ pulse is guaranteed to be at ground when the trigger pulse is at TTL 0 V because one of the throws of the analog switch, DG191, is connected directly to ground.

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[1] IXYS. IXFN120N65X2 - 650V, 108A MOSFET. `http://ixapps.ixys.com/DataSheet/DS100690B(IXFN120N65X2).pdf`, 2016. [Online].

[2] Toshiba. MG300Q1US11 - Insulated Gate Bipolar Transistor. `http://pdf.searchdatasheet.com/datasheets-0/toshiba/MG300Q1US11.pdf`. [Online].

[3] Harris Semiconductor. DG181 thru DG191. `http://pdf.datasheetcatalog.com/datasheet_pdf/intersil/DG182_to_DG191.pdf`. [Online].