PLL for 2nd harmonic cavity

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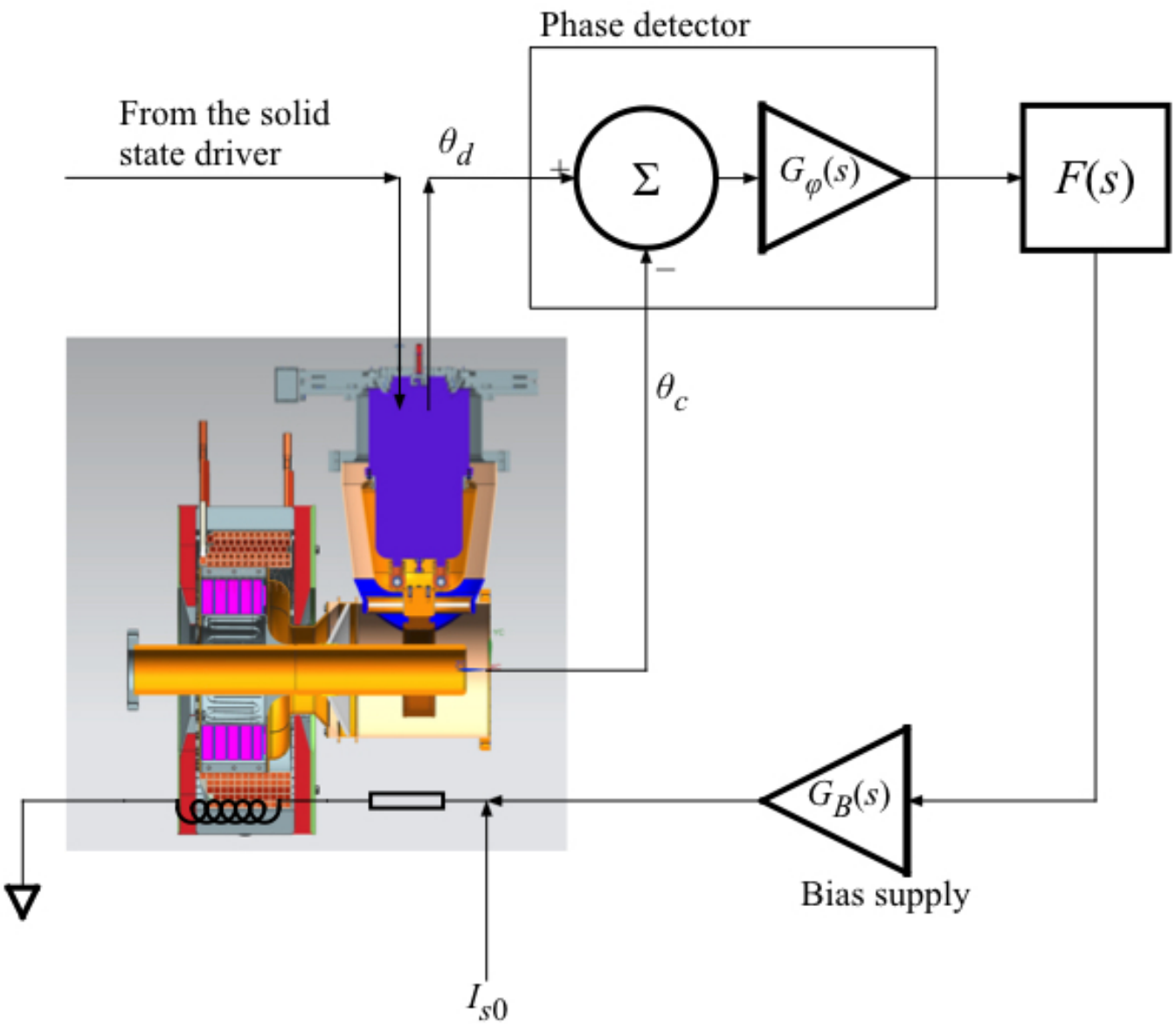
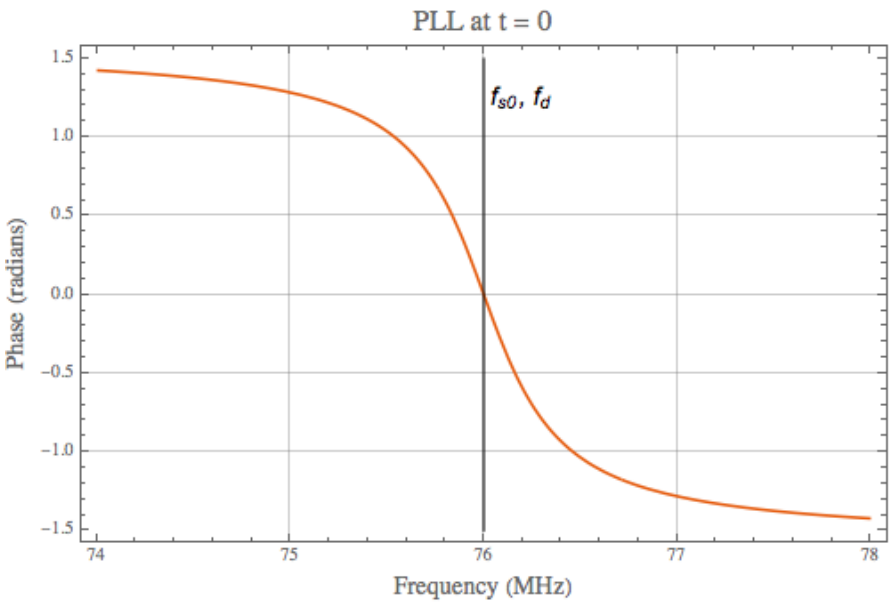
Why PLL?

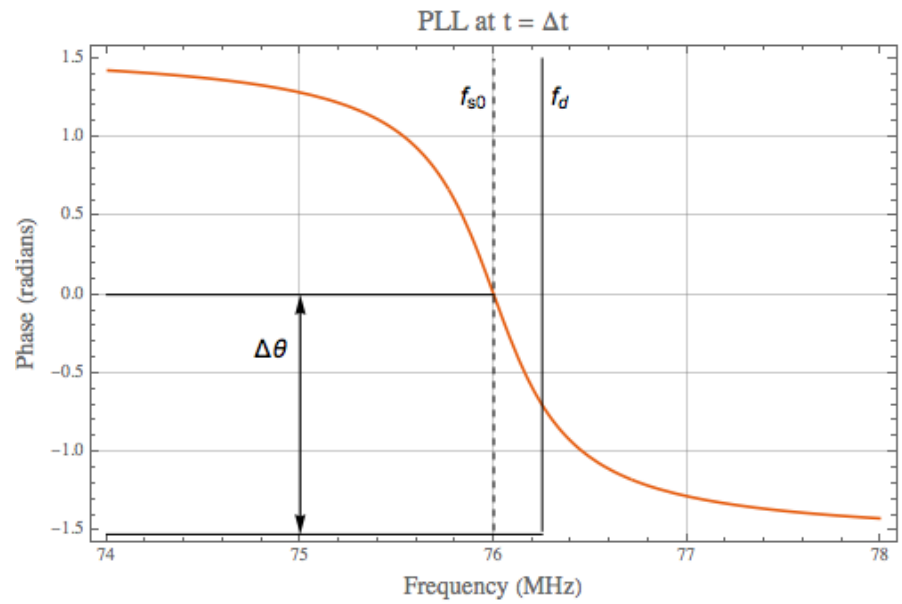
- We need to keep the cavity resonance and the drive frequency in sync.
  - There is a bias current ramp and we have to make sure that the error between the cavity resonance and the drive frequency is tolerable.
  - “Tolerable” here means that we have enough power to drive the cavity to 100 kV even if we are off resonance.
  - Note: we probably won’t drive the cavity at resonance due to Robinson stability requirements. A programmed offset phase in the PLL loop can easily accommodate this requirement.
- Note: No beam loading taken into account at this stage.
  - Need fast PLL for beam loading if necessary.
  - Or other forms of beam loading compensation.

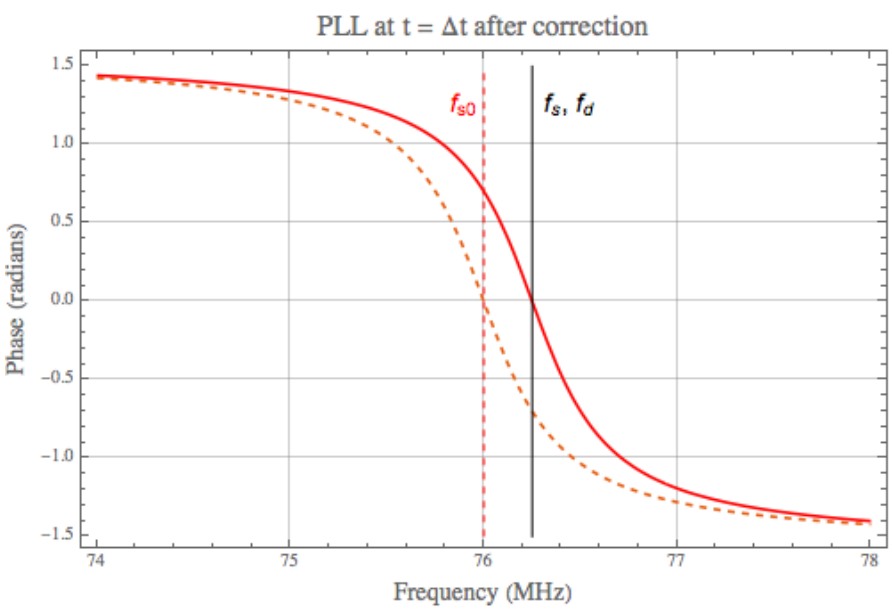
PLL block diagram



How PLL works with a grad student





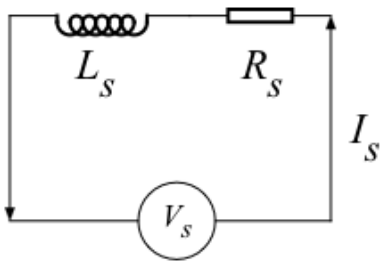


Our grad student looks at the output of the phase detector and sees that the phase difference, $\Delta\theta$, between the drive and the pickup is no longer zero. He then changes the solenoid bias to shift the resonance of the cavity so that $\Delta\theta$ goes to zero again.

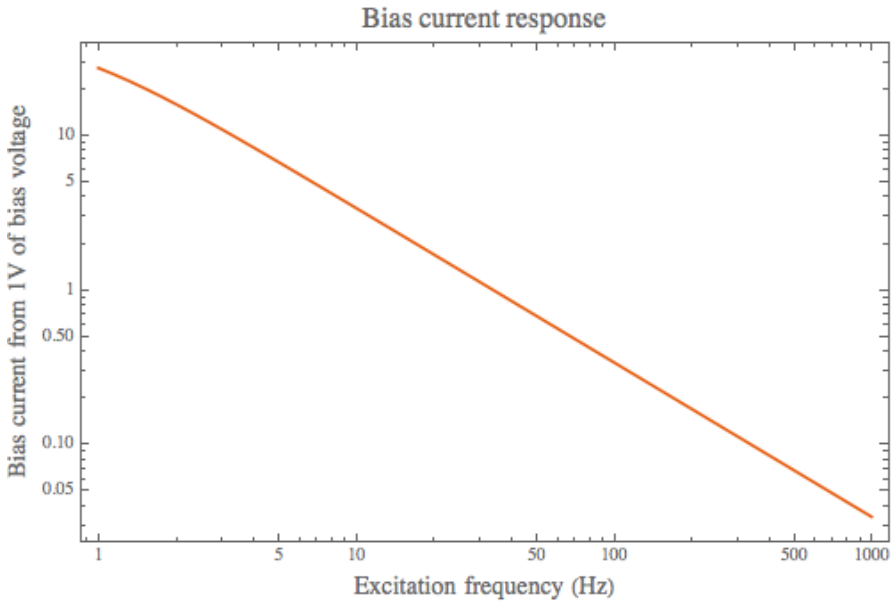
If he turns the bias knob too quickly, he might overshoot. If too slowly he might never catch up. ← This is the gain of the loop.

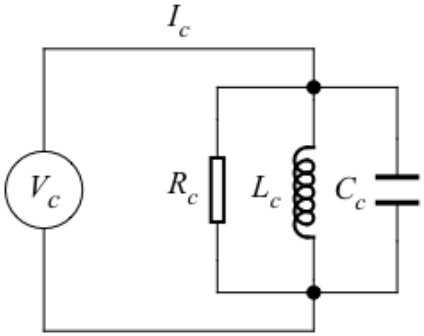
This is how a PLL works.

Modeling

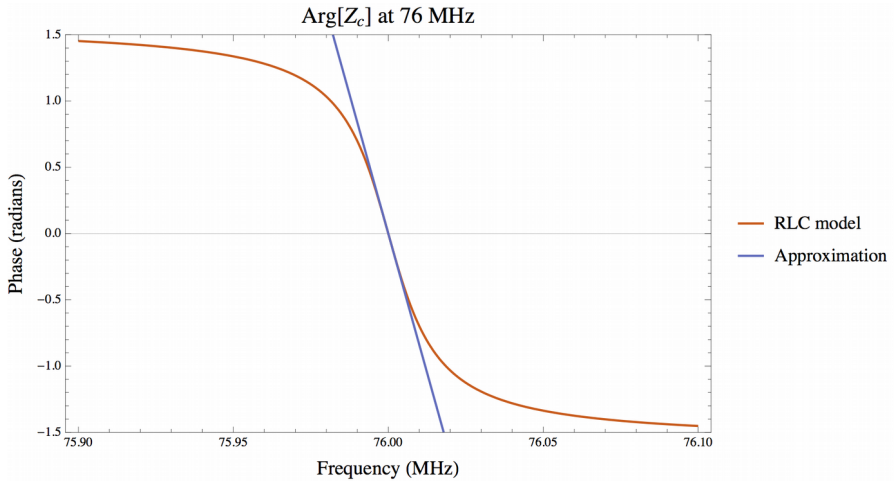


Bias solenoid modeled as LR circuit

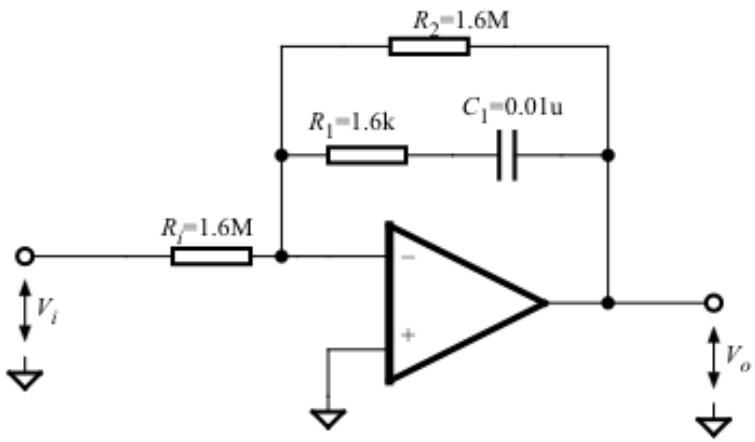




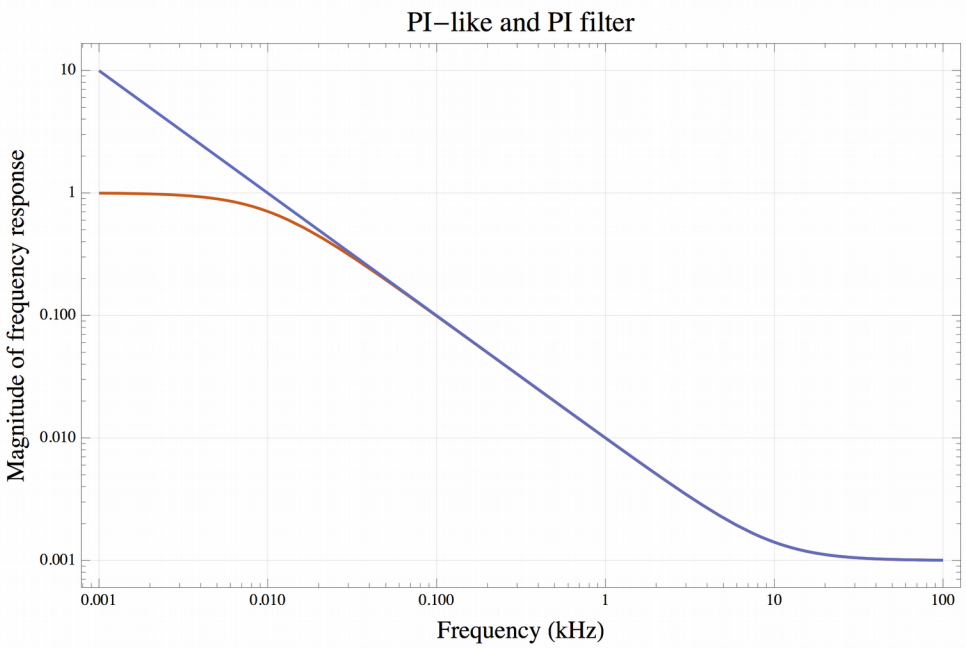
Cavity phase response linearized about resonance.

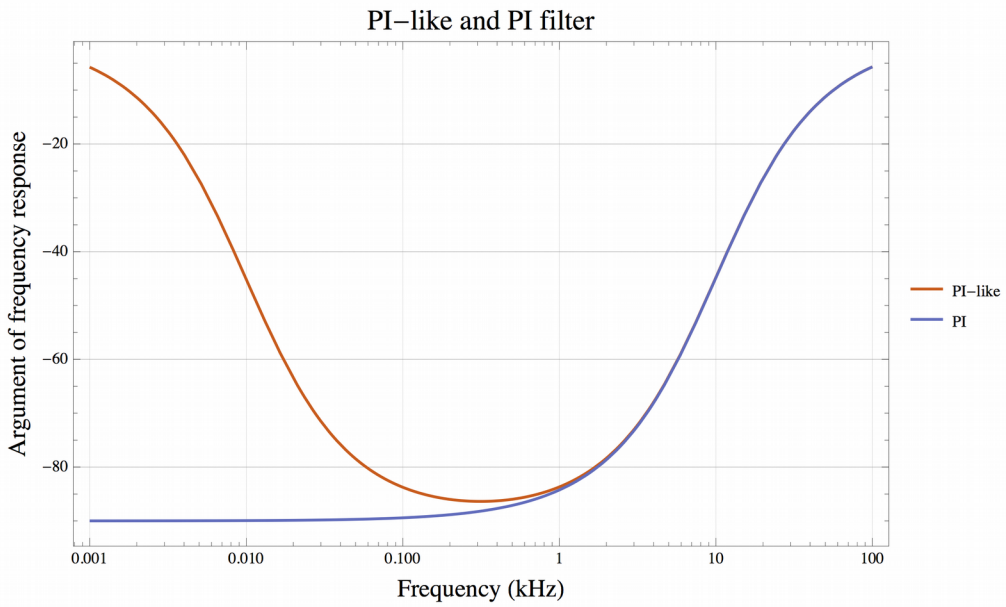


Usual to analyze PLL in Laplace space

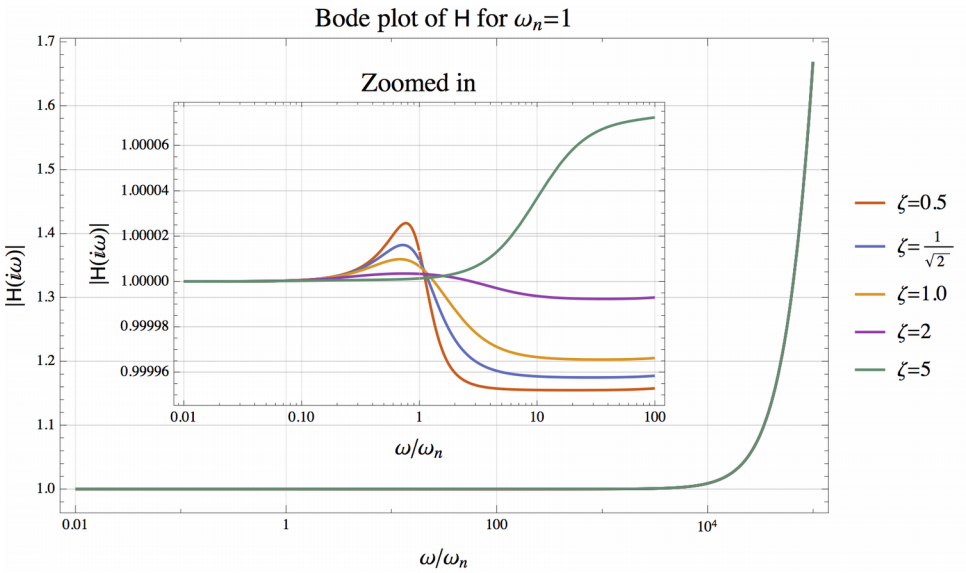


In “s” space analysis, I found that for the PLL to converge when there is a frequency ramp, I needed an integrator.



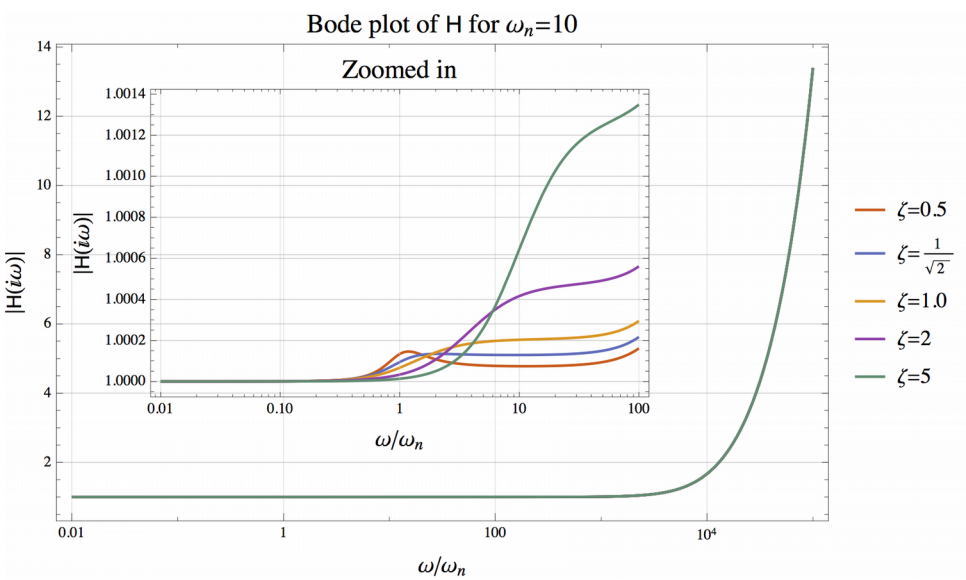


Normalized H Bode plots at 76 MHz



$$\left.\begin{aligned}\Theta_c &= \frac{(Z_s + 2\tau_c F G_B G_\varphi K_d)s - 2\tau_c Z_s s^2}{(Z_s + 2\tau_c F G_B G_\varphi K_d)s}\Theta_d \\ &= \left(1 - \frac{2\tau_c Z_s s}{Z_s + 2\tau_c F G_B G_\varphi K_d}\right)\Theta_d \\ \Theta_c &\equiv \mathcal{H}\Theta_d\end{aligned}\right\}$$

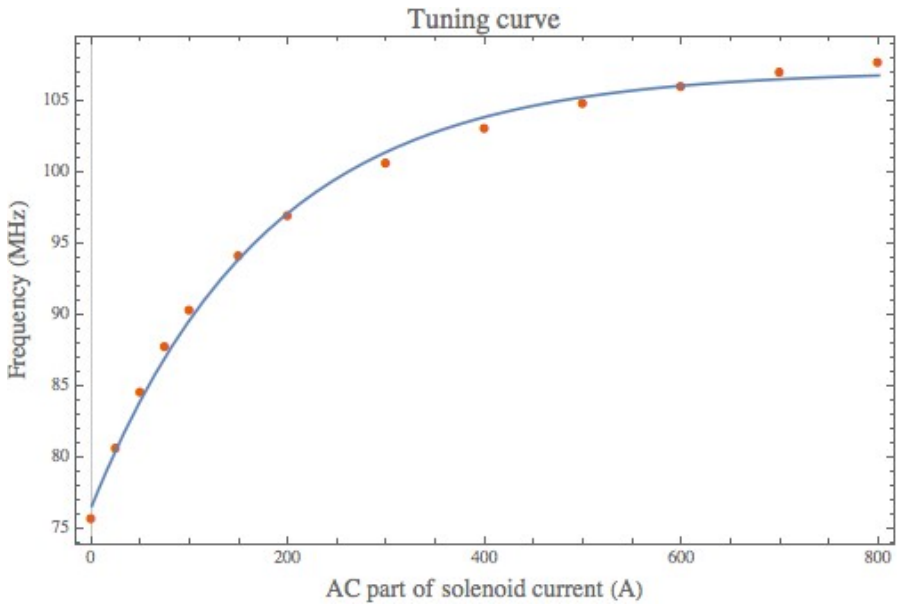
$$\boxed{\Delta\Theta_d = \Theta_d - \Theta_c = \frac{2\tau_c Z_s s}{Z_s + 2\tau_c F G_B G_\varphi K_d}\Theta_d}$$

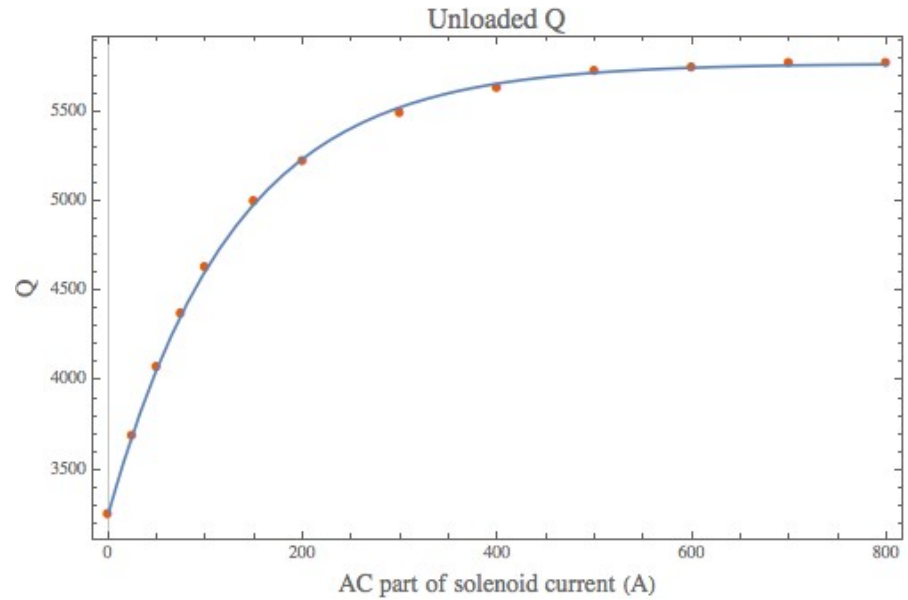


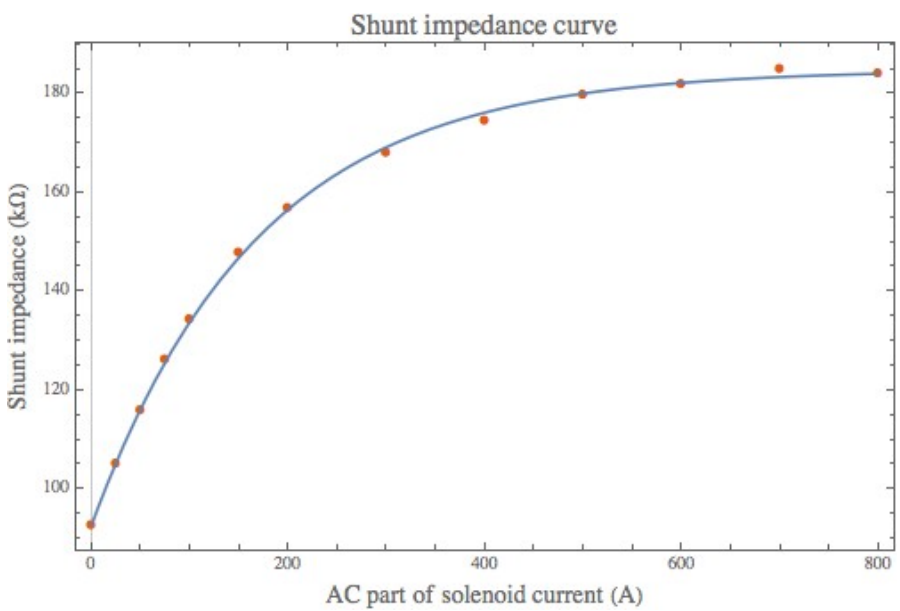
The H Bode plot does not look like a low pass filter because of the <u>extra “s” in the numerator from the bias solenoid.</u> However for low enough frequencies, everything converges. BW is limited to < 3 kHz.

This is ok since corrections are not expected to be larger than 1 kHz bw.

Time domain







$$\left.\begin{array}{lll} g_{I2R}(I_s) = 92.9335 + 91.9393\left(1 - e^{-0.0059101 I_s}\right) & [\mathrm{k\Omega}] & I_s \text{ to } R_c \text{ fit.} \\ g_{I2f}(I_s) = 76.6077 + 30.6104\left(1 - e^{-0.0056044 I_s}\right) & [\mathrm{MHz}] & I_s \text{ to } f_c \text{ fit.} \\ g_{I2Q}(I_s) = 3259.17 + 2513.67\left(1 - e^{-0.0077772 I_s}\right) & & I_s \text{ to } Q \text{ fit.} \end{array}\right\}$$

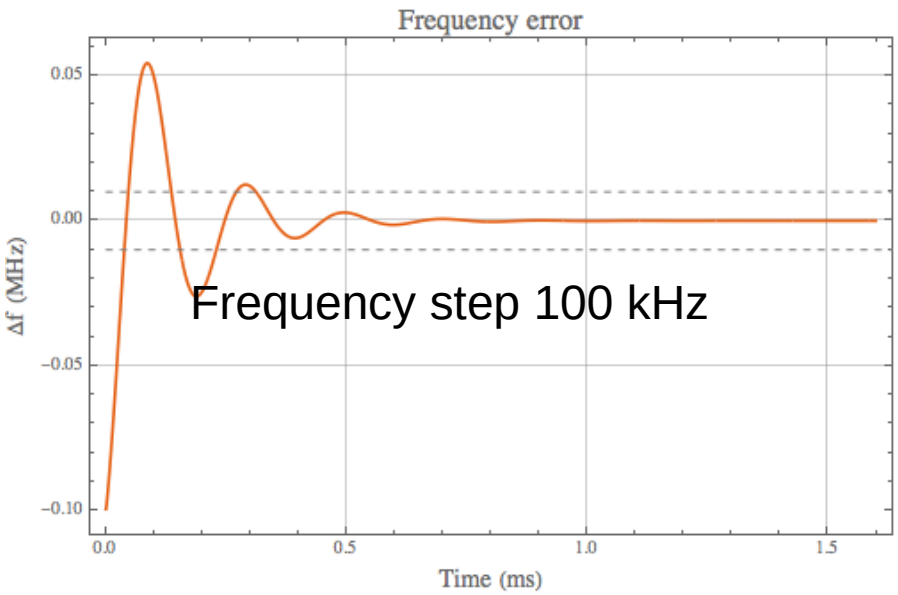
Use Gennady's CST results (22 Jun 2017) and fit to "charging" exponentials.

PLL parameters and requirements

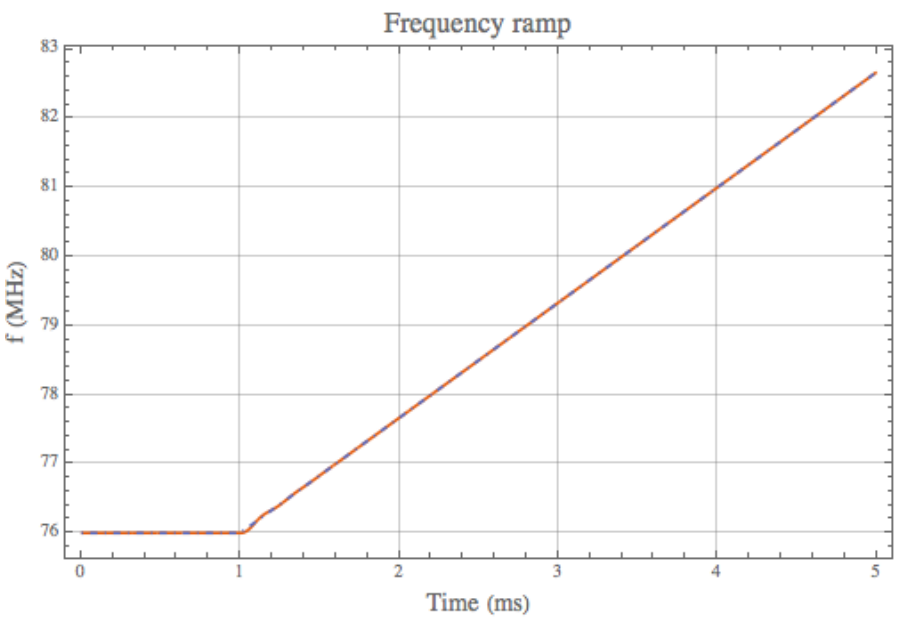
- Open loop gain set to 5000
- Bias solenoid
  - L_s = 4.7 mH, R_s = 21.6 mΩ
- Given the shunt impedance Rc and Qc, I can calculate the required frequency tolerance from 76 MHz to 81 MHz and assuming max power of 100 kW

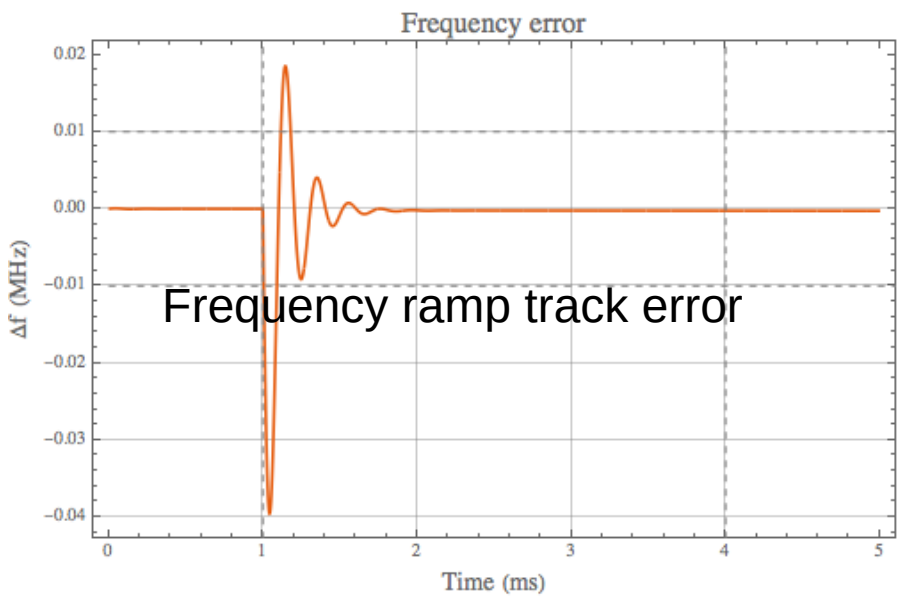
Frequency (MHz)	Q_c	shunt impedance R_c (kΩ)	maximum allowable frequency error (kHz)
76	3200	92.75	±10.9
81	3800	110	±10.9

Results

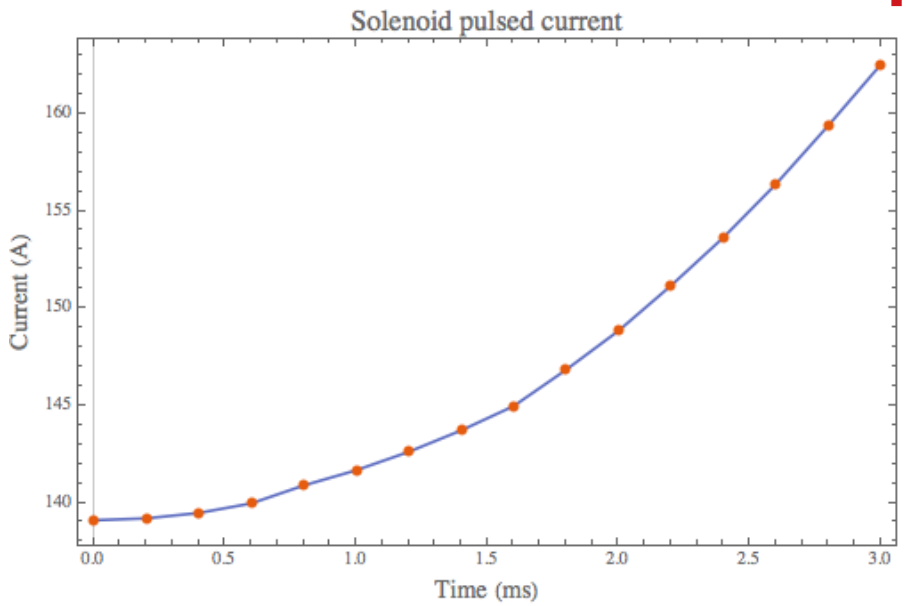


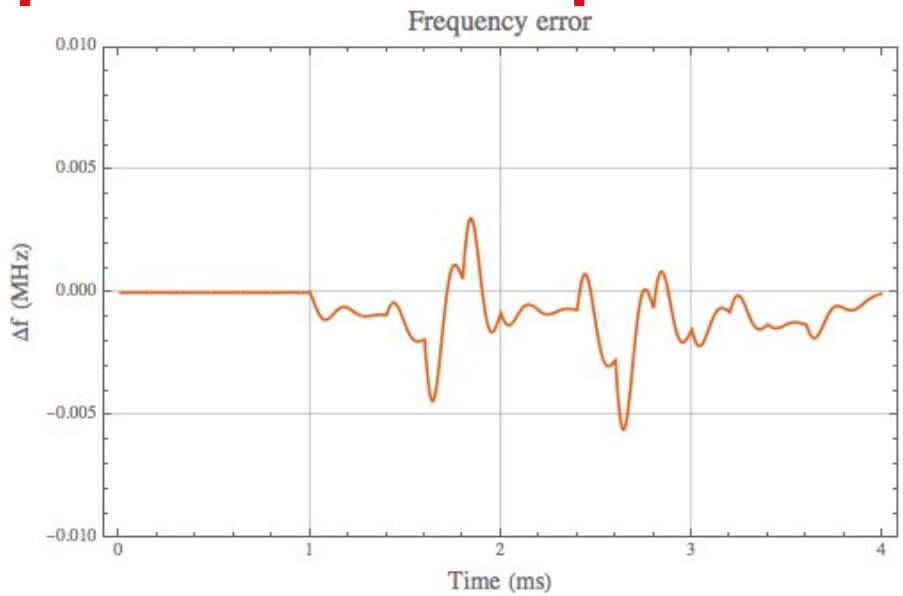
Sudden changes in slope are bad:
Frequency errors outside +/- 10 kHz.

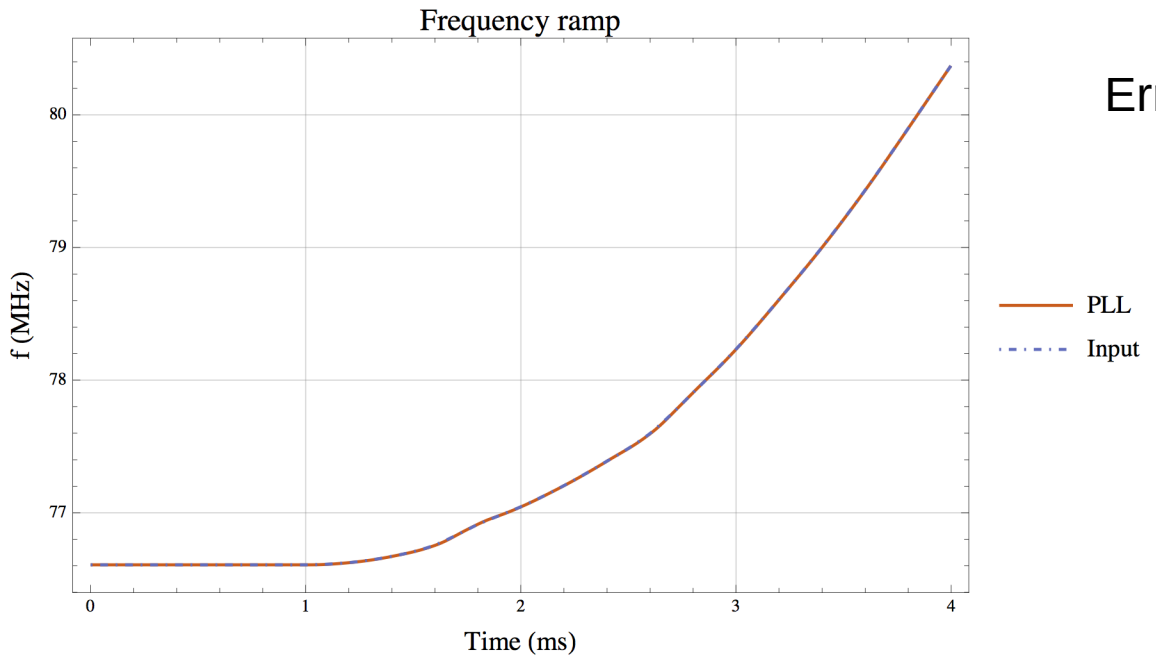




Results of proposed ramp







Errors are within the required +/- 10 kHz

Conclusion

- We have a theoretical design that should be able to track and lock to the given 3 ms ramp to within the required tolerance
  - No noise in the system that will reduce the bw.
  - No beam loading yet!
    - Initial calculations show that this may be a concern.