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**Date:** March 8, 2018

**Re:** Meeting Minutes, PIP-II Machine Protection Introduction to Computing Division

**Meeting Time: 2:00 pm to 3:00 pm**

**Meeting Location: AD / Huddle**

**Attendees:**

Craig Drennan, AD/Instrumentation (Secretary)

Nathan Eddy, AD/instrumentation

Peter Prieto, AD/Instrumentation

Vic Scarpine, AD/Instrumentation

Arden Warner, AD/Accelerator Physics Center (Presenter)

Sasha Shemyakin, AD/PIP-II

Rich Neswold, AD/Controls

Jin-Yuan Wu, PPD/EE Support

Gustavo Cancelo, SCD/Real-Time Systems Engineering (Group Leader)

Greg Deuerling, SCD/Real-Time Systems Engineering

Rick Kwarciany, SCD/Real-Time Systems Engineering

Alan Prosser, SCD/Real-Time Systems Engineering

Ryan Rivera, SCD/Real-Time Systems Engineering

Neal Wilcer, SCD/Real-Time Systems Engineering

**Request for Feedback:**

Please send any additions, corrections, rephrasing and/or comments to Craig Drennan. There has been liberal use of paraphrasing in recalling what others have said in the meeting. There may also be some editorializing and introduction of new thoughts that could use some review. Thank You.

**Minutes:**

Introductions

 The meeting was called to provide an introduction of the PIP-II and PIP2IT Machine Protection System (MPS) to engineers from the Scientific Computing Division/Real-Time Engineering group (SCD/RTE). This was done to see if SCD/RTE would be interested in providing engineering support for the development of this system.

Note that this meeting was limited to an introduction and was not intended to commit either SCD/RTE or the PIP II project management to anything. If SCD/RTE determines that they will be able to provide support for the PIP II MPS there will likely be another meeting where commitments and a course of action begin to be formalized.

This meeting included Peter Prieto and Vic Scarpine from AD/Instrumentation who have management responsibilities in PIP II, Arden Warner and Sasha Shemyakin who have design and management responsibilities for the PIP II and PIP2IT MPS systems, Rich Neswold from AD/Controls currently providing support for the PIP2IT MPS system, and Gustavo Cancelo, group leader for the SCD/RTE department.

If SCD/RTE decides they could participate in this design collaboration, Jim Steimel from AD/PIP-II, Jim Patrick, Department Head of AD/Controls, and others in the org-chart for SCD/RTE and PIP-II will be approached to meet and see if, and how this might go forward.

Arden Warner’s Presentation

Arden Warner’s presentation has been stored with these minutes in **Beams-doc-6189**. PIP-II will likely store these things in their own archive, also.

Before the presentation began several comments were made:

* Peter Prieto wanted to emphasize that the Machine Protection System (MPS) was only one of many (8) areas in the design of PIP-II where engineers from SCD/RTE might lend their support.
* Vic Scarpine expressed concern that Jim Patrick, the department head for AD/Controls, was not in attendance, and that it was AD/Controls is the one running the MPS. Arden explained that when the meeting started out it was only going to be four people gathering for an initial discusses and that further discussion would involve people who make decisions in AD/Controls. Arden had invited Rich Neswold, from AD/Controls, to the meeting since Rich has been working closely with Arden on the MPS for PIP2IT and because he is a good source for understanding how the control system works. Craig Drennan stated that the meeting was just to be a small iteration to see if the MPS work was a fit for the Scientific Computing Division group.
* Sasha Shemyakin stated that as we go forward we also need to include Jim Steimel in the discussion. Jim is the Project Engineer for Electronic Systems (correction?).

Beginning his presentation, Arden described the PIP-II Linac. **See the presentation slide 2**. This Linac will require a robust Machine Protection System to protect the accelerator and associated infrastructure from beam induced damage. The machine would initially be pulsed to inject beam into the Booster, with future accelerator complex upgrades having this Linac drive a CW beam, delivering mega-Watt power. This presents a significant beam damage potential. PIP2IT is our testbed where many ideas are tested. The injection is at low energy into super-conducting RF. This has never been done before. Energy is at 2.1 MeV. So, this is a challenge to instrumentation, machine protection and other systems.

The design currently requires a 10 usec response time from the MPS. The system would use multiple beamline instruments, machine data and triggers. Instrumentation would be used for both tuning the machine as well as for machine protection. We also have MDAT, machine data, that needs to be passed on to other systems, as well as triggers and other timing.

The scale of the system for PIP-II is going to be the same as that of the Tevatron, over a million devices. This will require fast data links. Some way of getting data around the system. And this has not been designed yet.

The **presentation slide 3** shows a very general block diagram. The blue block in the center represents the MPS. This includes the control system, Slot 0 controllers and all the FPGAs the MPS need to take data from all the subsystems represented by the beige blocks to the left. There are more such subsystems, but this provides the general idea. These subsystems are all distributed up and down the Linac. The MPS will control these primary actuators which can inhibit beam in the complex. These systems will be in the Linac itself, or in the Booster.

There will be lots of inputs. Some of this data will be processed data, some of it will be raw data from FPGAs. It is to be determined how the interface works. In between, these interfaces and the MPS, there needs to be some way of getting data to the MPS and other systems that need it so we can affect the primary actuators.

**Presentation slide 4** is another representation of all of the systems that need to be integrated, to work with the MPS. Some of the systems, such as the toroids, scrapers, and BLMs, are special in that the MPS will rely on them to make decisions. All these other systems are involved, and of course RF Interlocks, and these other systems can benefit from fast distribution of data.

**Presentation slide 5** shows a representation of the ACNET control system as it is right now. It is a three-tier system with Applications, Central Services and Front-Ends. The field hardware connects to many types of hardware such as older CAMAC, VME, VXI, PCI or even other platforms that we must consider as we move forward. It is at this lower tier that the machine protection system must sit. The MPS must receive data from the field hardware quickly and reliably, and then this data must be passed further up the control system. This is the current scheme as implemented for the current PIP2IT injector test MPS.

**Presentation slide 6** is a block diagram showing one example of integration. There is the MPS and the MPS Permit Generator. At some level it interacts with the accelerator complex, PIP-II level controls. On the left of the slide are instrumentation out in the field that the MPS relies on, and the blocks at the top represent sub-systems that also need to feed into the MPS system, at some level. The MPS Signal Interface/Fast Link block represents the missing piece. There is a need to get information quickly, especially when PIP-II Linac is run in a CW mode. There needs to be some source of streaming data through the system.

**Presentation slide 7** are Arden’s current thoughts on the Fast Link requirements. The slide text is copied below.

Distributed instrumentation and diagnostics

* + Ability to use processed (FPGA) instrumentation data from all parts of accelerator complex for MPS and RF interlock
	+ Requires hardware that interfaces to digitizing hardware electronics

High bandwidth data handling backbone

* + High speed transmitter/receiver capabilities (a communication protocols)
	+ High density fiber optic connections (MTP/MPO ???)

High resolution, high precision timing system

* + Sub-microsecond resolution
	+ Timestamp synchronization
	+ Machine Data at high update rates Gbps or better??
	+ Thresholds, Masking etc.
	+ Inexpensive
	+ Bridge to control system (Currently ACNET - lots of legacy stuff)

A bridge to the current control system is necessary. Once we have a broader discussion with Jim Patrick and AD/Controls, we can talk a lot more about this.

Vic Scarpine added at this point, that the system must be real-time. Delays and latencies must be managed and minimized. Issues of data traffic and collisions must be addressed. This must be clearly addressed and specified in the requirements.

Nathan Eddy added that the system should have deterministic delays.

Sasha Shemyakin added that the designers of the LLRF systems should be brought in on the discussion of a fast link. The LLRF system requirement for this link maybe even more severe. They will want to keep RF phases along the entire Linac to a tight tolerance.

Arden stated that we will need to expand on the requirements to include all these issues. **Presentation slide 8** is a very basic block diagram that we start from. There is a connection to the broader accelerator complex, systems besides the MPS.

**Presentation slide 9** provides some description of the MPS system we are currently using with PIP2IT. It shows It includes a general purpose FPGA for the MPS. It takes the inputs and creates a large register map that is used to set things. Jin-Yuan Wu helped Arden with the programming of this module. This module sits in a crate with the control system and with the digitizers and the other infrastructure that you need to generate a machine protection system.

General Discussion

Gustavo Cancelo inquired further about slide 9 and Arden reiterated that what was shown was just one board in the system. Essentially, they use a summation FPGA board, some digitizers, a front-end system. They are already running into data issues and limitations because at PIP2IT the instrumentation systems and the MPS are in segmented front-ends, and in being able to get data quickly, they must be concerned about where they draw the line. Does the data used for tuning stay here and the data for MPS stay there or do we put pressure on Rich and John to figure another way to get data to us quickly, so we can make decisions? It is not as big an issue with PIP2IT as it will be with PIP-II, where we will need a dedicated system.

Sasha asked Arden to describe what PIP2IT is for the people from SCD that may be unfamiliar. PIP2IT, the PIP II Injector Test (previously known as PIXIE), is in the CMTF facility at the north end of the lab. There is an accelerator front-end test of the technology that is necessary to build PIP-II. It is the low energy part of the system. This includes the source and the RFQ. It gets beam up to 2.1 MeV and will inject this beam into the super-conducting cavities to get the energy up to 11.4 MeV. The warm front-end system is existing now and this is the testbed we are using to test a lot of the technologies that we need to use.

Sasha related that an accident had already burned a hole in the vacuum system, and this was evidence of the importance of the MPS. There is 10 to 20 kW of beam power there.

Gustavo asked about the timeline for the work. Below is an estimate timeline from details of the discussion. Note that this is not a precise timeline. Further meetings and or requirements are needed to make schedules and contingencies more precise.

* PIP2IT is running beam right now and will continue this for the next few months
* PIP2IT will then be shut down until 2021, after the installation of the Half Wave Resonator (HWR). At this time new MPS hardware and system prototypes, and other systems, should be in place to be tested.
* The HWR will be commissioned and then beam will be off until 2022, after the installation of SSR1.

The prototype equipment, for PIP-II, will need to have been designed and tested by 2023. These systems will need to be scalable and scaled up for the completion of the PIP-II Linac in 2030.

* PIP-II has gone through reviews for CD-1 and expects to receive this approval in another month. Sasha remarked that one peculiarity is that all the activity with PIP-II will include Indian collaborators. Peter Prieto is interfacing with the Indians. We must remember that whatever we develop must be compatible with what the Indians are doing. Therefore, it is important to understand the entire architecture of the proposed system. Plans for the PIP-II MPS do not exist currently. There are requests now from the Indians for more information and more specifications.
* The director will be pushing to have the CD-2 review in the Spring of 2019 or sooner. In September 22, 2018 there will be CD-2 reviews of hardware designs. At this time, we will need to be able to present our plan for the MPS system.

Gustavo noted that the prototype systems designed and tested for PIP2IT needs to be scalable to the final PIP-II system.

It was asked how detailed designs needed to be for the CD-2 hardware design review.

Peter Prieto responded that you will have external reviewers that will be asking how you will be implementing the hardware. They are not asking for the final implementation. CD-3 is when you actually start implementing the hardware. For CD-2 you are saying approach will be and the reviewers will be evaluating whether your approach makes sense. So, for the MPS system, we will be saying this is how we plan to do it, and these are the pieces and you have to be very specific. Once they approve this, you can move into actual hardware design.

Sasha spoke up and stated that the specification for the MPS is still in draft form. At the CD-2 review we will need conceptual designs for everything.

Gustavo asked who will be in charge of designing and engineering the many different systems that Arden showed as having input to the MPS system? Who would be designing the different front-ends? Vic Scarpine replied that there are many groups that will be involved. There is the Instrumentation group, the Low-Level RF group, the Controls group, the Vacuum group.

Craig asked whether we were early enough in the process that if we come up with an MPS system that needs a specific interface, that we can tell other people that they need to put these interfaces on their boards? Peter replied that the process is clear. We will need to generate a Functional Requirements Specification (FRS), and then a Technical Requirements Specification as to how your going to implement the system. Then, and Interface document must be written that specifies all the interfaces between systems. For example, the MPS system would have an Interface document for each of the system Arden had mentioned as having a connection with the MPS system. It would specify what elements make up the interface. These are all the documents specifically required by the project management.

Gustavo tried to summarize the basic architecture described so far in the meeting. He described it as

* A layer, that is the front-end interfaces to all the devices.
* A second layer that is like the data concentrators and timing modules that Rick Kwarciany and company have built.
* And then switches, or something similar, to convey the information back to the MPS system responsible for taking action (perhaps the MPS Permit Generator).

Presentation of Slides by SCD/RTE

Arden asked to see some slides or information about what SCD/RTE had done in the past.

Rick Kwarciany said that for the Mu2E DAQ system they have been using a combination of off-the-shelf FPGA, PCI Express card with and FMC connector and a custom fiber optics FMC interface card. As time goes on they can replace the different pieces and that they hope to use mostly off-the-shelf modules. They do have some talented board layout people who can design the custom parts as needed.

Vic Scarpine asked how they would avoid collisions of data. How can you be sure that the system would respond in real-time? Nathan Eddy asked whether the fiber connections were all point to point?

Rick replied that for Mu2E they were doing a lot of point to point connections, but we are also using commercial 10 Gbit switches. With this, we have a timing system that synchronizes all the Data Transfer Controllers (DTCs) so that they interleave when sending packets so we do not get blocking at the switch.

Two-Tiered MPS System

Sasha Shemyakin brought up the logic that is in the currently implemented MPS for PIP2IT. It is assumed that the MPS would be a two-tiered system. The first tier would consist of devices that belong only to MPS and protects the entire machine from the beam. Sasha believes the first-tier connections for device data to the MPS will require a dedicated communications system.

Each individual system should provide its own protection and also input to MPS. For instance if a cavity starts sparking or if one of the insertion devices moves in and the mode of the machine in not appropriate, the MPS should shutdown the beam.

These and other concepts for the existing MPS for PIP2IT are described in the CDR that Arden Warner can make available.

Arden Warner brought up a concern with interfacing legacy systems in the Booster with newer PIP-II data and MPS systems. There may be scenarios where a fault beyond the PIP-II Linac would require beam to be shut off. Do we need to make the MPS extend further beyond the Linac?

Gustavo Cancelo’s Summary

Gustavo made a summary of what he heard and felt about it. He said that he believes that he now understands the challenge of the project, and the time line that the work needs to occur in. That there were two tasks. The first was developing prototype systems that would protect the PIP2IT machine and coming up with an architecture for the final PIP-II Linac. They will be going back to their offices and talk and see if they can add more people to this project.

More of what SCD/RTE has Developed

Vic Scarpine pointed out that the hardware that allows fast data communications discussed in the context of the MPS system, could be separated out for consideration with the other Linac systems such as RF and Instrumentation not related to MPS.

Nathan Eddy stated that from the RF and Instrumentation stand point, we would like a timing system that could be tagging things and synchronizing things at the butch level. The bunch frequency is at 162 MHz. This is an order of magnitude more that what we are doing now, but by today’s standards is reasonable.

Rick Kwarciany showed photos of the PCI Express board that they are using for the Nova and Mu2E data acquisition and timing distribution. There was also a photo of the custom FMC module with the fiber communications interfaces. These boards fit into a 3U high computer. They may fit in a 2U high unit. The FMC module supported up to 8 bidirectional links that could each run up to 10 Gbit/s. In Mu2E they are running a few of the modules at 10 Gbit/s and the rest at 4 Gbit/s. You can buy all sorts of FPGA boards in the FMC standard. This particular board has IO to PCI Express. It has 4 Gbit of DDR memory. The custom FMC fiber communications interface was designed in house because they wanted to have their own timing distribution layer in this board. The connections on the board support MPT fiber transmitters and receivers.

A block diagram of the Mu2E DAQ system was shown on another slide.

It was noted, that for the proposed MPS system that the PCI card in the PC should be reconsidered. If the computer was to reboot the card may lose power. You would want a second level system in a box with its own power supplies. There are other FMC carrier boards that could be used. There is a custom board that they have made that allows the connection of up to four FMC boards which allows for a lot of IO. This particular board also has gigabit ethernet on the main board.

There was more discussion of the available hardware.

If you remember something you found important that we should include in these minutes, let me know and I will add it.