Meeting Minutes

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**Date:** January 25, 2019

**Re:** Meeting Minutes, UCD Clock Decoder Support Meeting

**Meeting Time: 2:00 pm to 3:00 pm**

**Meeting Location: AD / Loft**

**Attendees:**

Craig Drennan, AD/Instrumentation (Secretary)

John Diamond AD/Instrumentation

Kevin Martin AD/EE Support

Dan McArthur AD/Controls

Peter Prieto AD/Instrumentation

Duane Voy AD/Instrumentation

**Request for Feedback:**

Please send any additions, corrections, rephrasing and/or comments to Craig Drennan. There has been liberal use of paraphrasing in recalling what others have said in the meeting. There may also be some editorializing and introduction of new thoughts that could use some review. Thank You.

**Minutes:**

Introduction

In this meeting, we began considering the support of the current clock decoding and timing modules widely used around the Accelerator Division. These modules decode TClk, MDAT and Beam Sync serial streams to provide timing and trigger for many data acquisition and control systems. Craig McClure has been the main person supporting these devices and has recently retired. We are taking this opportunity to communicate with the Controls department to discuss the current status of support and consider updating the specifications for a new revision of the modules.

Discussions and Emails

It was pointed out that the AD/RF department also uses the VXIUCD version of the clock decoder modules but were not at the meeting today. A future meeting will include discussion of specifications and support with them. Future discussions are also expected to include Greg Vogel and Valery Rychenkov from AD/Controls.

Duane Voy started the discussion of the timing modules. He explained that the systems we are most concerned with are the older BPM systems that are based on the Echotek digitizers. He had done an inventory and found that we have 27 nodes that use the generation of timing modules being considered.

Duane later provided a listing of the timing modules used for BPM systems in the following areas:

1. MI-8 beam transport line
2. MiniBooNE beam transport line
3. NuMI beam transport line
4. Delivery Ring
5. Main Injector
6. Recycler
7. Muon Transfer

Duane included the following notes

1. A BPM timing subsystem consists of
     - a VME Industry Pack (IP) carrier board
     - a VME carrier board, fanout board
     - an IP-UCD IP module
     - an IP-TSG IP module
2. We currently have 25 operational nodes in the field.
3. We currently have 2 operational development nodes.
4. There are 2 development nodes that have long since been scavenged for their parts.
5. TSG firmware version 2 may be replaced with version 4.
6. TSG firmware version 5 is distinctly different and not backward compatible.
7. Given 5 & 6 above, we require spares for both TSG firmware versions 4 and 5.
8. We should NO LONGER consider the development nodes to be part of any spares pool!

Additional follow-up to the meeting included some information that Dan McArthur received from Craig McClure. Craig wrote:

1. There are 18 [***spare***] General Purpose Industrial Pack (GPIP) modules that are functional.
2. Six of these modules have been programmed with PROMs and fully tested to be IPUCDs.
3. Six others have been programmed to be Delivery Ring BPM Timing Signal Generators (version 5, IPTSGs). These, however, have not been fully tested.

\*\* Note from C. Drennan: I do not see spares developed for IPTSG version 4 in the email.

1. These 12 modules are intended for use by AD Instrumentation as spares.
2. The remaining 6 GPIP modules are available to be programmed and tested as needed.
3. There are approximately 25 other GPIP modules that do not power up.

Craig McClure’s email to Dan included further details on other aspects of the modules.

In the meeting, Kevin Martin asked about the designer and manufacturer for the GPIP modules. These Industry Pack standard modules were designed by Fermilab, and BiRa Systems Inc. was contracted to produce them. BiRa Systems Inc. no longer supports these modules and the FPGA’s used on the GPIP are no longer available. Kevin stated that EE Support uses the PMC module version of the UCDs (PMCUCD) exclusively.

Instrumentation also uses the PMCUCD on each of the BPM front end processors, for the systems listed previously.

Duane mentioned some reliability issues with the PMCUCDs. He said that in the past the PMCUCD system (hardware, firmware, software) was not particularly stable (deterministic). For this reason, Duane and the other front-end developers, got into the mode of using the IPUCDs on VME carrier boards. We also needed the IPTSG Timing Signal Generator (a.k.a. Beam Sync Timing module) that is on the VME carrier boards. The IPTSGs supply functions that the PMCUCDs do not provide. The PMCUCDs are on the front-ends for the sake of ACNET communication functions (MOOC).

About a year and a half ago, Charlie Briegel did some more work on the PMCUCD and fixed the problems. Duane has since used the PMCUCD with the Booster longitudinal damper system without a problem.

As for a time line, the IPUCD and IPTSG modules were used on the older 6800 front-end processors that had connections for the installation of IP modules. When the switch was made to the MVME power-PC, these had PMC slots, not IP slots, and the PMCUCD was developed. When Instrumentation was not having good results using the newer PMCUCDs they went back to using the IP modules on a separate VME carrier card.

With regard to the IPTSG Timing Signal Generator (a.k.a. Beam Sync Timing module) there are three active versions, 2, 4 and 5. Craig McClure said that we can replace version 2 modules with version 4 modules. Version 5, however, is design specifically for the Delivery Ring. In the Delivery Ring they use the Recyclers Beam Sync clock to get injection information and then they switch over to Dave Petersen’s LLRF turn marker and RF signals. When we see the extraction event from the Recycler Ring and then start counting the Delivery Ring RF and turn marker.

Of the 27 nodes listed by Duane Voy, 2 are test nodes. One test node is using a version 2,4 IPTSG and the other is using the version 5 Delivery Ring IPTSG. Up until now we have not had any spares.

Duane mentioned that some of the IP modules had a faster FPGA that was required for the IPTSGs. He also mentioned that there are 8 bit DIP switches used to configure the firmware that he never understood.

Looking Forward to New Clock Decoder Form Factors

We are needing to begin making decisions on the form that DAQ systems for future projects will take, particularly for PIP-II. Kevin Martin pointed out that almost all DAQ designs include their own FPGA in which the clock decoding could be done. What are the trade offs between everyone building their own decoders and having a central design supported by the Controls department? Dan mentioned that both the PMC and the IP module clock decoders are full timing module that can receive a beam sync or TClk event and wait a settable delay, or count RF ticks, and fire a trigger pulse.

Peter Prieto said that he had developed a VME Timing module for the Recycler that decodes MDAT, TClk and Beam Sync. This is the design that the newer BPM systems in Booster and IOTA timing is based on. Duane mentioned that Nathan Eddy’s and Alexey Semenov’s modules for beam damper applications decode TClk and Beam Sync in the FPGAs.

Dan mentioned the MultiFunction Timing Unit or MFTU, that Mark Austin has developed. It has many clock decoding functions and fine programmable delay and rf clock inputs. It is a stand-alone ethernet device. You do not need a CAMAC or VME crate. A summary of the I/O for this 1U rack mount device is below.

Predefined I/O

2 Clock inputs (Booster RF or TTL version available)

2 Trigger inputs (TTL)

2 BS Clock inputs

2 BS Clock outputs (fed directly from the respective BS Clock input)

1 TCLK input

Configurable I/O

32 channels (configurable as either Input or Output in groups of 4)

Mark has told me that the price for the unit is $3k, and he gives the following introduction.

The MFTU is a system whose main intent is to function as a gated timer module that counts the delay based on a given clock, however, it can do so much more than that. The MFTU has a version selection from 0-4095. This allows for many different options preprogrammed into the FPGA that can then simply be selected for the functionality desired by the end user.

Nearly everyone at the meeting expressed interest in learning more about the MFTU. I spoke with Mark and he will be making the documentation available soon.

Discussion of PMCUCDs

Kevin mentioned that the PC104 based systems used for power supply control have a PMC adapter that can use the PMCUCD and the ACNET front-end processors need PMCUCDs for communication with ACNET.

Kevin went on to describe that there is the oldest version that cannot be procured anymore. This board was bought from Techno-Box. Kevin has a large stock of these PMCUCD\_v1 boards. Kevin uses these for the MECAR systems.

Techno-Box has a newer PMCUCD\_6070 that uses a larger, yet still obsolete, FPGA. There is a newer version of the firmware and software drivers for these PMCUCD\_6070 that works well. Kevin needed more features like MDAT decoding, as well as TClk decoding and an external trigger for free-running timers not associated with TClk. The new features would not fit into the older FPGA on the PMCUCD\_v1. So, he worked with Craig McClure to develop the firmware and software drivers for the PMCUCD\_6070. **Kevin expects that Craig McClure had bought several of the PMCUCD\_6070 modules but does not know where they would be kept.**

After the meeting, Dan looked at the Technobox PMC modules used for the PMCUCD\_v1 and PMCUCD\_6070. His email is below.

<https://www.technobox.com/xmc-pmc-digital-io-controllers-adapters-modules-fpga-programmable-configurable.htm>

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| [Digital I/O Controllers / Adapters FPGA Programmable Configurable Board / Card / Module - XMC,PMC,VME,cards,modules,boards,VPX,PCI Express (PCIe),U.2,m.2,NVMe,Technobox,mezzanine,adapters,daughter card,VITA 42,VITA 61](https://www.technobox.com/xmc-pmc-digital-io-controllers-adapters-modules-fpga-programmable-configurable.htm)www.technobox.comPart Number Click to sort Product Photo Datasheet Description Click to sort; 2195: 32-Channel Digital PMC with 30-ns Time Stamp function: 2372: 96-Channel Reconfigurable Digital PMC with Altera Flex 10K70 FPGA PMC |

The PMCUCD starts life as a Technobox Model 2372 “96-Channel Reconfigurable Digital PMC with Altera Flex 10K70 FPGA PMC”.

The Flex 10K70 is obsolete.  An updated version of the card is listed on the Technobox website, Model 6070, based on a Cyclone 1 FPGA which is… drumroll… obsolete.

The story goes that Craig designed the original card, then turned it over to Technobox to productize and produce.  He may have schematics that we could update with a more modern FPGA.

After the meeting Dan McArthur received a quote from Technobox for buying more PMCUCD\_6070s.

For the PMCUCDs there is the possibility of using the current PMCUCD design and update the FPGA.

About IP Modules

For the IP Timeline Signal Generators (IPTSG), Duane said that Craig McClure had recently ported the Delivery Ring, version 5, FPGA firmware from MaxPlus to Quartus.

The VME fan-out carrier board, that the IPTSGs are connected to, has signal conditioning for incoming RF used as clocks, and possibly other inputs and outputs. Dan said that we should have a look at what is on the fan-out carrier board. Peter remembered that the RF inputs on Craig’s boards typically required a minimum signal strength of 0 dBm. Peter also shared that he typically brings RF signals into a PLL clock distribution chip so he could produce different phase locked clocks from the RF input. Duane said that Craig McClure had made another version of this carrier board, last year. This version has a black faceplate.

Duane remembered that Craig McClure has a VME module with a single small board that uses a phase-lock loop to take the Beam Sync signal in and output 53 MHz. Niral is using this board with the Delivery Ring BPM system. This board is not very developed. Peter was not aware of this. Duane said that he knows other places this board is used, but not in any production system.

Peter asked who was going to be supporting these boards in the future. Dan McArthur said that he expects that AD Controls will. Where the money to build things will come from was considered. From my understanding of the Field Work Proposal and Controls being a thrust, I would expect the money to be in the Controls department budget.

Kevin Martin asked about the MDAT transmitters. He is concerned about the spares’ status for these. John said that Greg Vogel manages these, and Mike Kuplic puts them together. This is also a VME carrier board with an IP module.

Next Meeting

There should be a follow-up meeting to get updates as to what spares have been found and ideas and decisions on how the old things will be supported. We could also consider what documentation is available to reference in writing specifications and designing UCDs and TSGs with up to date FPGA’s.

The next meeting has not been scheduled yet.

If you remember something you found important that we should include in these minutes, let me know and I will add it.