Digital Notch Filter Operating Manual
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The purpose of the digital notch filter is to decrease the total dynamic range occupied by a beam signal from a pickup in a circular accelerator or storage ring. The notches are tuned to harmonics of the beam revolution frequency and track the frequency as the beam is accelerated. The spacing of the notches are tuned to optimize signal level and phase response of the beam modulation frequency, whether for phase modulation (synchrotron motion) or amplitude modulation (betatron motion).

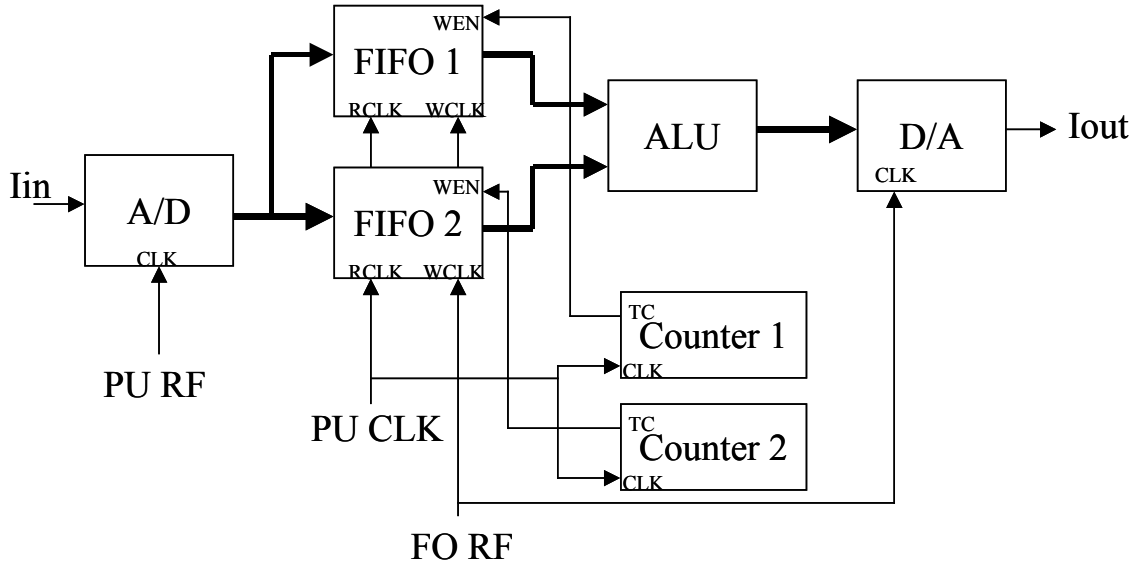


Figure 1: Block diagram of notch filter card.

The digital notch filter consists of one 14-bit digitizer, two 64k-value asynchronous FIFO memories, a 14-bit ALU, one 14-bit DAC, and two counters. The input signal is digitized and loaded into both FIFOs. The FIFOs hold the data for the number of clock tics specified by the counters and then out put their data to the ALU. The ALU performs the desired math function on the data and drives the input to the DAC. The output signal comes from the DAC.

When the card is reset, the FIFOs are set to their proper delays. Data enters the FIFOs immediately after a reset, but the output of each FIFO is disabled until their respective counters have completed their countdown. The countdown value of each counter is set by the user and is loaded into the counters on a reset.

I/O Description:

PU RF – Input – This signal acts as the clock for the A/D. There is a comparator at the front end of this input, so the input signal must have zero crossings to affect a trigger. Either an RF waveform, or an AC coupled square wave will work. The specifications of

the A/D limit the clock frequency to a 10MHz minimum. The PU RF input can be run asynchronously with the PU CLK input, but this is not recommended due to possible timing conflicts. The PU RF can be a multiple of PU CLK without timing conflicts.

PU CLK – Input – This signal provides the clock triggers for the input of the FIFOs and the countdown counters. There is a comparator at the front end of this input, so the input signal must have zero crossings to affect a trigger. The PU CLK input is meant to run asynchronous with the FO RF input. There is a region where the phase between the two clocks can cause the delay to be indeterminate by a clock pulse. If the FO RF leads the PU CLK by 3ns, there is no indeterminacy.

FO RF – Input – This signal provides the clock triggers for the output of the FIFOs and the DAC. There is a comparator at the front end of this input, so the input signal must have zero crossings to affect a trigger.

RESET – Input – TTL input that clears the FIFOs and restarts the delay counters. Expected pulse width between 10-100_s. The card must be reset after power up and should be reset every time the clocks are interrupted.

Iin – Input – Analog input of delay card.

Iout – Output – Analog output of delay card.

On Board Controls:

Fifo delay count 1 – The switch banks S1 and S2 control the least significant byte and most significant byte of the first fifo delay counter preset respectively. This value sets the number of clock cycles stored in the fifo to maintain the proper delay of the card. The actual value of the delay is the value plus 3 clock ticks due to latencies in the system. A bit is logic high when the switch is set “ON”.

Fifo delay count 2 - The switch banks S3 and S4 control the least significant byte and most significant byte of the second fifo delay counter preset respectively. This value sets the number of clock cycles stored in the fifo to maintain the proper delay of the card. The actual value of the delay is the value plus 3 clock ticks due to latencies in the system. A bit is logic high when the switch is set “ON”.

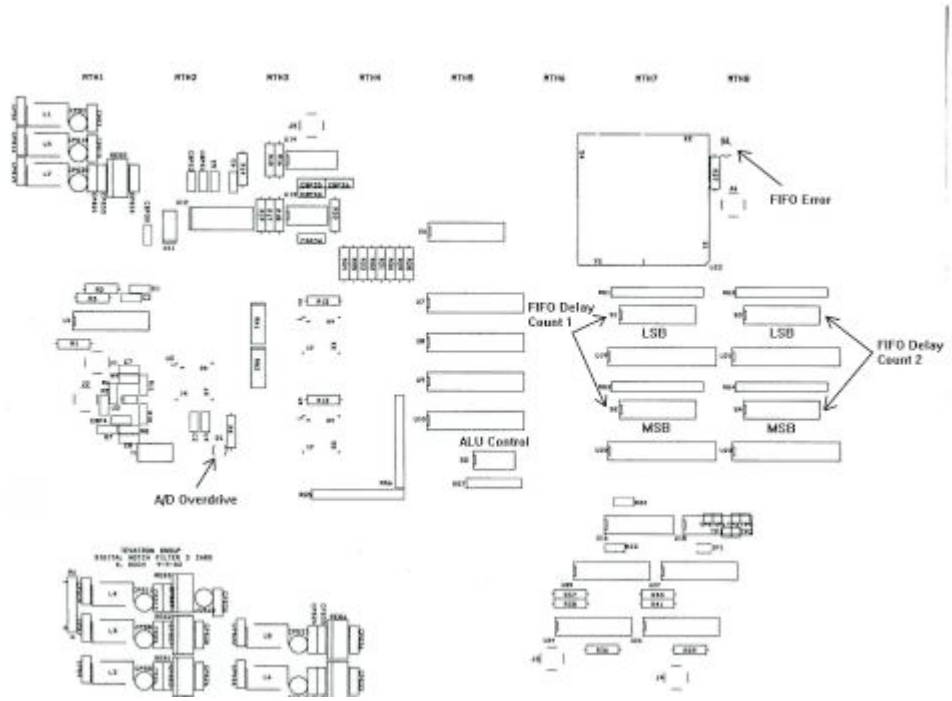
ALU control – The switch bank S5 is the control for the ALU on the card. Switch #4 on the bank is the carry input. This should be set high for any subtraction functions to perform proper twos complement subtraction. The ALU functions for switches 1-3 are shown below. Switch #3 also disables the second fifo by setting its output to high impedance. The outputs are pulled high so that the logic “AND” function allows the first fifo data through without alteration. This is useful for delay measurements when the notch is not desired.

S3S2S1	000	001	010	011	100	101	110	111
Function	Clear	B-A	A-B	A+B	A’	Preset	A	Preset

Table 1: ALU logic functions for switch settings. A refers to fifo1 and B refers to fifo2. S3 disables fifo2.

Fifo Error – The LED D2 activates when any fifo sets its empty flag or full flag. This light should not be active unless there is a problem with the fifo or one of its clocks.

A/D Overflow – The LED D1 activates when the A/D is driven beyond its digital range.



Absolute Maximum Ratings:

Iin	±2.5V
FO RF, PU CLK, PU RF	±5V
Reset	-2V to 7V

Electrical Characteristics:

Iin

Input Voltage Range[1]	±1.0V
Input Resistance	50_
Max Bandwidth	250MHz

[1] The A/D range specification is the full 14bit range of the digitizer. The ALU has no overflow protection, so if a math function requires more than 14 bits for a result the DAC will cut off the MSB.

AC Coupled Roll-off	20kHz

Clock Inputs

Input Voltage Range	-2.5V to 5V
Input Resistance	50_
Operating Point	700mV p-p
Max Frequency with notch	40MHz
Max Frequency w/o notch	65MHz

Reset

Input Level	TTL
Input Resistance	High Z
Pulse Width min	100ns