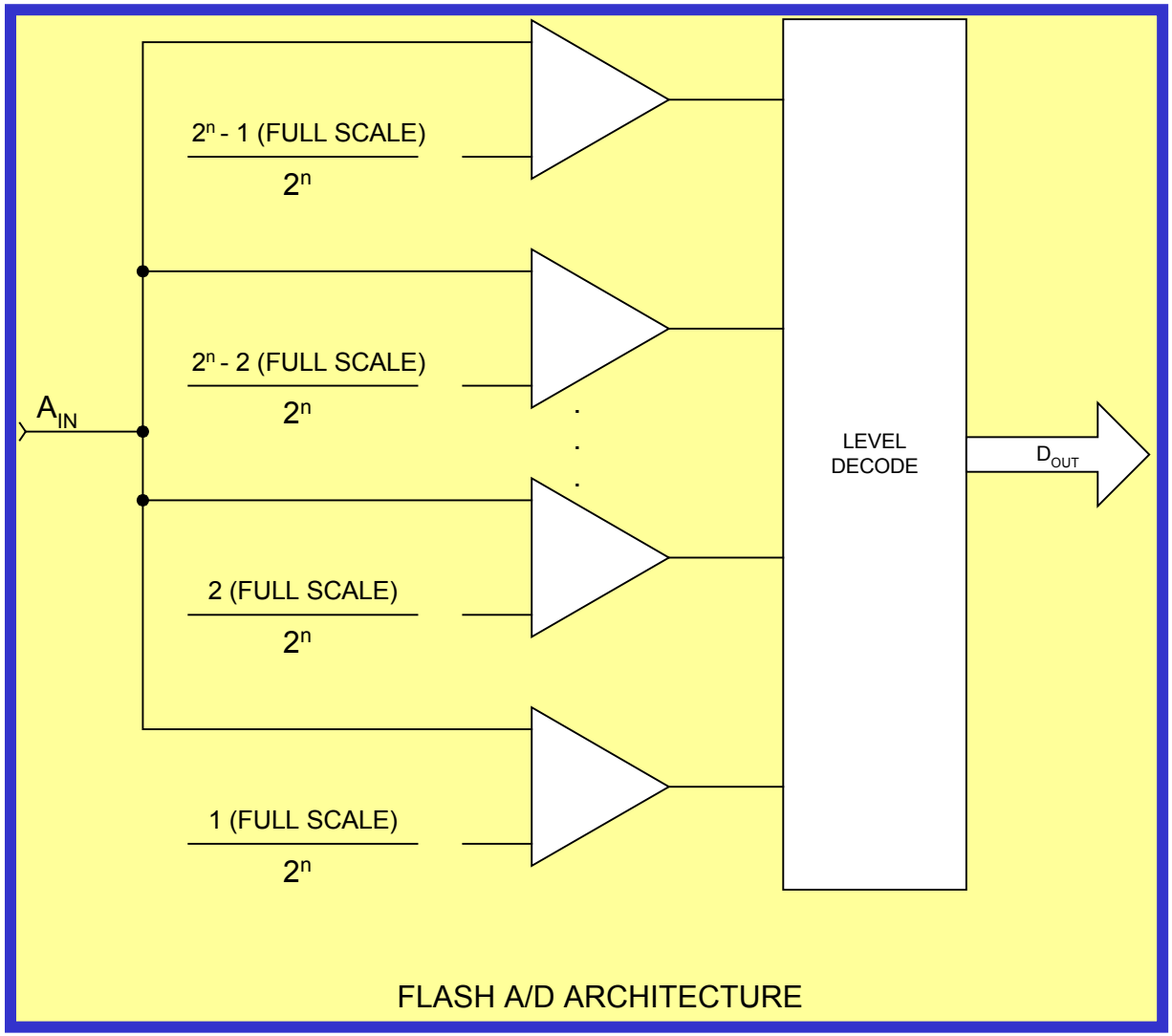
FAST DIGITIZATION AND DIGITIAL RECEIVER TECHNOLOGY

INTRODUCTION

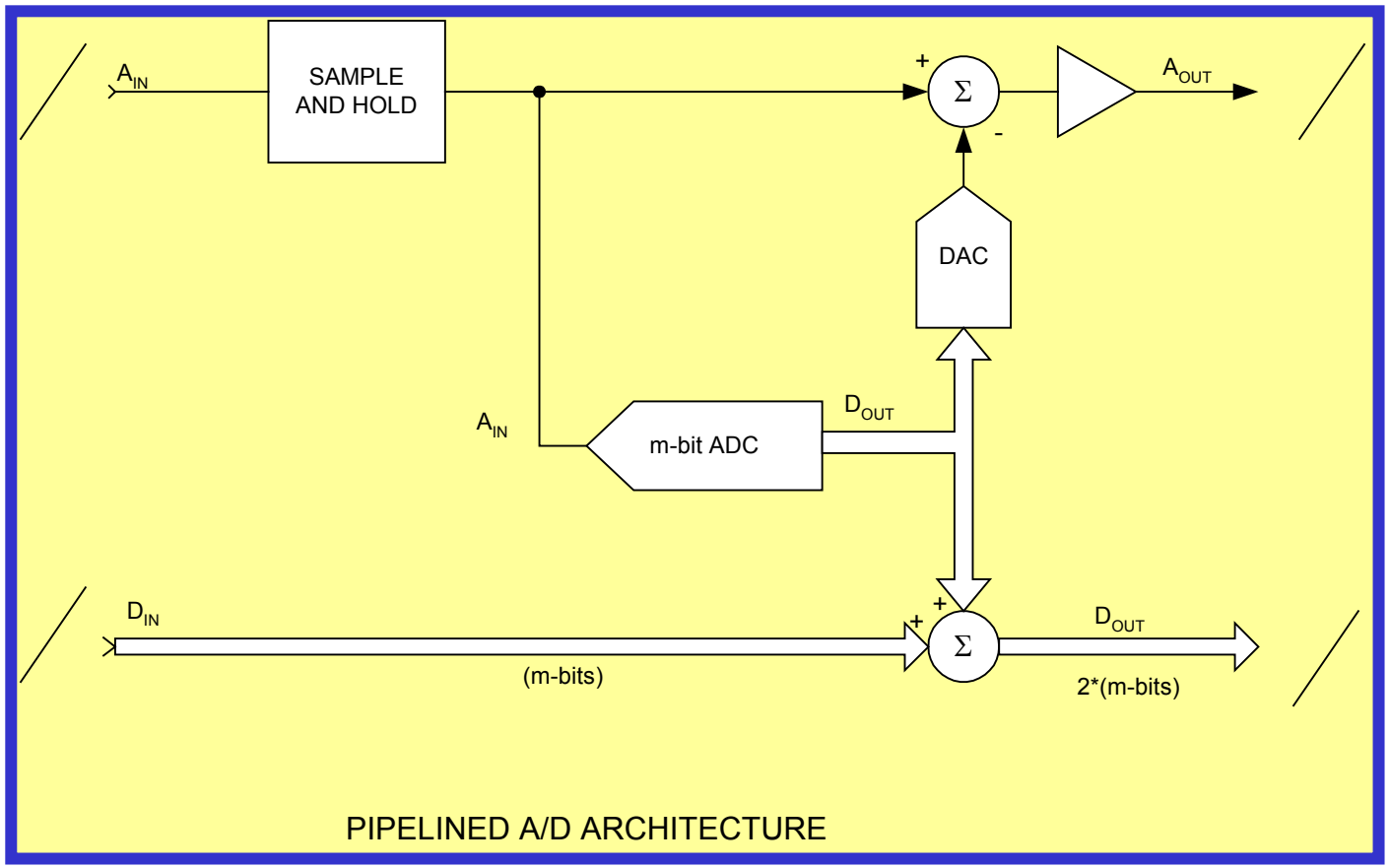
A/D CONVERTER ARCHITECTURES

ECHOTEK CORP.



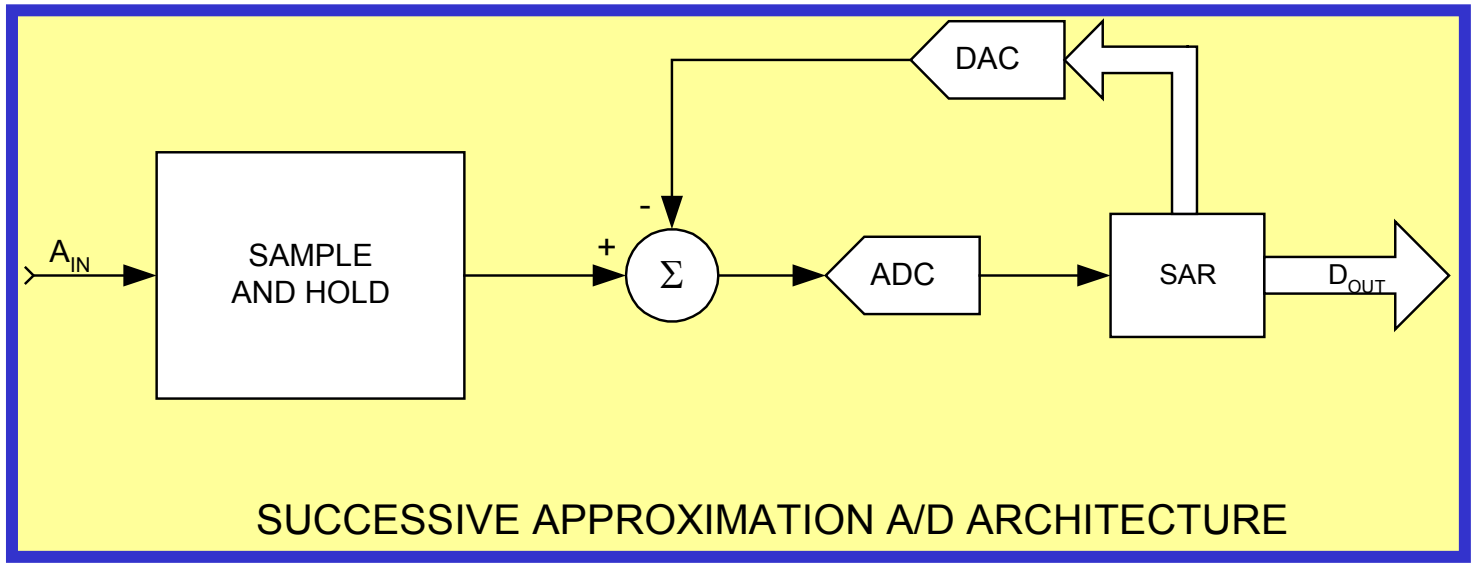
FLASH A/D ARCHITECTURE

ECHOTEK CORP.



PIPELINED A/D ARCHITECTURE

ECHOTEK CORP.



SUCCESSIVE APPROXIMATION A/D ARCHITECTURE

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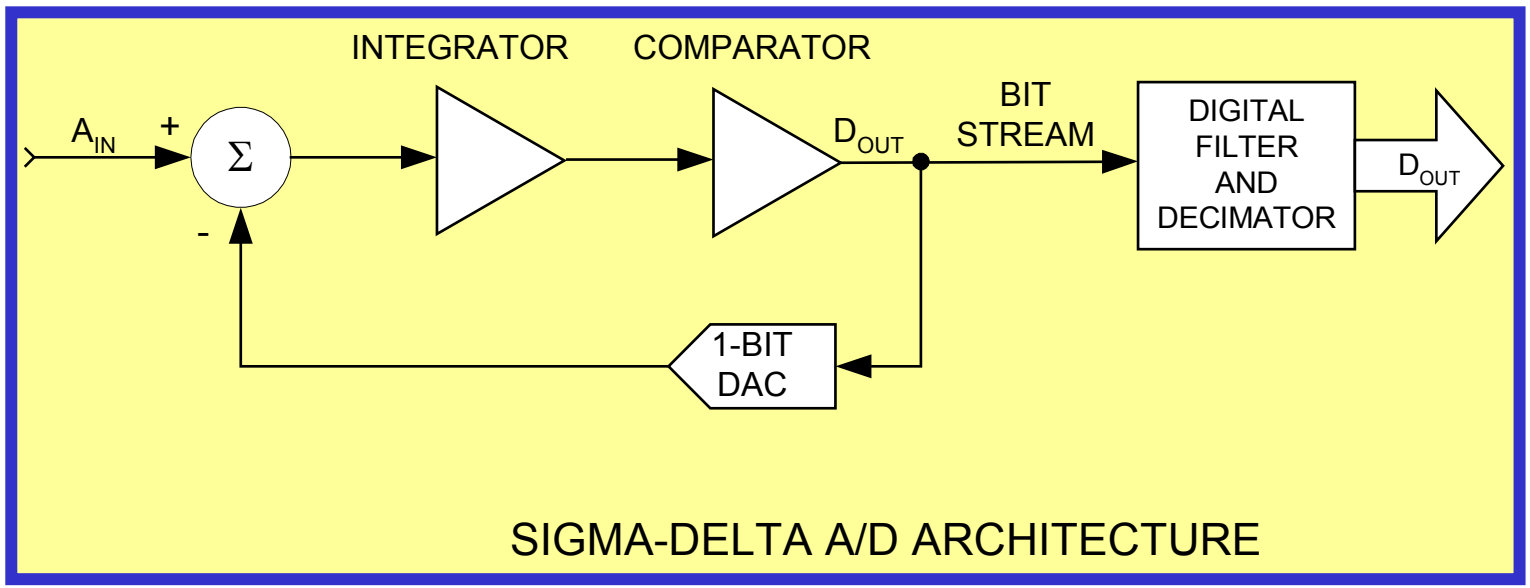

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A/D SPECIFICATIONS

Signal-To-Noise Ratio (SNR or S/N)

rms Signal to rms Noise

Quantization Error = $V*LSB/\sqrt{12}$

rms Signal = $0.5\ V/\sqrt{2}$

$SNR = 2^n\sqrt{3}/\sqrt{2} = 1.225*2^n$

$SNR_{db} = 20\ Log\ (2^n\sqrt{3}/\sqrt{2})$

$SNR_{db} = 20\ Log\ (2)*n + 20\ Log\ (\sqrt{3}/\sqrt{2})$

$SNR_{db} = 6.021*n + 1.763\ (dB)$

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Dynamic Range (DR)

Signal-to-Noise And Distortion (SINAD)

Effective Number of Bits (ENOB)

$$\text{ENOB (bits)} = (\text{SINAD} - 1.763)/6.021$$

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Aperture Uncertainty (Jitter)

Seconds rms

$SNR = -20 \text{ Log } (2\pi F_{in} * T_{au})$

For $T_{au} = 0.25$ ps rms

$F_{in} = 10$ MHz, SNR = 96 dB

$F_{in} = 100$ MHz, SNR = 76 dB

$F_{in} = 500$ MHz, SNR = 62 dB

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Spurious-Free Dynamic Range (SFDR)

Amplifier SFDR = 2/3(P1-P0-10Log(BW)-NF)

P1 = IP3 - GAIN

PO = Input Noise Power (-114 dBm, 50 Ohms)

BW = Bandwidth in MHz

NF = Noise Figure

Example:

SFDR = 2/3(+38-16-0-114+4) = -88 dB

A/D SFDR = rms signal to peak spurious component

A/D SFDR can be > ideal SNR

Dither Noise for Better SFDR

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Processing Gain

- Frequency Domain
  - Gain = 10 Log (number of points) Complex
  - Gain = 10 Log (number of points/2) Real
- Time Domain
  - A/D Integrated Noise Is Constant
  - Increasing Sample Rate Lowers Noise Per Sample
  - Gain = 10 Log (Decimation)
- Filter Design Can Give Slight Increase
- There Is A Limit To The Passband Noise Floor
- Correlated Digital Sample Noise Floor

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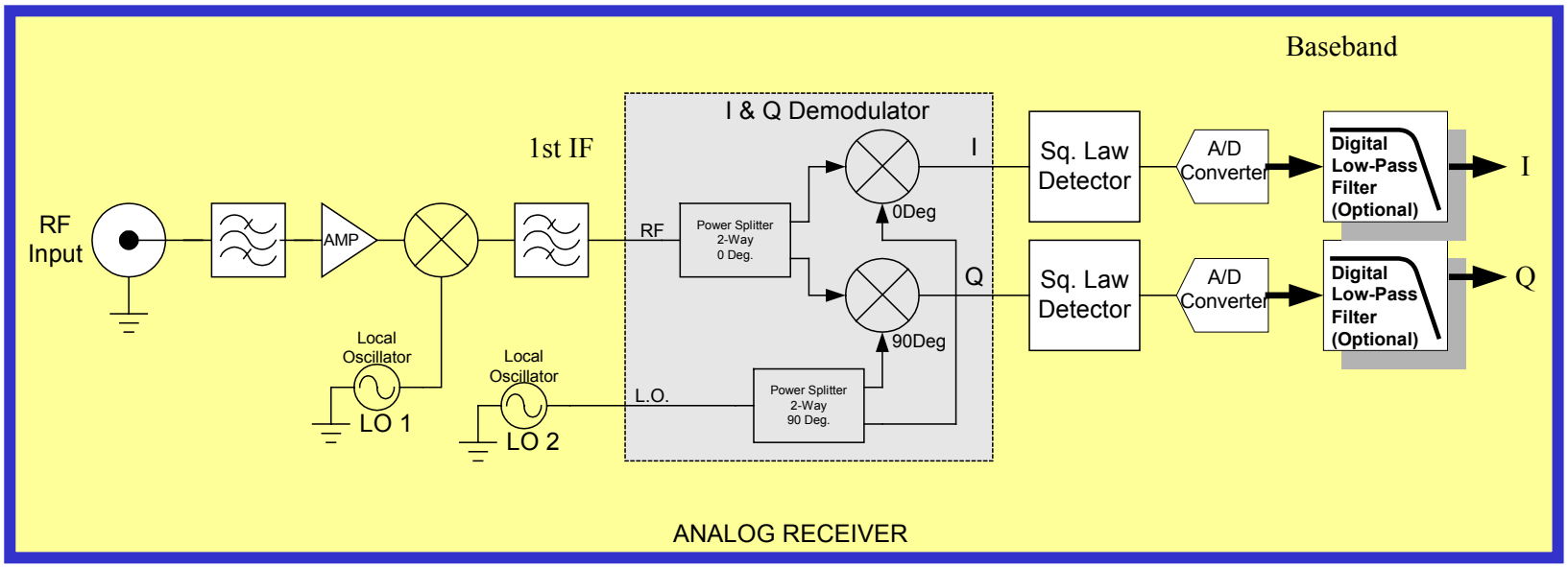
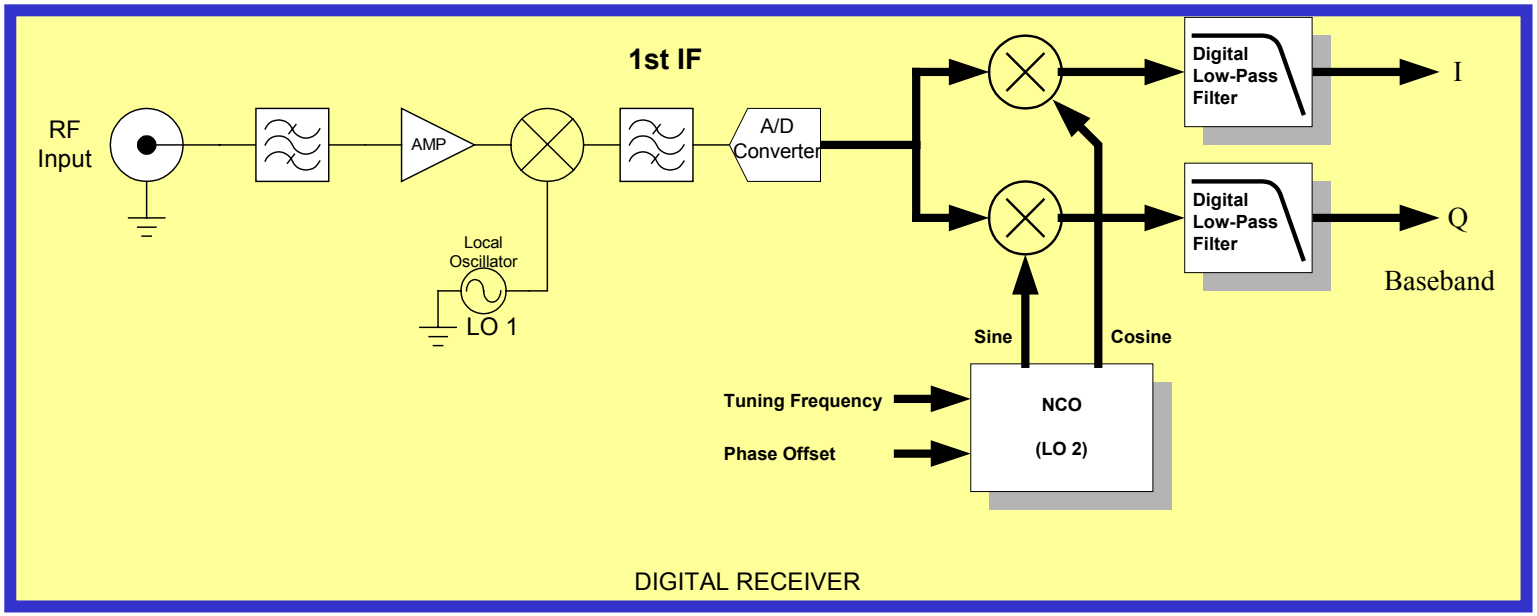
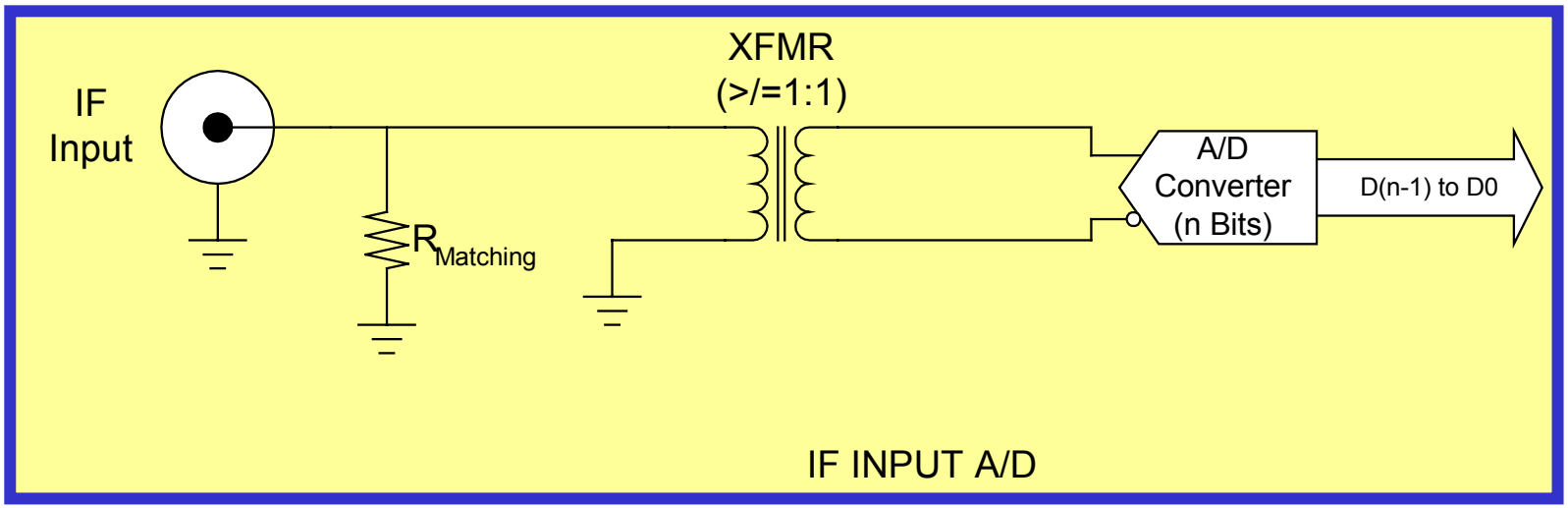


ECHOTEK CORP.



ECHOTEK CORP.



Digitization Requirements

Band-Limited

Headroom

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Digital Mixing

Fs/4 Up/Downconversion

$I(t) = A(t) \text{ consine } (2\pi F(t))$
$Q(t) = A(t) \text{ sine } (2\pi F(t))$
0° - 90° - 180° -270°

Consine Sequence
1 0 -1 0

Sine Sequence
0 -1 0 1

Fs/2 Spectral Inversion (1, -1)

Numerically Controlled Oscillator (NCO)

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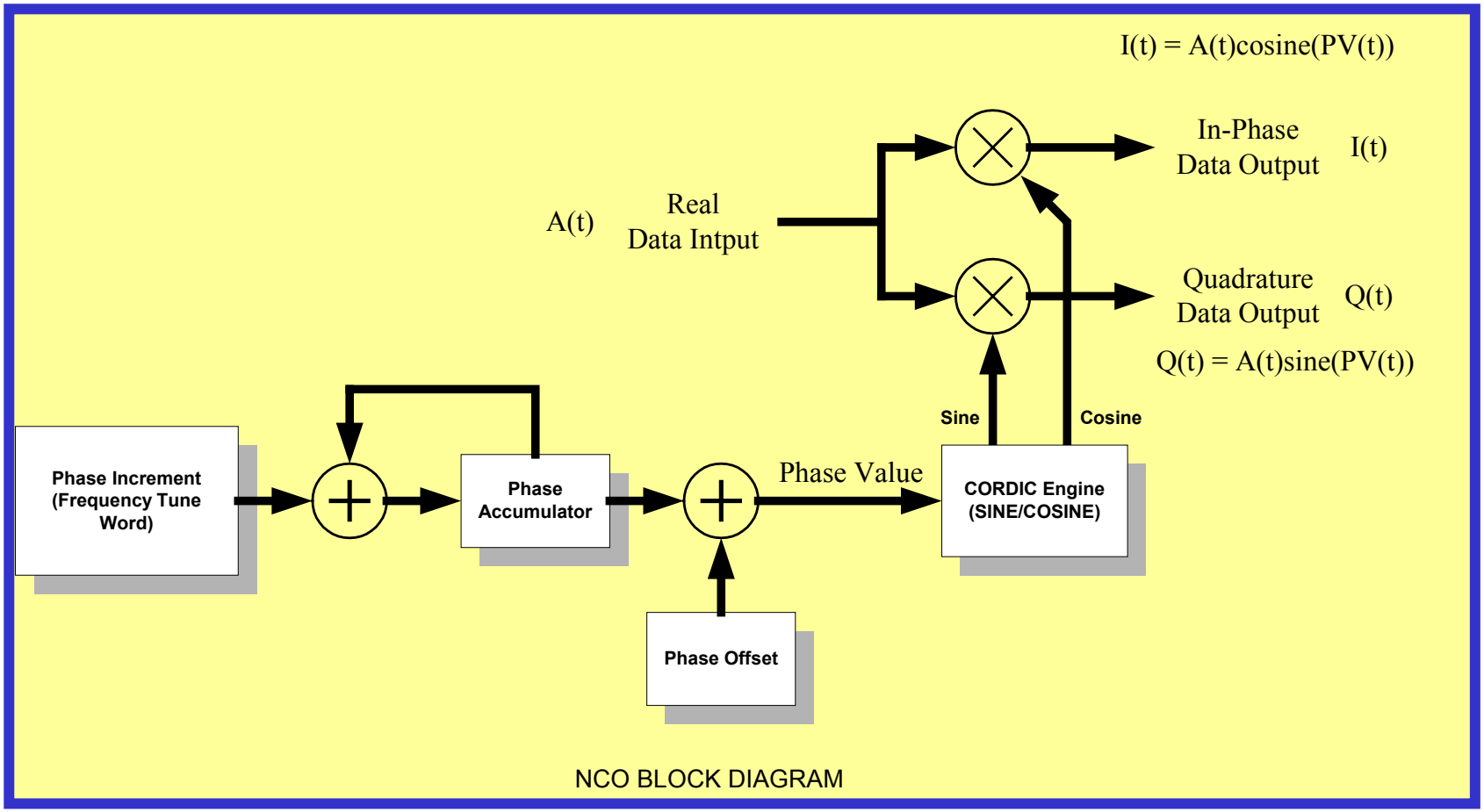

NCO BLOCK DIAGRAM

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CORDIC Precision

Clock Rate (LO Frequency)

Multipliers (18 x 18)

Interleaved NCO's

I(t) and Q(t) Filtering

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Digital Filtering

- CIC (High Decimations)
- FIR (Sharp Response)

Commercial Digital Receiver Chips

- Analog Devices
- Graychip (TI)
- Harris (Intersil)

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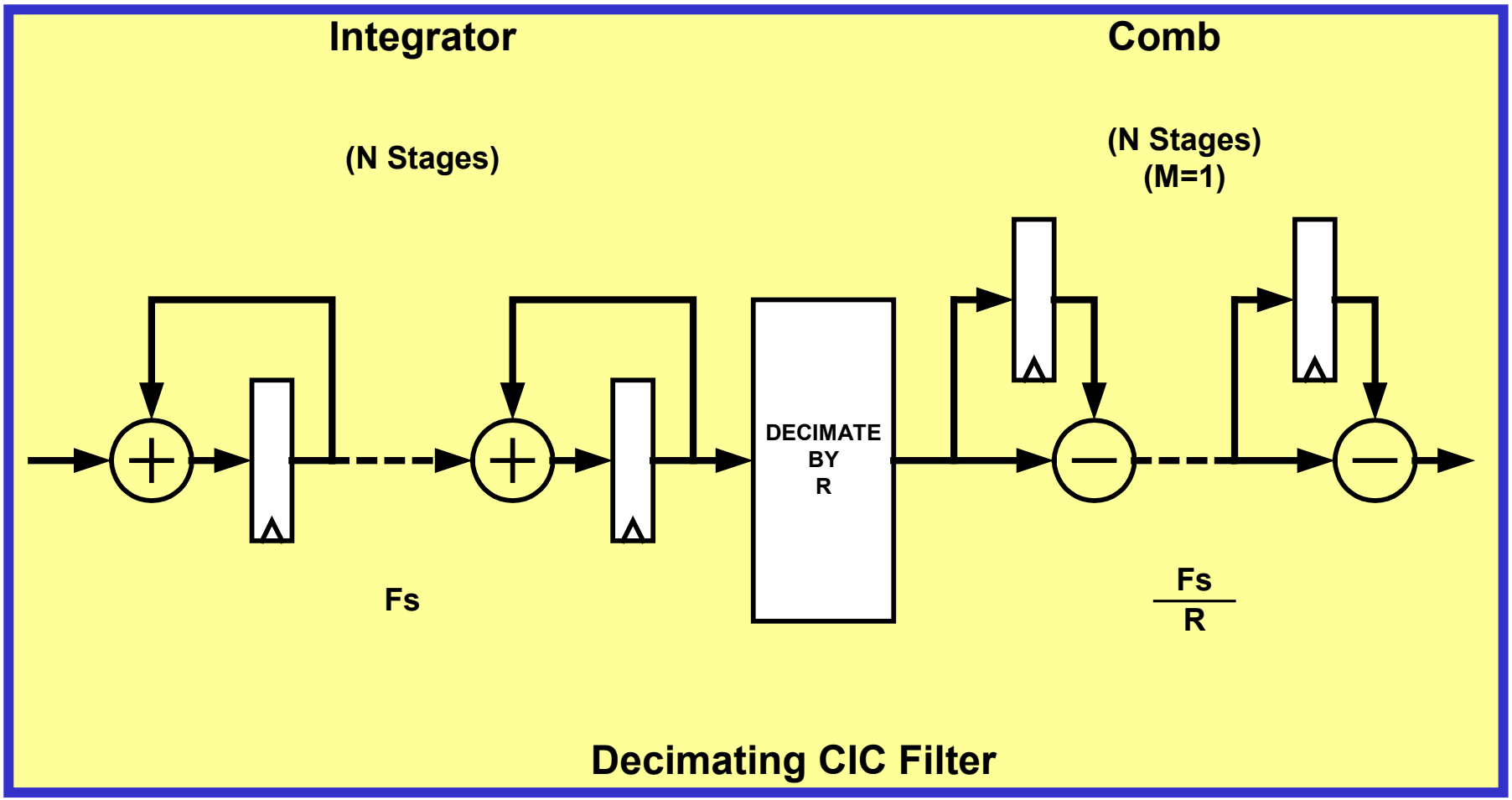

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CIC Response (Decimating)

Magnitude Squared $P(f) = (1/(M*R)^N)^2 \text{ sine } (\pi MfR/fs)/\text{sine}(\pi f/fs))^{2N}$

fs = input sample rate

R = decimation

f = input frequency

Often Plotted Normalized to $f_{out} = fs/R$

$P(f) = (\text{sine}(\pi Mf)/\text{sine}(\pi f/R))^{2N}$

P(f)dB = 10 Log (P(f))

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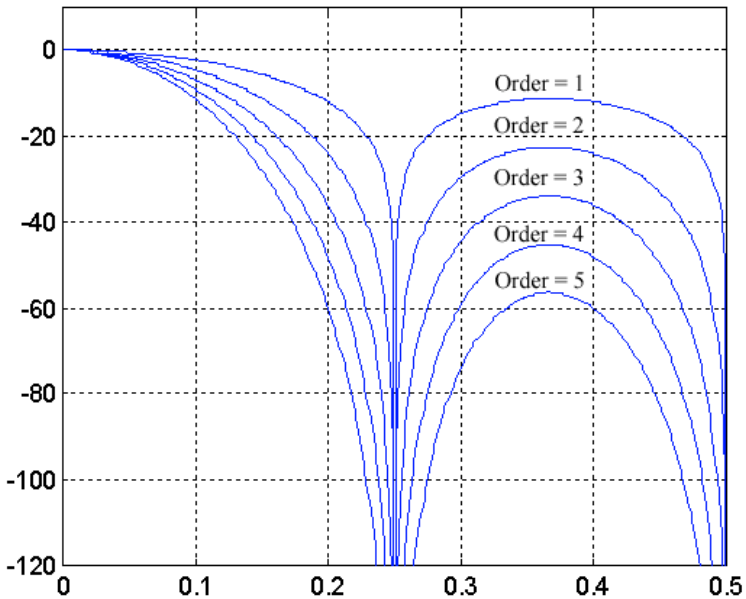
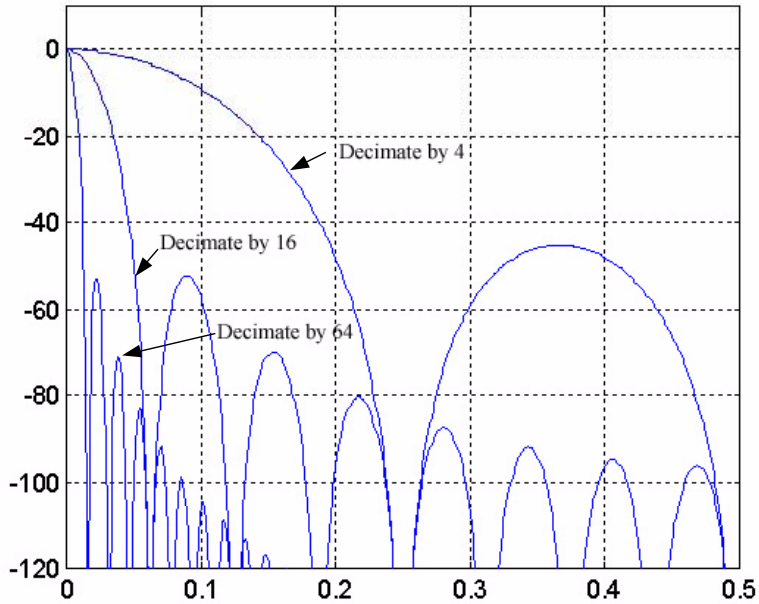
CIC RESPONSE



Decimate by 4, Varying Order



Varying Decimation, Order = 4

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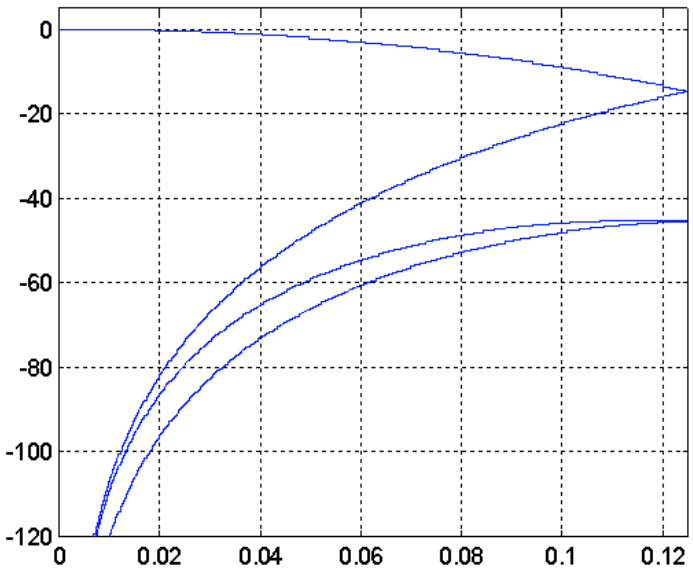
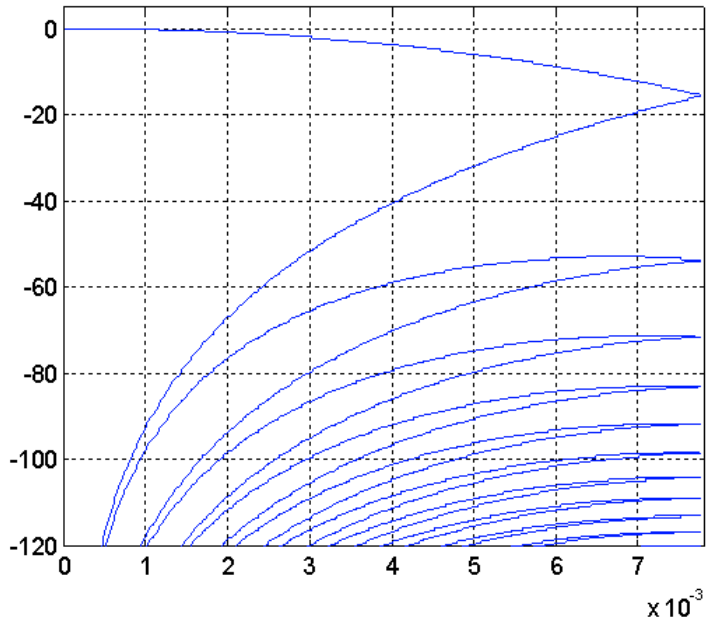
CIC ALIAS REJECTION



Order = 4, Decimation = 4



Order = 4, Decimation = 64

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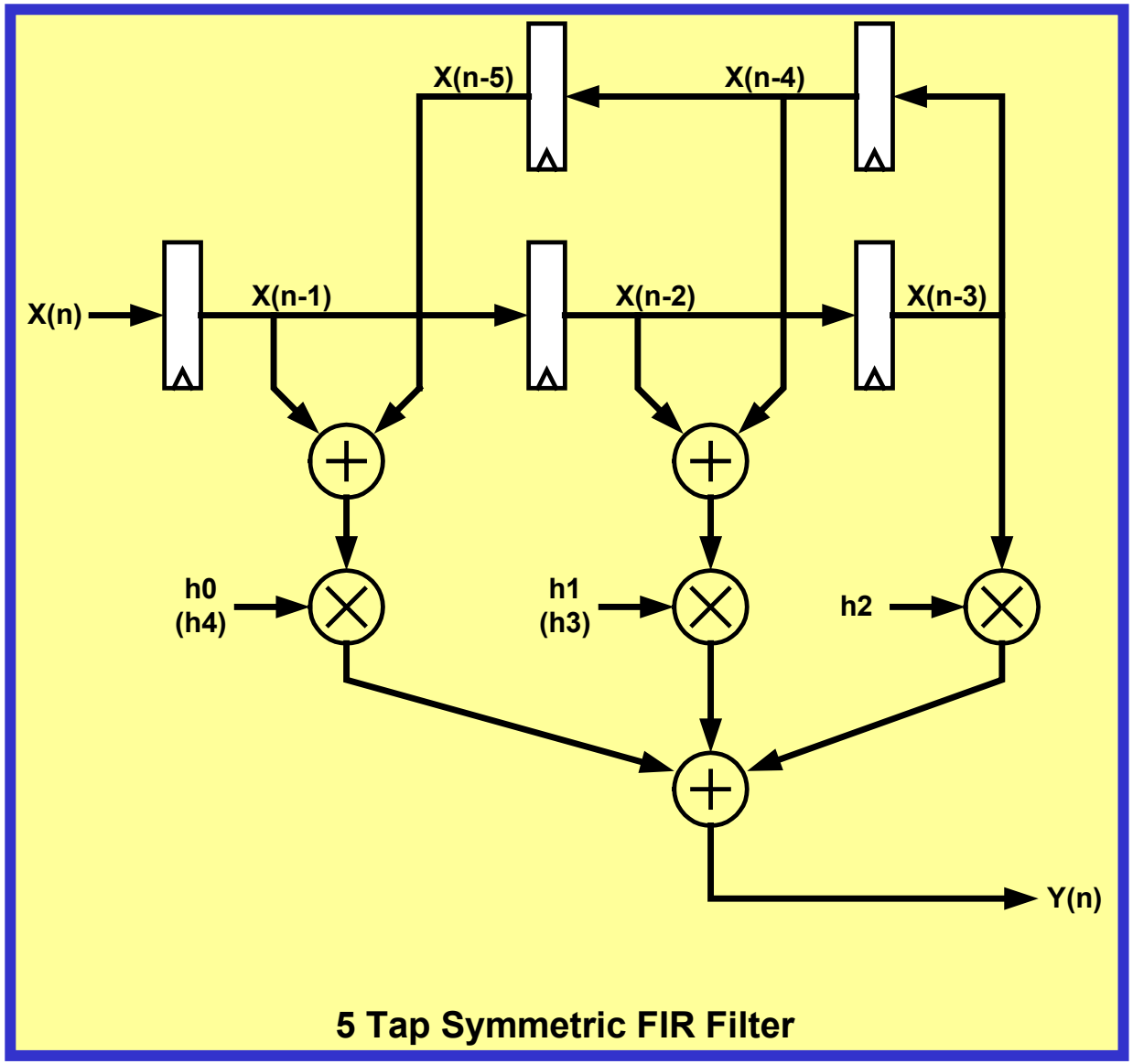
FIR Filters

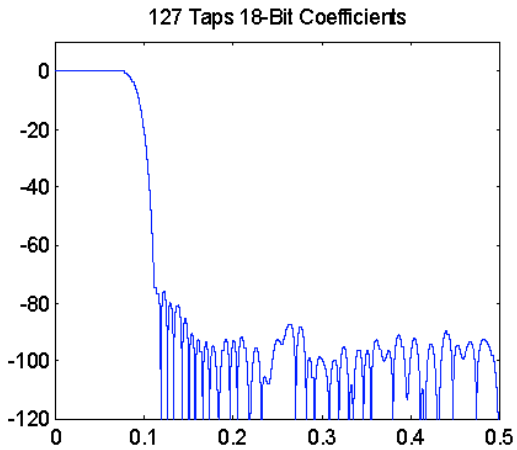
Transversal Filter Equivalent
Sharp Response
Number of Taps
Numerical Precision
Polyphase
Fully Parallel
Symmetrical Coefficient FIR is Phase Linear
Window Functions (Blackman, Hamming, etc.)
Remez (Parks-McClellan)

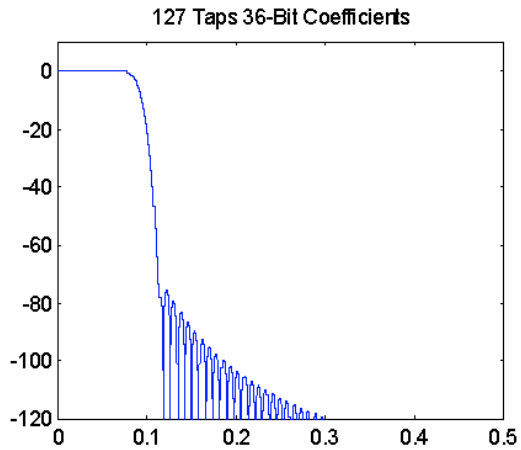
ECHOTEK CORP.

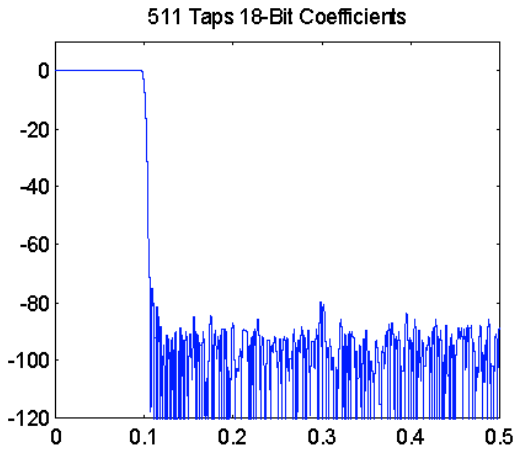


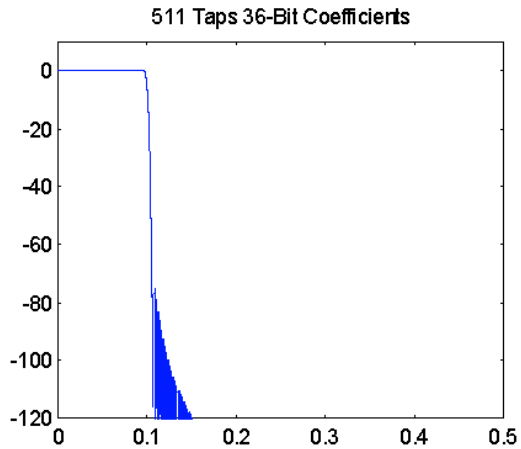
5 Tap Symmetric FIR Filter

FIR BLACKMAN



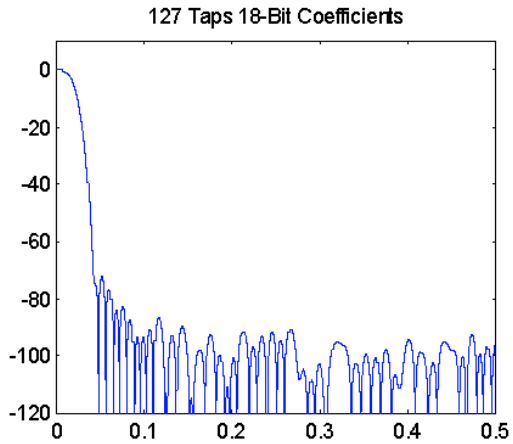


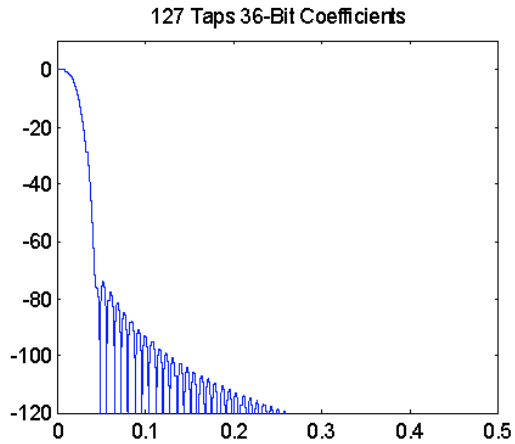


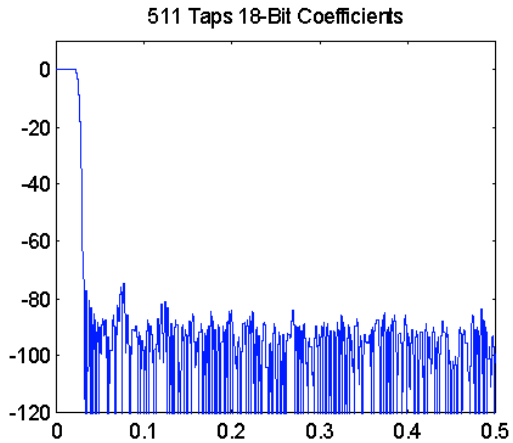


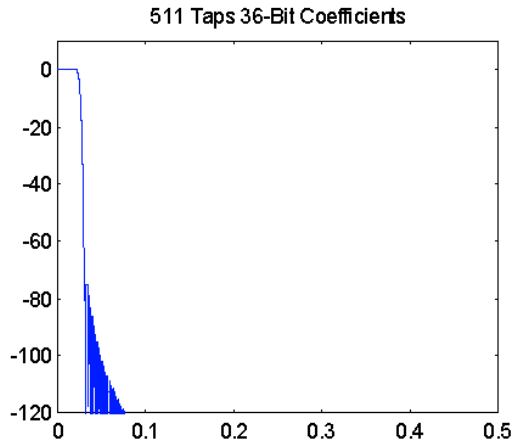
Decimate by 4

FIR BLACKMAN









Decimate by 16

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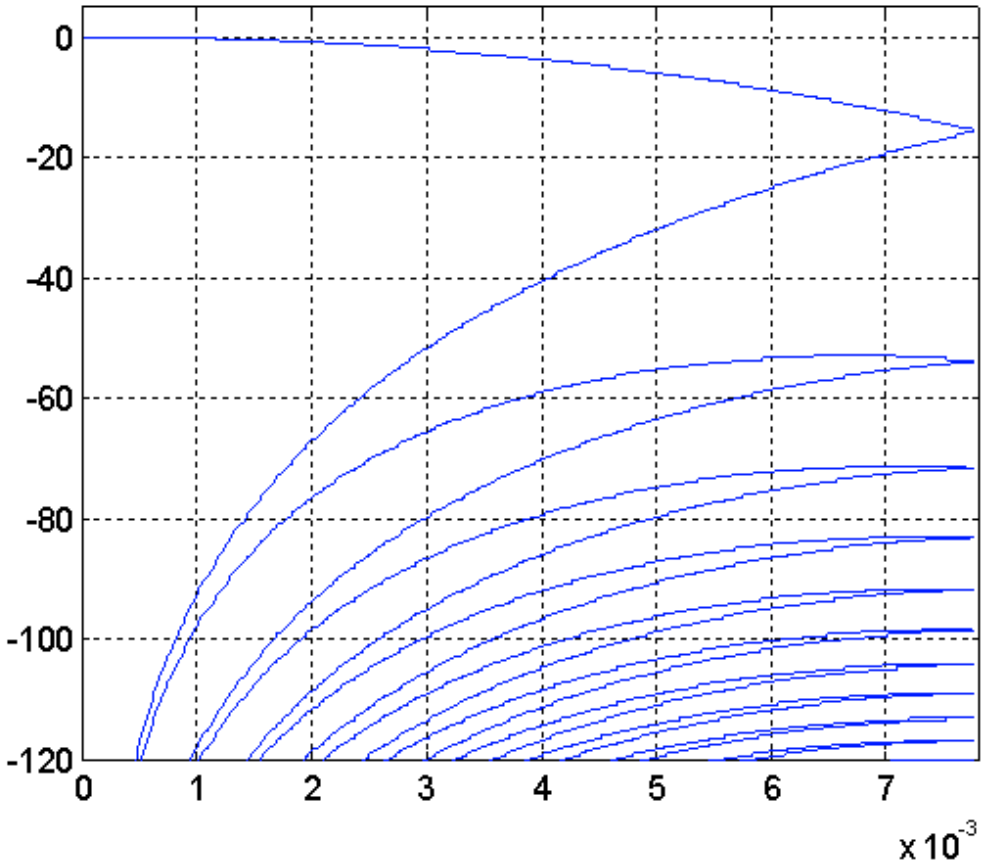
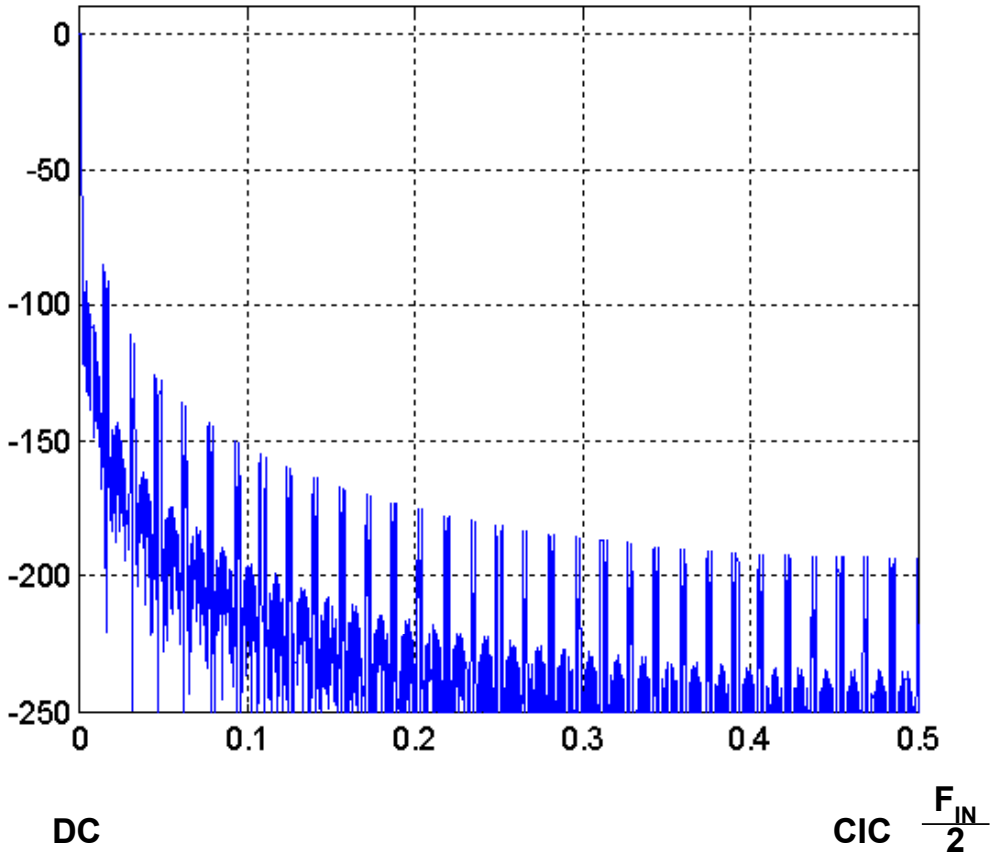
CIC ALIAS REJECTION

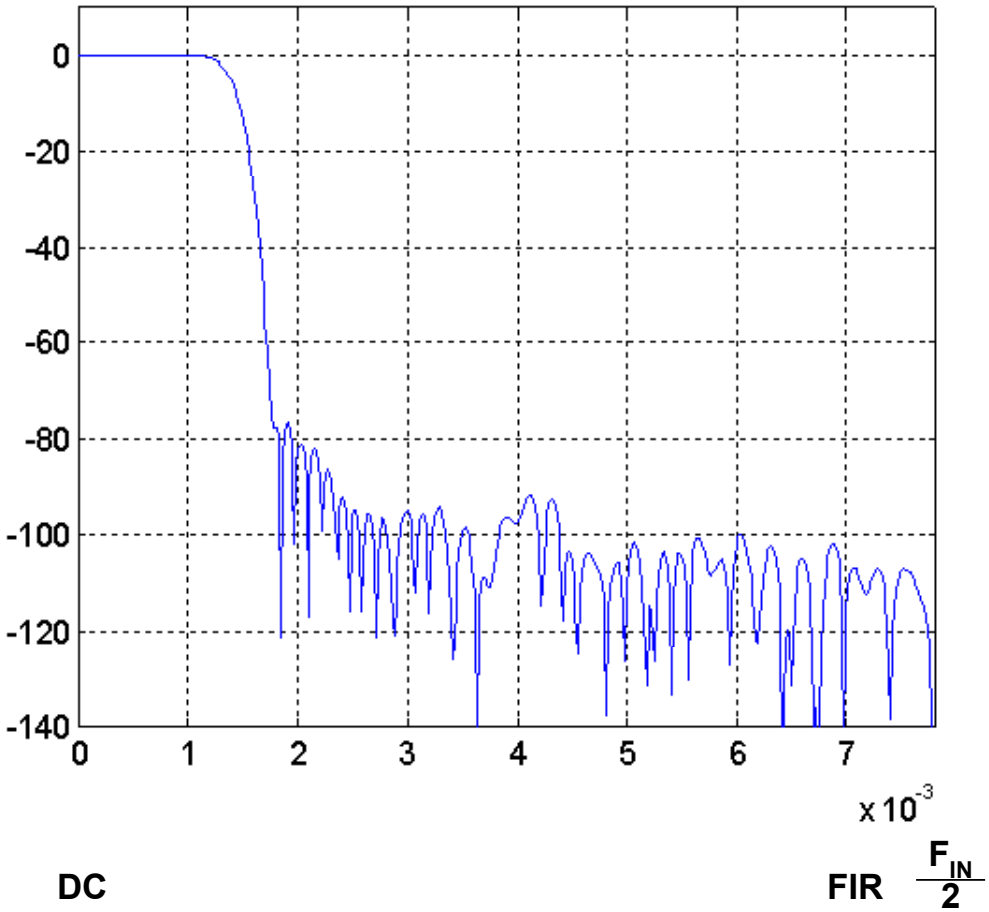


Order = 4, Decimation = 64



CIC (Order 4, Decimate by 64) with 127-Tap FIR, Decimate by 2
(18-Bit Coefficients, Decimate by 4 Design)

ECHOTEK CORP.



CIC (Order 4, Decimate by 64) with 127-Tap FIR, Decimate by 2
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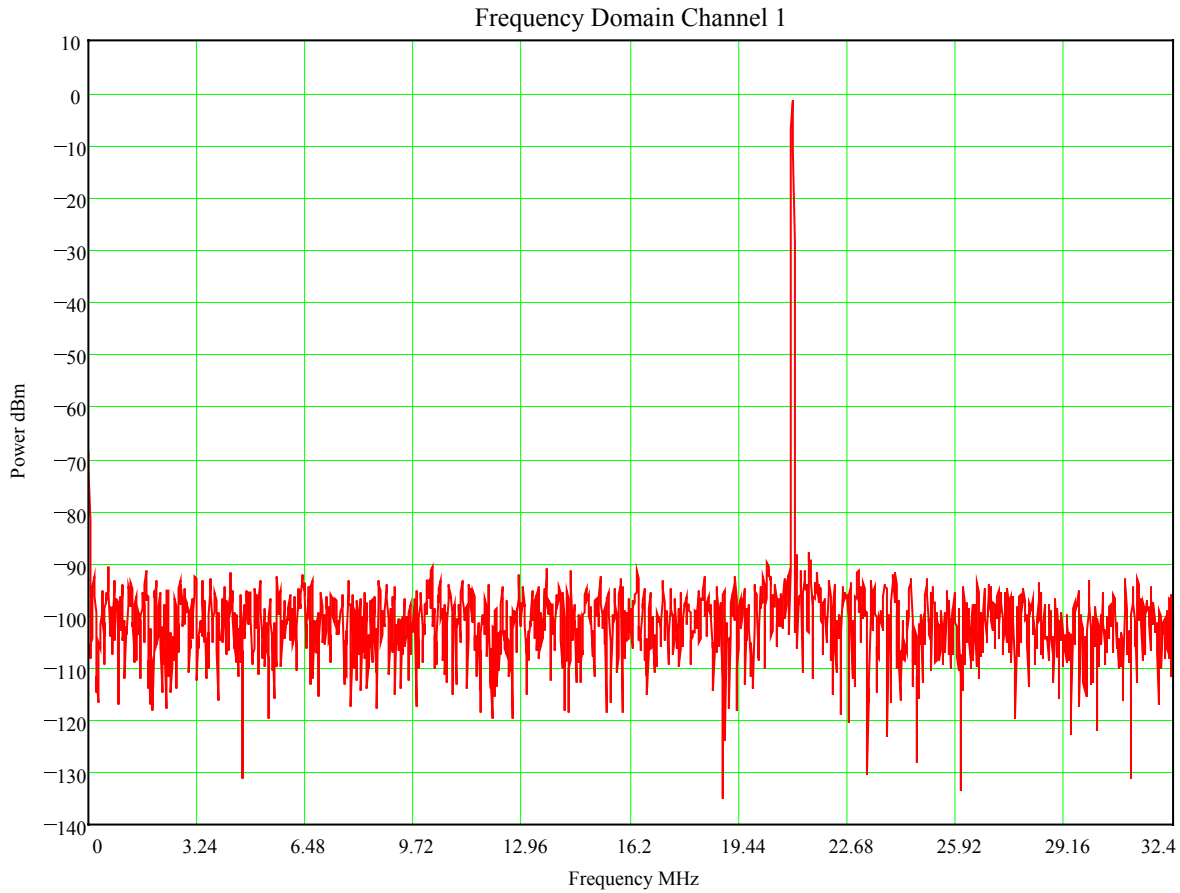
ECHOTEK CORP.



ECDR-GC314-PMC Raw A/D Data

Source: 21.03 MHz. 5.5 dBm @ HP8664A with 20 MHz HPF and 32.4 MHz LPF at Channel 1 Input. Clock: 64.8 MHz. Crystal Oscillator with 60 MHz HPF and 65 MHz LPF. 2048 Point FFT

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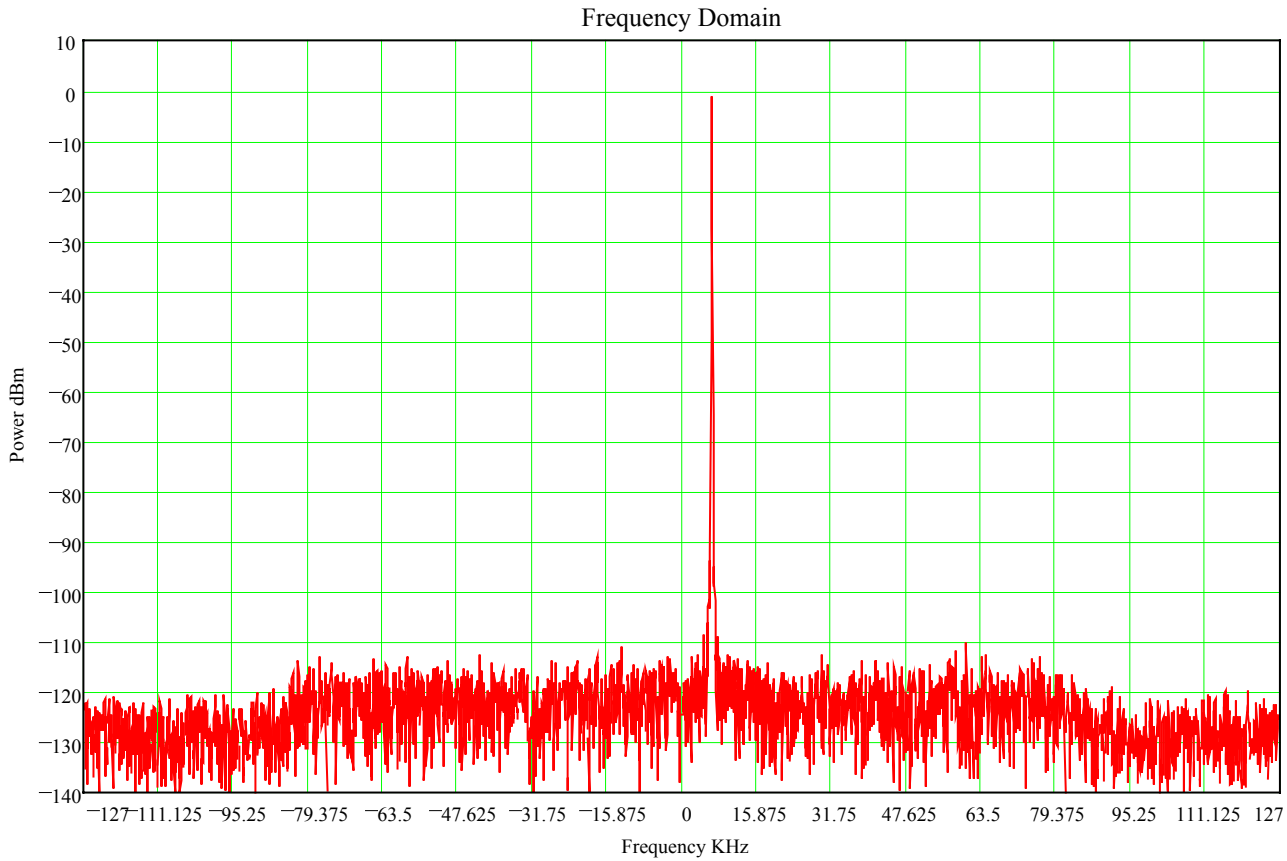

ECDR-GC314-PMC Receiver Data

Source: 21.03 MHz. 5.5 dBm @ HP8644A with 20 MHz HPF and 32.4 MHz LPF at Channel 1 Input. Center Frequency at 21.02355 MHz.
Clock: 64.8 MHz. Crystal Oscillator with 60 MHz HPF.
Receiver Processing Gain = 10Log(256) = 24 dB, 4096 Point CFFT.
A/D S/N (Jitter) = $-20\text{Log}\left(2\pi 21.03\text{x}10^{6}(0.1\text{x}10^{-12})\right) = 97.6$ dB

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Digital Receiver Advantages

Improved Performance
- Reduced Components and Cost
- No Component Tolerance, Frequency or Temperature, etc. Dependence
- Reduced Obsolescence
- Improved SFDR
- Near Perfect I&Q Balance
- Near Perfect Filtering

Application Commonality
- Easily Reconfigured
- Reduced System I/O
- Distributed Processing

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Product Design Considerations

Today's Technology Requirements
- Schematic Capture
  - Component Libraries
  - Parts Footprints
  - BOM
  - Netlist
  - Notes and Documentation

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Board Layout

CAD
Auto-routers
Multi-layer
Vias
Controlled Impedance
Mechanical Considerations
Special Requirements (Mixed-Signal)

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Product Manufacture

PC Board Manufacture

Capabilities Required
Min. Quantities Hole Size, Line Width, Controlled Impedance, Testing, etc.

PC Board Stuffing

Min. Quantities, Component Size, Inspection, Testing, etc.

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Example Beam Instrumentation Product Design

Bunch-by-Bunch Current Monitor
- Include Co-adding

Support Beam Steering

Example Parameters
- F_{RF} = 360 MHz = F_{CLK}
- Number of Bunches = 300
- F_{REV} = 1.2 MHz
- Trigger = Bunch 1
- Four BPMs
- Band-limited Analog Inputs

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Design Elements

A/D: AD9430 (12-bits, >210 MSPS, 700 MHz BW)
- Time-Interleaved Pairs

PECL Clock Logic

Programmable Logic
- Altera Stratix FPGA (One Per Channel)
- In-Circuit Reprogrammable Configuration

Standard Bus Interface (VME, PCI, etc.)

Additional Altera Stratix FPGA
- Beam Steering Algorithms

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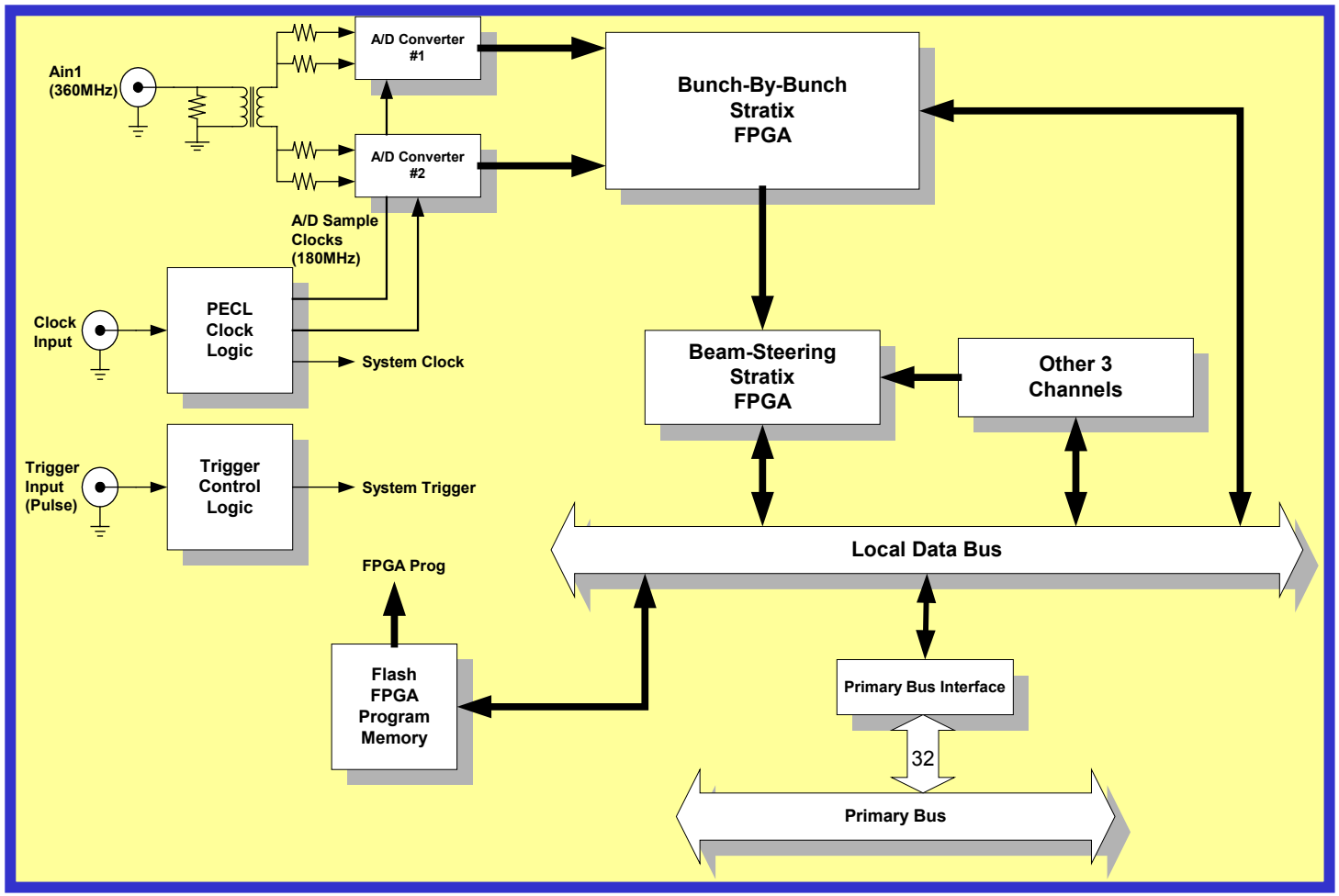

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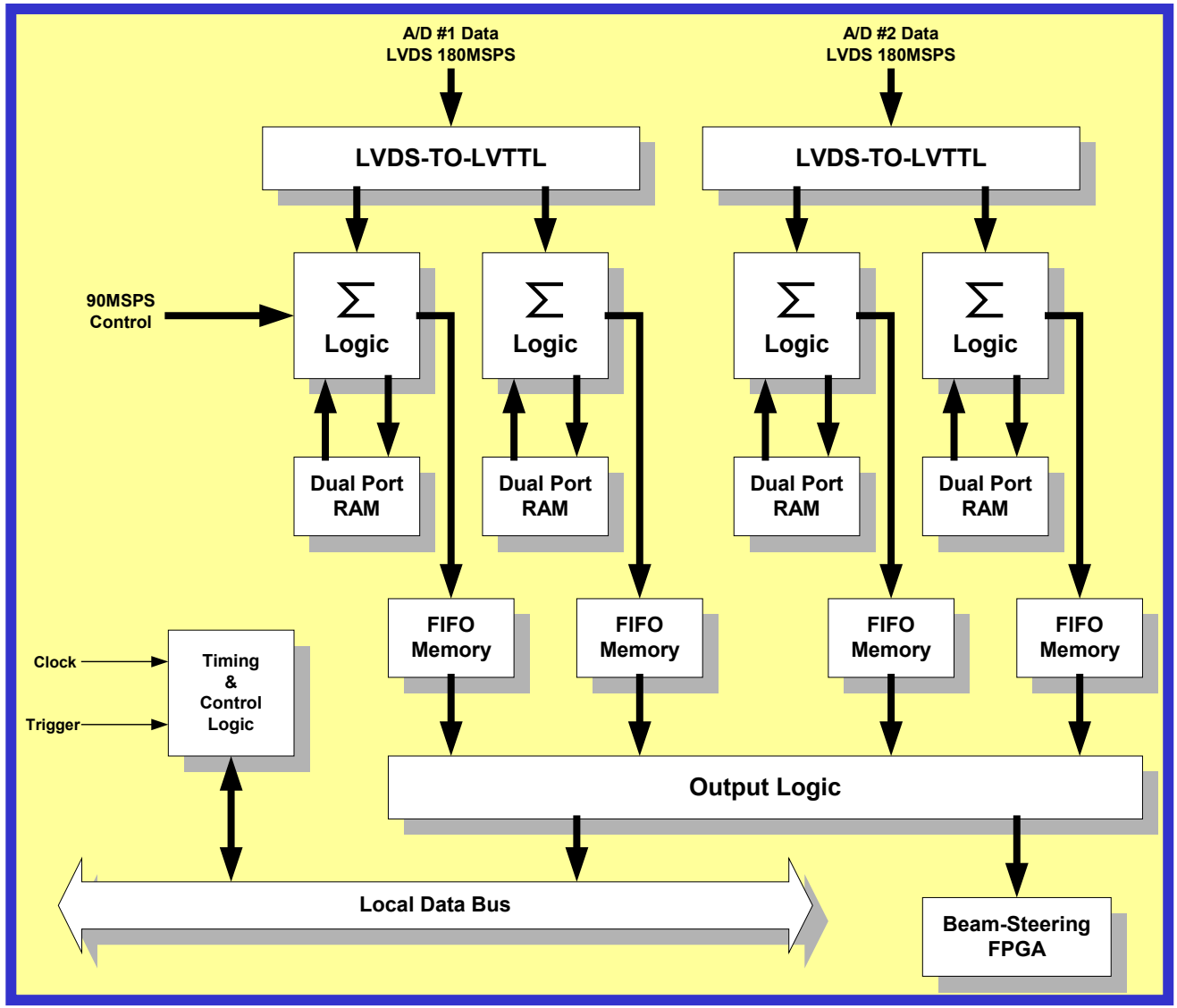

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Other Bunch Data Processing Options

Individual Bunch Filtering
Individual Bunch Digital Receiver (1.2 MHz)
Multi-Bunch Digital Receiver (360 MHz)

Beam Steering Algorithms

Difference-Over-Sum
AM/PM Conversion
Log-Ratio
Stable Beam Suppression

IP Cores

Log, Rectangular-to-Polar, FIR, DFFT, etc.

In-Circuit Programming

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The Stratix Device Family

Device	Logic Elements	32x18 M512 Blocks	128x36 M4K Blocks	4,096x144 MegaRAM Blocks	Total RAM Bits	DSP Blocks
EP1S10	10,570	94	60	1	920,448	6
EP1S20	18,460	194	82	2	1,669,248	10
EP1S25	25,660	224	138	2	1,944,576	10
EP1S30	32,470	295	171	4	3,317,184	12
EP1S40	41,250	384	183	4	3,423,744	14
EP1S60	57,120	574	292	6	5,215,104	18
EP1S80	79,040	767	364	9	7,427,520	22
EP1S120	114,140	1,118	520	12	10,118,016	28

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Package Offerings & User I/O

Device	672-Pin BGA Wire-Bond 1.27 mm 35 x 35	956-Pin BGA Flip-Chip 1.27 mm 40 x 40	672-Pin FBGA Wire-Bond 1.0 mm 27 x 27	780-Pin FBGA Flip-Chip 1.0 mm 29 x 29	1020-Pin FBGA Flip-Chip 33 x 33	1508-Pin FBGA Flip-Chip 40 x 40	1923-Pin FBGA Flip-Chip 45 x 45
EP1S10	341		341	422			
EP1S20	422		422	582			
EP1S25	469		469	593	702		
EP1S30		679		593	726		
EP1S40		679			769	818	
EP1S60		679			769	1,018	
EP1S80		679				1,199	1,234
EP1S120							1,310

Vertical Migration Supported