

ANALOG BOX DESCRIPTION

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1.0 INTRODUCTION

This document describes the Analog Box portion of the Beam Position Monitor system (BPM) for the Fermilab Energy Doubler. The Analog Box is the hardware that resides between the RF Modules and the Multibus hardware. For a general description of the BPM system see Operations Bulletin #888, FERMILAB ENERGY DOUBLER BEAM POSITION MONITOR SYSTEM, Rod Gerig, 7/82.

The initial section of this document describes the Analog Box from the perspective of a block diagram. The next section builds on the block diagram description but provides a circuit description.

Throughout this document signal names will be followed by a slash (/) if the signal is logically true at a TTL "0" state. For instance SNEN/ means that SNApshots are ENabled when this signal line is at a TTL level of 0 volts. A signal line will be called Asserted or Active when it is logically true. To negate a signal means to make it logically false.

2.0 BLOCK DIAGRAM DESCRIPTION

The Analog Box contains two major circuits. One of these is the daughter card of which there is one for each detector. The second is the mother board of which there is one per Analog Box.

2.1 Analog Box Daughter Card

Refer to Fig. 1. The position and intensity signals from the RF modules are sent directly to each daughter card. The purpose of the daughter card is to provide a computer readable value of these signals at card edge, measured in a beam triggerable manner. To do so it must:

- o Provide a means of arming and disarming the trigger circuit.
- o Provide a trigger circuit with a variable intensity threshold, that produces a gate for the S/H.
- o Contain fast gatable Sample and Hold (S/H) amplifiers for both position and intensity signals.
- o Make sure that the processor is informed if the trigger circuit falsely triggered.
- o Provide circuits for getting the analog voltage in the correct range for the Analog to Digital Converter (A/D). In the case of the intensity signal this includes transforming the voltage, which is linearly proportional to the intensity, into a signal with a logarithmic response.
- o Provide a fast A/D which upon command will digitize either position or intensity.
- o Provide a means of reading out the desired value, either position or intensity.

2.1.1 Daughter Card Arming - The arming of the daughter cards is under control of the mother board with the ARM/ and DISARM/ pulses being bussed to all cards simultaneously. The S/H gate generator will disarm the card at the leading edge of the gate to prevent further triggering. The FLAG signal (FLASH Gate) must be asserted (which it always is during Snapshots) to arm the daughter card. Whenever FLAG is not active the daughter card is disarmed, regardless of the state of the ARM/ and DISARM/ lines. More will be said about the origin of these control lines in the description of the motherboard.

2.1.2 Daughter Card Triggering And Gate Generation - At the heart of the triggering circuit is a comparator which receives intensity signal at one input and a settable threshold at the other. A portion of the logical output is fed back to the threshold input to provide stability at intensities near the threshold voltage. The output of the comparator called BIP/ (Beam Is Present) is sent back to the motherboard, but more importantly, its leading edge triggers the gate generator. The duration of the gate depends on the choice of modes. If batch mode is selected the gate will be 200 nanoseconds, and if bunch mode is selected, 40 nanoseconds. The gate generator has the responsibility of reporting on the validity of the measurement. It does this by setting a line,

THAGL/ (Track and Hold Amplifier Gate Latch) which when active indicates that BIP/ was active throughout the gate. In other words the intensity must be greater than the threshold level during the entire gate for THAGL/ to be asserted. The motherboard sends a pulse, ACLR/ prior to each arming which clears THAGL/. An additional line from the motherboard is called CHEN (CHannel ENable). This signal, when negated, prevents the comparator from firing, and forces THAGL/ into an inactive state.

2.1.3 Sample And Hold Amplifiers - The gate from the gate generator passes through a level shifter, an isolating pulse transformer and is applied to the gate input of two FET switches. These switches allow the input position and intensity signals to charge the S/H storage capacitors.

2.1.4 Signal Conditioning - The position signal from the RF modules covers a range of +/- 2.2 volts. The A/D will digitize an input signal in the range of 0 to -.5 volts. A resistor network provides level shifting and attenuation.

The intensity signal is applied to a logarithmic amplifier which consists of a matched pair of transistors used in a transdiode configuration in the feedback loop of the amplifier.

2.1.5 Daughter Card Digitizing - The conditioned signals are coupled to the A/D through a second set FET switches. The selection of which switch is on is made by a line called INSEL/ (INTensity SELect). INSEL/ is negated throughout Snapshot data taking, thereby always selecting position. A START CONVERT pulse from the motherboard prepares the A/D for conversion, and 11 cycles of the 10 MHz clock are applied to the clock input of the A/D to perform the conversion.

2.1.6 Data Readout - The 8-bit output of the A/D appears at both output buffers. The position buffer is a transparent latch, so that under Snapshot conditions when only position information is needed, assertion of POS STROBE/ will place the position data on the data bus. In Flash mode when both position and intensity data are needed, LPOS/ (Latch POSition) must be asserted after the conversion of the position signal to store the data for a later POS STROBE/. Then INSEL/ is asserted and the intensity signal is converted. Intensity data is then available by asserting INT STROBE/.

2.2 Motherboard Block Diagram Description

Refer to Fig 3. The motherboard is divided into four functional groupings.

1. Read/Write registers which contain primarily downloaded data.
2. Address decoding for data registers on the daughter cards.
3. Snapshot control circuits.
4. Flash timing and control circuits. Flash control and Snapshot control share some common circuits.

2.2.1 Read/write Registers - There are five registers (six bytes) of downloaded data used by the Analog Box. The registers and their uses are described below. A list of addresses is found in Appendix A.

- o Intensity Threshold - This 8 bit register provides input for a D/A converter which in turn provides the analog signal used by each daughter card as the threshold voltage at the comparator. The actual voltage used by the comparator is divided down on the daughter card.
- o Miscellaneous Bits - This register contains 2 R/W control bits and 3 read only bits used for diagnostic purposes.

BIT 0 Batch/Bunch control. Batch = 0. This signal is bussed to all daughter cards where it is used to set the length of the S/H gate.

BIT 1 FTO/ (Flash Time Out) Described below.

BIT 2 SNARM (SNAPSHOT ARM) Described below.

BIT 3 FIP (Flash In Progress) Described below.

BIT 4 Unused

BIT 5 Unused

BIT 6 Unused

BIT 7 Proton or antiproton control.
PEAR(antiproton) = 1. This signal which

indicates measurement of either protons or antiprotons is used by the Flash timing circuits and additionally is made available to external hardware on the back of Analog Box via a BNC connector. This signal line will be called PBAR (antiprotons indicated by TTL high)

- o Dead Channel Mask - This is a 16 bit register requiring two read or write operations to access. Actually only 12 of the bits comprise the mask, each bit is sent to its corresponding daughter card where it becomes CHEN (CHannel ENable). A signal line, BPDR/ which is discussed later is routed to the MSB of the byte containing only 4 bits of the mask. This read only bit is used for diagnostic purposes.
- o Flash Width - As will be discussed later, the arming of the daughter cards in the Flash mode of operation is gated so that precise timing can be specified. The width of the gate is under host control, and the 8 bit value is stored in this register. One LSB equals .1 microseconds.
- o Flash Delay - The application of this register is similar to the Flash Width register except this specifies a delay used before any gates are generated. One LSB equals .1 microsecond.

2.2.2 Address Decoding For Data Registers - All of the registers which contain beam oriented data reside on the daughter cards. The Multibus hardware or software can access this data directly by specifying its address (See Appendix A for address specifications). The motherboard decodes the addresses and generates the strobes mentioned earlier in discussing the daughter cards. In addition to the strobes, the decoding hardware generates control signals to enable a bus driver which puts the data on the dataway to the Multibus, while at the same time disabling the bus tranceiver which connects the R/W registers to the dataway.

The motherboard also allows readout of the 12 THAGL/ bits which are used to indicate a valid reading. This is accomplished in two different ways. One of the ways the reading is done is via a set of two octal inverting buffers which place the set of THAGL/ bits on the data lines when the appropriate addresses are selected in a read operation. The so called THAG register is read in this manner after a Flash. The second way the THAGL/ bits can be read uses a 12 to 1 inverting multiplexer and a separate data line to Multibus. The same address lines which generate the position

strobes select the corresponding THAGL/ line and place it on the THAGR line to Multibus. This in effect becomes a nine bit read operation, and is the technique used in reading Snapshot data.

2.2.3 Snapshot Control - Although this section of the motherboard description is called Snapshot control it is somewhat a misnomer. The process of taking Snapshot data is under Multibus control with the motherboard acting as a slave generating the appropriate signals upon command.

Snapshots are enabled when the motherboard receives an enable on SNEN/ (SNAPSHOT ENABLE). If there is no beam detected when SNEN/ is asserted, the arming process begins immediately. The presence of beam is determined by a signal called BPOR/ (Beam Present OR) which is the ORing of all daughter card BIP/s. If BPOR/ is active no arming will occur until it is negated. Note that all detectors must simultaneously report 'no beam' before the arming process can begin. Note also that BPOR/ is sent back to Multibus where its assertion negates SNEN/ and begins timing the process of digitizing and reading the data.

Once the motherboard detects the assertion of SNEN/ and the negation of BPOR/ the arming process begins. This consists of generating an ACLR/ pulse to clear the THAGL/ bits, and generating the ARM/ pulse. A one-shot is triggered at this time which will generate a DISARM/ pulse after it times out. This is used only when beam does not arrive in the expected amount of time.

At this time the daughter cards are sampling the position signal and the motherboard is waiting for Multibus to send a CVEN/ (Convert Enable). When this pulse arrives the motherboard responds by generating a START CONVERT pulse which is sent to all daughter cards, and then gates 11 cycles of the 10MHz clock to each A/D chip. At this point the motherboard's contribution to Snapshot control is over, Multibus will now come around and read the position data and the THAGL/ bits. Throughout this process the control lines INSEL/ and LPOS/ remain negated.

2.2.4 Flash Control - Whereas Snapshot control was in the hands of Multibus, the Flash data taking process is essentially controlled by the motherboard. The trigger pulse for a Flash Data frame appears at the Analog Box on a data line called FLAT/ (FLASH TRIGGER). The leading edge of FLAT/ asserts both FIP and FIP/ (Flash In Progress). The assertion of these signal lines terminates the Snapshot process, both in Multibus and on the motherboard, and sets the motherboard up for Flash data taking. The trailing edge of FLAT/ triggers the generation of the ACLR/ and ARM/ pulses. The arming of the daughter cards in Flash mode is more involved though, than for Snapshots. A separate FLAG

(FLASH Gate) must be generated for each daughter card allowing for the delays in beam travel, and signal travel from the detectors to the BPM. This gate must be asserted on each card for the card to effectively be armed. The generation of these gates is the job of the box on the block diagram called Flash Timing. The assertion of FIP loads two sets of count down counters with the downloaded values of Flash Delay and Flash Width. The 10MHz clock is immediately applied to the Flash Delay counter and when it has counted down a "common flash gate" called FLASH WIDTH/ is asserted. This gate remains active while the Flash Width counter counts down. FLASH WIDTH/ must be translated into individual FLAGS for the daughter cards, and this is accomplished on a separate plug-in card called the Flash Trigger Distribution Card. The FTD card receives FLASH WIDTH/, the 10MHz clock, and the PBAR line. FLASH WIDTH/ becomes the input to a set of 8-bit parallel-out serial shift registers clocked by the 10 MHz clock. The outputs are made available to a set of jumper wires so that a given detector may receive its Flash Gate from any output over a range of 1.6 microseconds. The PBAR line is used to control 2 to 1 data selectors so that different delays can be established to look at antiprotons. The outputs of the data selectors essentially become the FLAGS.

The circuitry for generation of individual FLAGS was put on a separate card because the distribution is unique for different service buildings. Thus Analog Boxes can be changed and the proper distribution can be maintained by replacing the FTD card.

Once the FTD card has negated the last FLAG, it asserts a signal line called ENDF/ (END of Flash) which notifies the motherboard that all Daughter Cards should now have valid data stored in their S/H circuits. A DISARM/ pulse is sent to all Daughter Cards, and a shift register, acting as a state processor is activated, clocked with a 1.6 microsecond clock. This processor steps through the following tasks at the times indicated, with respect to the assertion of ENDF/.

- 0.0 us Assert FTD/ (Flash Time Out) which lets Multibus know that A/D conversion is about to begin.
- 1.6 us Generate a convert enable pulse. This will cause the control circuitry to send a START CONVERT pulse and the GATED 10MHz clock to the Daughter Cards to digitize the position data.
- 3.2 us Generate both LPOS/ to latch the position data, and INSEL/ to place the intensity signal at the A/Ds input.
- 8.0 us Generate a second convert enable pulse, this time digitizing the intensity signal. The extra time between these two states allows the intensity signal to settle.

9.6 us Negate INSEL/.

At this point the motherboard has completed the control of the Flash data taking process. Mutibus must come around and read the positions, intensities and the THAQ register. When it is finished it will assert TWI/ (sorry, no acronym) which negates FIP and resets any remaining control lines (LPOS/,FTD/) from the Flash data taking. Snapshot data taking will resume with the next SNEN/.

3.0 CIRCUIT DESCRIPTION

The circuit description follows the same format as the block diagram description.

3.1 Circuit Description For The Daughter Card

The Analog Box daughter card schematic diagram is Fermilab drawing number 1680.00-ED-158407.

3.1.1 Daughter Card Arming - The ARM/ pulse from the motherboard sets the Flip Flop (FF) U3A to set Q. U3A is reset either by the rising edge of the S/H gate which clocks a '0' through, or by DISARM/ which clears U3A. The Q output of U3A is ANDed in U18 with FLAG to form the 'composite arm' level for the daughter card.

3.1.2 Daughter Card Triggering And Gate Generation - The Daughter Card is triggered by the negative going intensity signal. A NE529 comparator receives the intensity signal at one input, and a threshold level at the other input. The threshold level at the input to the comparator is reduced by a factor of 20.6 from the motherboard threshold level. The positive going output from the comparator is used to provide hysteresis into the threshold input. For control purposes the negative going output is controlled by CHEN. A TTL '0' on CHEN disables this output.

The arm level developed by U3A appears as the J input to U2A, a negative edge triggered J-K Flip Flop ('S112). U2A is clocked by the negative going edge of the comparator, so that the arm level appears at the Q output, where it becomes the S/H gate. The length of this gate is determined by U1A, which generates a clear pulse for U2A. The inputs to U1A, which acts as a negative logic OR gate, are the independent clears for Batch mode and Bunch mode. These two clear pulses are derived in the following manner. The negative going output of the comparator triggers U5A, a 'LS123

one-shot. The pulse length of U5A is set to ~200 nanoseconds which determines the gate length for Batch mode operation. The trailing edge of the Q/ output triggers U5B, which delivers a short negative going pulse to U1A. This becomes the Batch mode clear pulse. The leading edge of the Q/ output from U5A is delayed 40 nanoseconds by an RC network and then used to clock U2B. The J input to this FF is the BATCH/ signal line. If this signal line is set high, for Bunch mode operation the output the Q/ output will go low, clearing U2A in Bunch mode. If BATCH/ is asserted (TTL low) this clear pulse will not be generated.

The Flip Flop U3B is used to generate the THAGL/ bit. The ACLR/ pulse from the motherboard clears U3B. The positive going output from the comparator appears as the D input to U3B. The Q/ output from U2A is used to clock U3B. Thus, the trailing edge of the S/H gate clocks the state of the positive going output of the comparator through as THAGL/. Valid beam is therefore defined as an intensity signal which exceeded the threshold, and is still greater than threshold at the end of the S/H gate. Note that the Thagl signal is enabled by CHEN in U1 and then inverted to become THAGL/.

The motherboard is informed about the state of the comparator via signal line BIP/. BIP/ is the negative going output of the comparator stretched by U5.

3.1.3 Sample And Hold Amplifiers - U14 is a quad low "on" resistance FET switch. Its characteristics are such that if the gate voltage is maintained negative with respect to the source, it is "off" and if positive it is "on". The magnitude of the source to drain "on" resistance depends in part on how large the source to gate voltage is. To achieve fast sampling times it is necessary to have a small charging time constant for the 220 pf storage capacitors. The pulse transformer, besides providing a 20 volt turn on pulse, also allows keeping the gates quiescently at -5.0 volts (i.e. "off") by tying the secondary center tap to -5 volts. The transformer also provides an opposite polarity gate pulse for canceling capacitive feed thru to the intensity port (C1 trimmer), pedestal cancellation (C2 trimmer) at the storage capacitor, and BATCH/BUNCH convergence of the low intensity signal levels. These compensations are only necessary for the Intensity channel.

Q1 is used to get a low Z driving source for the transformer primary and also for current gain. Two sections of U8 are paralleled for increased current capability. The large primary pulse current is supplied by the 1 MFD capacitor and it is charged by a constant current source (Q2). Using a constant current source protects the pulse transformer primary if for some reason Q1 should become permanently latched on.

Both the Intensity and Position inputs have 50 ohm terminations on the P.C. board. Also both inputs are driven by 50 ohm sources and therefore the total FET S/H charging Z is 25 ohms. The "on" resistance of the SD-5000 (U14) is typically 25 ohms. Therefore the charging time constant is 11 nanoseconds. U13 and U15 are FET input Op Amps connected as followers and therefore allow long hold times with negligible droop. Although the slew rates of U13 and U15 are typically only 9 volts / microsecond, A/D conversions are not done until the outputs have settled.

3.1.4 Signal Conditioning - Since the Position input signal ranges between +/-2.5 volts and the A/D chip (U6) requires 0 to -0.5 volts, both a factor of ten attenuation and a level shift are needed before going to the A/D analog input. Both of these requirements are met with a passive resistive network at the output of U13. The U13 offset adjust pot. allows calibrating a 0 0 volt Position input signal to be equal to a hex 80 digital output.

Since the Intensity signal is expected to cover a 2.5 to 3 decade range, and since the A/D conversion is limited to 8-bits, it was deemed necessary to use a logarithmic conversion between the intensity S/H and the A/D chip. This is accomplished by U9 and U12 Op Amps which have diode connected transistors (2N2060) as feedback elements. This generates an output from U12 that is typically 60 millivolts per decade change of input current. U9 is used as a reference log output and also cancels the large (typically -2.5 mv/deg C) forward temperature coefficient of the log feedback elements.

The output of U10 is 2.5 times the difference between U9 and U12 outputs. The U15 offset adjustment pot allows calibrating the low intensity end (i.e. 10 mv) and the U10 offset adjustment pot allows calibrating the middle intensity range (i.e. 100 mv).

3.1.5 Daughter Card Digitizing - The conditioned position signal is applied to the source input of switch U14C, and the conditioned intensity signal is applied to the source input of U14D. The drain outputs of these switches are connected together and tied to the A/D input. The switches are controlled from signal line INSEL/ by gates USD, UBE, and UBF so that only one switch can be on at a time. The bipolar levels needed by these switches is provided by Q3 and Q4.

The actual digitizing is done by U6, a TRW 1001 chip which is a fast, successive approximation 8-bit digitizer. U6 requires a reference voltage which is derived by taking one tenth of the Analog Box minus 5 volt line. The START CONVERT pulse, and the

10 MHz clock for digitization are provided from the motherboard as needed.

3.1.6 Data Readout - The 8 data lines from the A/D are bussed to the inputs of U4, a 'LS373 transparent latch, and to U7, an octal line driver. The output of U4 will follow the inputs as long as the Output Control pin is asserted, and the Enable G pin is held high. On the daughter card the Output Control is driven by POSITION STROBE/ from the motherboard and the Enable G pin is driven by LPOS/. When reading Snapshot data (position only) LPOS/ is kept high so that the outputs track the inputs, and the data is placed on the dataway when the POSITION STROBE/ pulse is decoded. When LPOS/ is asserted, U4 will latch the position data at the outputs. The outputs of U7 always track the inputs, but in practice the Gate Control pins, connected to INTENSITY STROBE/, are only asserted after intensity data has been digitized.

3.2 Motherboard Circuit Description

The Analog Box motherboard schematic diagram is Fermilab drawing number 1690.00-ED-158400.

3.2.1 Read/Write Registers - The Read/Write registers physically are U4, U5, U7, U8, U20, U21, U22, U23, U24, U25, U26, and U27. Each register consists of a 'LS374 octal latch and a 'LS244 line driver. Data on the data bus is latched into the 'LS374 when its clock pin is strobed. The strobe pulses for the 'LS374s are generated by address decoding chip U19, a 'LS138 3-to-8 line decoder which is enabled by dataway signal WST/. The data to be written is coupled through to the Analog Box data bus by U46 and U47, 'LS243 bus transceivers which are set to the 'write' direction by dataway line WAD.

The outputs of the latches are made available to the hardware that requires the data, and to the inputs of the 'LS244 line drivers. The line drivers place the data back on the data bus when their output control pins are asserted. The address decoding for read operations is done by U17, also a 'LS138 3-to-8 line decoder, which is enabled by an output from U18. The additional logic is needed since there are many more read registers in the Analog Box than write registers. More will be said about address decoding for reading data registers in the next section.

The intensity threshold is converted to an analog signal by U28, an AD7533UN 10-bit DAC with the two least significant bit inputs grounded. Its current output is converted to a voltage output by Op Amp U13 which also includes a 2N3906 transistor in

the feedback loop. This provides the drive capability necessary for servicing up to 12 Daughter Cards. The desired +1.0 to -4.0 volt threshold range (divided on the Daughter Cards) is achieved by first getting a 0.0 to -5.0 volt range out of U28 (using a +5 volt reference) and then offsetting by 1 volt with an adjustable current into the Op Amp summing point.

3.2.2 Address Decoding For Data Registers - The decoding of the address lines to generate the INTENSITY STROBE/ and POSITION STROBE/ pulses needed by the Daughter Cards utilizes two levels of decoding chips. The first level is U18, the 'S139 dual 2-to-4 line decoder mentioned in the last section. One of these decoders uses address lines A2 and A3 to select one of four 3-to-8 line 'LS138 decoders. Of these four 3-to-8 line decoders, one, U17, is used to access the Read/Write registers. The other three U1, U6, and U11 decode address line A0, A1, and A4 to generate the strobes needed by the Daughter Cards. The selection of either U1, U6, or U11 is detected by U50A, a 'LS11 negative logic OR gate which turns on the Daughter Card bus driver (U43) and places the Read/Write register bus transceivers in their isolated state.

The THAQ registers (parallel readout of THAQL/ lines) are read from U3 and U10, 'LS240 octal line drivers. The decoding for these is performed by the logic used to decode addresses for the Read/Write registers. The serial readout of THAQL/ lines is accomplished with U2 and U9, 'LS251 8-line data selectors with 3-state outputs. Both use address lines A0, A1, and A2 to select which THAQL/ line is selected. The appropriate selector is chosen by the second 2-to-4 line decoder of U18 which monitors address lines A3 and A4.

3.2.3 Snapshot Control - Each Daughter Card sends a signal called BIP/ to the motherboard which indicates that the daughter card currently senses beam passing its detector. All of the BIP/ lines are ORed in U12 a 'S133 13 input negative logic OR gate to form BPOR/. (BPOR/ is deglitched by U42B, a one shot which is triggered by the first BIP/.) BPOR/ will only be a TTL "high" level if NO BIP/s are asserted.

The Snapshot data taking process begins when Multibus asserts SNEN/. The entire data taking process, both the multibus hardware and the motherboard, waits for the negation of BPOR/. (i.e. all detectors simultaneously reporting no beam.) BPOR/ is shipped to multibus and on the motherboard it is NANDed with SNEN so that the NAND of Snapshot ENable and NOT BPOR/ in U53 sets FF U40A. The Q output of U40A is SNARM (SNAPSHOT ARM). SNARM goes to input 1B of U35, an 'LS157 2 to 1 line data selector. In this case U37 is used as a control selector with FIP/ being the select line. As long as FIP/ (Flash In Progress) is high (we will see that it

always is during snapshots) the 'B' or snapshot control lines will be coupled through to the outputs. In the case of snapshots, SNARM clocks U31A which then clocks U30B, both 'LS74 FFs acting as 50 nanosecond one-shots. U31A produces ACLR/ which clears all of the THAGL lines, and U30B generates the ARM/ pulse which arms the daughter cards.

In the normal scenario beam will now pass one of the detectors, setting BPDR/. This has no direct effect on the motherboard, but when the multibus hardware detects the assertion of BPDR/, it will immediately negate SNEN/ which (after a delay in U42A) resets U40A, the SNARM FF. U40A in turn generates a positive going disarm edge on its Q/ output which finds its way through the control selector, U39, to U30A again acting as a one-shot. The disarm pulse generated here is bussed to all the daughter cards.

The next step in the snapshot data taking process is again initiated by multibus. Control line CVEN (ConVert ENable) is asserted, clocking a TTL high signal from U41, through the control selector to the D input of U38. U38 synchronizes the convert enable command to the 10 MHz clock. The output of U38 is used to load U55, an 'LS161 synchronous counter with the value '4'. U55 then counts up to 15 (driven by the 10 MHz clock) and shuts off. During the time it is counting it couples 11 cycles of the 10 MHz clock out to the ADCs on the daughter cards by gating on U57A. Note also that the presence of a '4' at the parallel outputs of U55 produces the START CONVERT pulse at the output of U57B. This pulse is also bussed to all the daughter cards.

After waiting the appropriate length of timing the multibus hardware will read the twelve positions from the daughter cards utilizing motherboard address decoding described in Section 3.2.2.

3.2.4 Circuit Description Of Flash Data Taking -

The process of taking Flash data is a major disruption to the normal process of taking Snapshot data. When the multibus hardware detects a Flash clock event it stops generating any snapshot control signals and sends a pulse, FLAT/ (FLASH Trigger) to the Analog Box. The leading (falling) edge of FLAT/ is used to clock flip flop U40B whose outputs are FIP and FIP/ (Flash In Progress). These signal lines are only set by FLAT/, remaining unasserted during the Snapshot data taking process. FIP/ is used in three ways; it notifies multibus that the Analog Box is in the process of taking Flash data, it clears SNARM, and it set the control selector, U39 to select Flash control signals. FIP is used to clear several control flip flops, and it begins the generation of the FLAGS (FLASH Gates) which we will discuss shortly.

Meanwhile, the trailing (rising) edge of FLAT/ becomes the control signal, coupled through U39, generating the ACLR/ and ARM/ pulses in the same manner as SNARM.

At this point the control circuits we've been considering are waiting for the assertion of ENDF/ (END Flash) in order to generate any further digitization commands. To see how ENDF/ is developed we have to look at the timing associated with the FLAGS. Recall that each daughter card receives an individual FLAG line which is used as part of its arming circuitry. Immediately upon the assertion of FIP, all FLAGS are negated in U14, U15, and U16. This will effectively disarm all daughter cards until the FLAGS are asserted. U33, U34, U35, and U36 are two sets of cascaded synchronous 4-bit counters ('LS193s). FIP is connected to the load input of these counters so the assertion of FIP will allow these counters to count as soon as a clock is provided. The 10 MHz clock is immediately coupled to the U35, U36 pair which is the Flash Delay counter. Nothing happens to any FLAGS while this counter is counting down. Upon counting down, the borrow is set which couples the 10 MHz clock to the second set of counters, U33 and U34, and shuts the first set off. While these Flash Width counters are counting down, signal line FLASH WIDTH/ is asserted.

This operation can be summarized by saying that a signal line, FLASH WIDTH/, is asserted Flash Delay (in units of .1 microseconds) after FIP is asserted, and remains asserted Flash Width (again in units of .1 microseconds). This provides aggregate control over the FLAGS for each Analog Box. However it is desirable to have individual control for each daughter card of the FLAG delay. This is the function of the Flash Trigger Distribution Card, Fermilab Drawing 1680.00-EC-158414.

The FLASH WIDTH/ line appears as the input to a pair of 'LS164 parallel-out serial shift registers. These shift registers are clocked by the 10 MHz clock. The FLASH WIDTH/ gate appears at the parallel outputs in successive steps of .1 microsecond delay providing a maximum delay of 1.6 microseconds. Jumpers can be inserted on the card choosing the amount of delay needed for a particular channel. The FTD card also provides the capability of using different delays for circulating antiprotons. Three 'LS157 data selectors are used to select either the set of 'proton' jumpered signal lines, or 'antiproton' jumpered signal lines. The outputs of the data selectors are NANDed with FIP in U14, U15, and U16 to produce the 12 FLAG signals. When the trailing (rising) edge of the FLASH WIDTH/ gate reaches the last shift register output it clocks a TTL high into the output of an 'LS74 FF. This in turn is synchronously clocked into a second 'LS74 FF whose Q/ output becomes ENDF/.

The generation of the ENDF/ signifies the end of the Flash data gathering process as far as the daughter card Sample and Hold circuits are concerned. It really doesn't matter whether any beam was detected or not. (In the Snapshot mode the detection of beam

BPOR/s assertion, signified to the hardware that digitization should commence.) The Flash data taking mode is not forgiving, if beam does not occur during the FLAG on a given daughter card no THAGL/ bit will be reported for that card.

The ENDF/ pulse is returned to the motherboard where it provides several functions. It is routed through the control line selector, U39, to generate the disarm pulse for the daughter cards; it synchronizes a 10 MHz divide by 16 counter (U52), and it is used to provide a control input to U54, an 'LS164 shift register used as a state processor. U52 clocks this shift register at a 1.6 microsecond rate effecting the operations listed in Section 2.2.4 using primarily circuitry already described in the section on Snapshot control.

Readout of the data is under multibus control, and when multibus is again ready to set the Analog Box into the snapshot mode it asserts TWi/ which clears U40B, negating FIP and FIP/.

APPENDIX A

ANALOG BOX ADDRESS ASSIGNMENTS

The following are the address assignments used by Multibus to access Analog Box data registers. All addresses are specified in hex, and the two digit number represents the 5-bit address decoded by the Analog box.

7D20 - 7D22 POSITION DATA Channels 0 - 11 READ ONLY
 00 - 0B

7D30 - 7D3B INTENSITY DATA Channels 0 - 11 READ ONLY
 10 - 1B

		D7 D6 D5 D4 D3 D2 D1 D0	
		+---+---+---+---+---+---+---+---+	
7D2C	THAGR	! B! X! X! X! 11110! 9! 8!	READ ONLY
0C		+---+---+---+---+---+---+---+---+	
		!-> CHANNELS	
		BITS 4-7 UNUSED	
		BITS 0-3 THAGL/ BITS for channels indicated	

		D7 D6 D5 D4 D3 D2 D1 D0	
		+---+---+---+---+---+---+---+---+	
7D2D	THAGR	! 7! 6! 5! 4! 3! 2! 1! 0!	READ ONLY
0D		+---+---+---+---+---+---+---+---+	
		!-> CHANNELS	

		D7 D6 D5 D4 D3 D2 D1 D0	
		+---+---+---+---+---+---+---+---+	
7D2E	DEAD	! B! X! X! X! 11110! 9! 8!	R/W
0E	CHANNEL	+---+---+---+---+---+---+---+---+	
	MASK	!-> CHANNELS	
		BIT 7 BPOR/	
		BITS 4-6 UNUSED	
		BITS 0-3 CHEN BITS for channels indicated	

ANALOG BOX ADDRESS ASSIGNMENTS

		D7 D6 D5 D4 D3 D2 D1 D0	
7D2F	DEAD	+---+---+---+---+---+---+---+---+	
OF	CHANNEL	7 6 5 4 3 2 1 0	R/W
	MASK	+---+---+---+---+---+---+---+---+	
		!-> CHANNELS	

7D3C	INTENSITY THRESHOLD	8-BIT DAC value	R/W
1C			

		D7 D6 D5 D4 D3 D2 D1 D0	
7D3D	MISC.	+---+---+---+---+---+---+---+---+	
1D	BITS	P X X X F S T B	R/W
		+---+---+---+---+---+---+---+---+	
	BIT 7	PBAR/	
	BITS 6-4	UNUSED	
	BIT 3	FIP	READ ONLY
	BIT 2	SNARM	READ ONLY
	BIT 1	FTO/	READ ONLY
	BIT 0	BATCH/	

7D3E	FLASH DELAY	8-BIT timer value	R/W
1E			

7D3F	FLASH WIDTH	8-BIT timer value	R/W
1F			

APPENDIX B

BACK PANAL OUTPUT FOR PBAR/P CONTROL

This output on the back panel of the analog box is unused at the present time. It is intended to provide control of the stripline terminators when the reality of PBARs necessitate the ability to terminate the striplines at the (traditional) upstream end. This appendix lists the electrical specifications of this output.

The output is a 75452 open collector driver with a high level output voltage of 30 volts and a maximum sink current capability of 500 milliamps. In the proton (P) mode the BNC output is in the HI Z state (i.e. off state). Note that if inverse logic is desired, a 75451 could be used. Note also that this BNC port acts only to control an externally powered device such as a relay or solenoid. If this device is inductive it should have its own snubbing diode to prevent high voltage transients.

APPENDIX C

ENERGY DOUBLER

DRAWING NO	DRAWING TITLE	DWN	DATE
680.00 EE 158400	BPM, ANALOG CRATE, MOTHER BD. SCHEMATIC		
BE 158401	" " " " ARTWORK		
BE 158402	" " " " DRILL DWG.		
BE 158403	" " " " COMP. LAYOUT		
BE 158404	" " " " SOLDER MASK		
BE 158405	" " " " SILK SCREEN		
BP 158406	" " " " PARTS LIST		
ED 158407	BPM, ANALOG CRATE, DAUGHTER BP. SCHEMATIC		
BC 158408	" " " " ARTWORK		
BC 158409	" " " " DRILL DWG.		
BC 158410	" " " " COMP. LAYOUT		
BC 158411	" " " " SOLDER MASK		
BC 158412	" " " " SILK SCREEN		
BP 158413	" " " " PARTS LIST		
EC 158414	BPM, ANALOG CRATE, FLASH TRIG. BD. SCHEMATIC		
BC 158415	" " " " ARTWORK		
BC 158416	" " " " DRILL DWG.		
BC 158417	" " " " COMP. LAYOUT		
BC 158418	" " " " SOLDER MASK		
BC 158419	" " " " SILK SCREEN		
1180.00			

APPENDIX C-2

ENERGY DOUBLER

DRAWING NO	DRAWING TITLE	DWN	DATE
1680.00 BP 158420	BPM, ANALOG CRATE, FLASH TRIG. PP. PARTS LIST		
MC 158421	" " " FRONT PANEL MACHINING		
MC 158422	" " " " SILK SCREEN		
MC 158423	" " " " ASSEMBLY DWG.		
MC 158424	" " " REAR " MACHINING		
MC 158425	" " " " SILK SCREEN		
MC 158426	" " " " ASSEMBLY DWG.		
MC 158427	" " " " CHASSIS SIDES MACHINING		
MB 158428	" " " " CHASSIS SLIDE END SUPPORT BLOCK		
158429			
158430			
158431			
158432			
158433			
158434			
158435			
158436			
158437			
158438			
1680.00 158439			

$V(mv) = -953N + 48.5 = (5/20.6) / R + 48.5$

DAC Input dec. out. hex

1	001	01	47.5
2	002	02	46.6
3	003	03	45.6
4	004	04	44.7
5	005	05	43.7
6	006	06	42.8
7	007	07	41.8
8	010	08	40.9
9	011	09	39.9
10	012	0A	39.0
11	013	0B	38.0
12	014	0C	37.1
13	015	0D	36.1
14	016	0E	35.2
15	017	0F	34.2
16	020	10	33.3
17	021	11	32.3
18	022	12	31.3
19	023	13	30.4
20	024	14	29.4
21	025	15	28.5
22	026	16	27.5
23	027	17	26.6
24	030	18	25.6
25	031	19	24.7
26	032	1A	23.7
27	033	1B	22.8
28	034	1C	21.8
29	035	1D	20.9
30	036	1E	19.9
31	037	1F	19.0
32	040	20	18.0
33	041	21	17.1
34	042	22	16.1
35	043	23	15.1
36	044	24	14.2
37	045	25	13.2
38	046	26	12.3
39	047	27	11.3
40	050	28	10.4
41	051	29	9.4
42	052	2A	8.5
43	053	2B	7.5
44	054	2C	6.6
45	055	2D	5.6
46	056	2E	4.7
47	057	2F	3.7
48	060	30	2.8
49	061	31	1.8
50	062	32	-1.1
51	063	33	-1.1
52	064	34	-2.0
53	065	35	-3.0
54	066	36	-3.9
55	067	37	-4.9
56	070	38	-5.8
57	071	39	-6.8
58	072	3A	-7.7
59	073	3B	-8.7
60	074	3C	-9.6
61	075	3D	-10.6
62	076	3E	-11.5
63	077	3F	-11.5

Intensity Threshold DAC settings

64	100	40	-12.5
65	101	41	-13.4
66	102	42	-14.4
67	103	43	-15.3
68	104	44	-16.3
69	105	45	-17.3
70	106	46	-18.2
71	107	47	-19.2
72	110	48	-20.1
73	111	49	-21.1
74	112	4A	-22.0
75	113	4B	-23.0
76	114	4C	-23.9
77	115	4D	-24.9
78	116	4E	-25.8
79	117	4F	-26.8
80	120	50	-27.7
81	121	51	-28.7
82	122	52	-29.6
83	123	53	-30.6
84	124	54	-31.5
85	125	55	-32.5
86	126	56	-33.5
87	127	57	-34.4
88	130	58	-35.4
89	131	59	-36.3
90	132	5A	-37.3
91	133	5B	-38.2
92	134	5C	-39.2
93	135	5D	-40.1
94	136	5E	-41.1
95	137	5F	-42.0
96	140	60	-43.9
97	141	61	-44.9
98	142	62	-45.8
99	143	63	-46.8
100	144	64	-47.7
101	145	65	-48.7
102	146	66	-49.7
103	147	67	-50.6
104	150	68	-51.6
105	151	69	-52.5
106	152	6A	-53.5
107	153	6B	-54.4
108	154	6C	-55.4
109	155	6D	-56.3
110	156	6E	-57.3
111	157	6F	-58.2
112	160	70	-59.2
113	161	71	-60.1
114	162	72	-61.1
115	163	73	-62.0
116	164	74	-63.0
117	165	75	-63.9
118	166	76	-64.9
119	167	77	-65.9
120	170	78	-66.8
121	171	79	-67.8
122	172	7A	-68.7
123	173	7B	-69.7
124	174	7C	-70.6
125	175	7D	-71.6
126	176	7E	-72.5
127	177	7F	-72.5

approx beam intensity 170 ppb

128	200	80	-73.5
129	201	81	-74.4
130	202	82	-75.4
131	203	83	-76.3
132	204	84	-77.3
133	205	85	-78.2
134	206	86	-79.2
135	207	87	-80.1
136	210	88	-81.1
137	211	89	-82.1
138	212	8A	-83.0
139	213	8B	-84.0
140	214	8C	-84.9
141	215	8D	-85.9
142	216	8E	-86.8
143	217	8F	-87.8
144	220	90	-88.7
145	221	91	-89.7
146	222	92	-90.6
147	223	93	-91.6
148	224	94	-92.5
149	225	95	-93.5
150	226	96	-94.4
151	227	97	-95.4
152	230	98	-96.3
153	231	99	-97.3
154	232	9A	-98.3
155	233	9B	-99.2
156	234	9C	-100.2
157	235	9D	-101.1
158	236	9E	-102.1
159	237	9F	-103.0
160	240	A0	-104.0
161	241	A1	-104.9
162	242	A2	-105.9
163	243	A3	-106.8
164	244	A4	-107.8
165	245	A5	-108.7
166	246	A6	-109.7
167	247	A7	-110.6
168	250	A8	-111.6
169	251	A9	-112.5
170	252	AA	-113.5
171	253	AB	-114.5
172	254	AC	-115.4
173	255	AD	-116.4
174	256	AE	-117.3
175	257	AF	-118.3
176	260	B0	-119.2
177	261	B1	-120.2
178	262	B2	-121.1
179	263	B3	-122.1
180	264	B4	-123.0
181	265	B5	-124.0
182	266	B6	-124.9
183	267	B7	-125.9
184	270	B8	-126.8
185	271	B9	-127.8
186	272	BA	-128.7
187	273	BB	-129.7
188	274	BC	-130.7
189	275	BD	-131.6
190	276	BE	-132.6
191	277	BF	-133.5

2x10⁹ ppb

192	300	C0	-134.5
193	301	C1	-135.4
194	302	C2	-136.4
195	303	C3	-137.3
196	304	C4	-138.3
197	305	C5	-139.2
198	306	C6	-140.2
199	307	C7	-141.1
200	310	C8	-142.1
201	311	C9	-143.0
202	312	CA	-144.0
203	313	CB	-144.9
204	314	CC	-145.9
205	315	CD	-146.9
206	316	CE	-147.8
207	317	CF	-148.8
208	320	D0	-149.7
209	321	D1	-150.7
210	322	D2	-151.6
211	323	D3	-152.6
212	324	D4	-153.5
213	325	D5	-154.5
214	326	D6	-155.4
215	327	D7	-156.4
216	330	D8	-157.3
217	331	D9	-158.3
218	332	DA	-159.2
219	333	DB	-160.2
220	334	DC	-161.1
221	335	DD	-162.1
222	336	DE	-163.1
223	337	DF	-164.0
224	340	E0	-165.0
225	341	E1	-165.9
226	342	E2	-166.9
227	343	E3	-167.8
228	344	E4	-168.8
229	345	E5	-169.7
230	346	E6	-170.7
231	347	E7	-171.6
232	350	E8	-172.6
233	351	E9	-173.5
234	352	EA	-174.5
235	353	EB	-175.4
236	354	EC	-176.4
237	355	ED	-177.3
238	356	EE	-178.3
239	357	EF	-179.3
240	360	F0	-180.2
241	361	F1	-181.2
242	362	F2	-182.1
243	363	F3	-183.1
244	364	F4	-184.0
245	365	F5	-185.0
246	366	F6	-185.9
247	367	F7	-186.8
248	370	F0	-187.8
249	371	F9	-188.8
250	372	FA	-189.7
251	373	FB	-190.7
252	374	FC	-191.6
253	375	FD	-192.6
254	376	FE	-193.5
255	377	FF	-194.5

Admin. T. Threshold DAC constant

3x10⁹ ppb

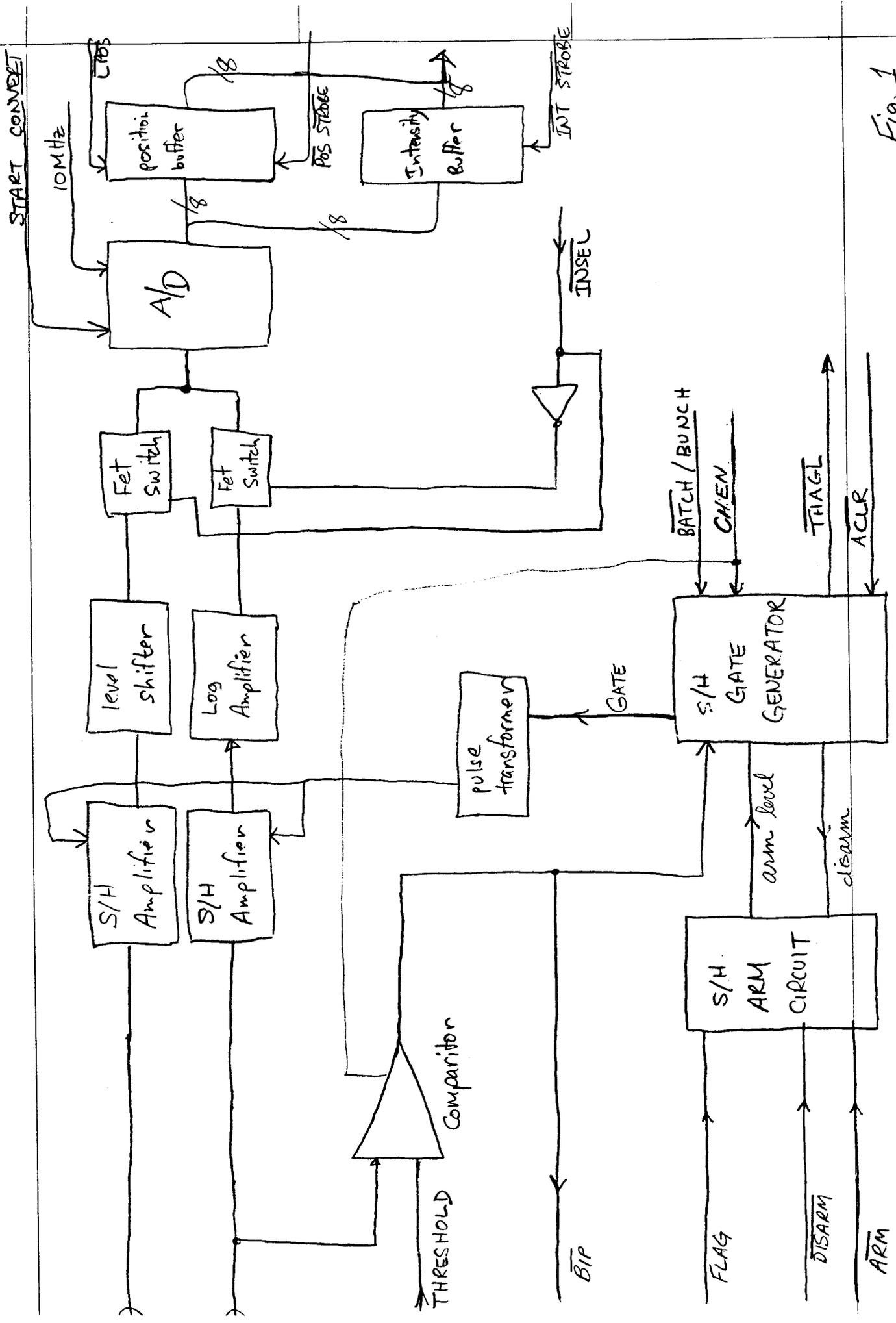
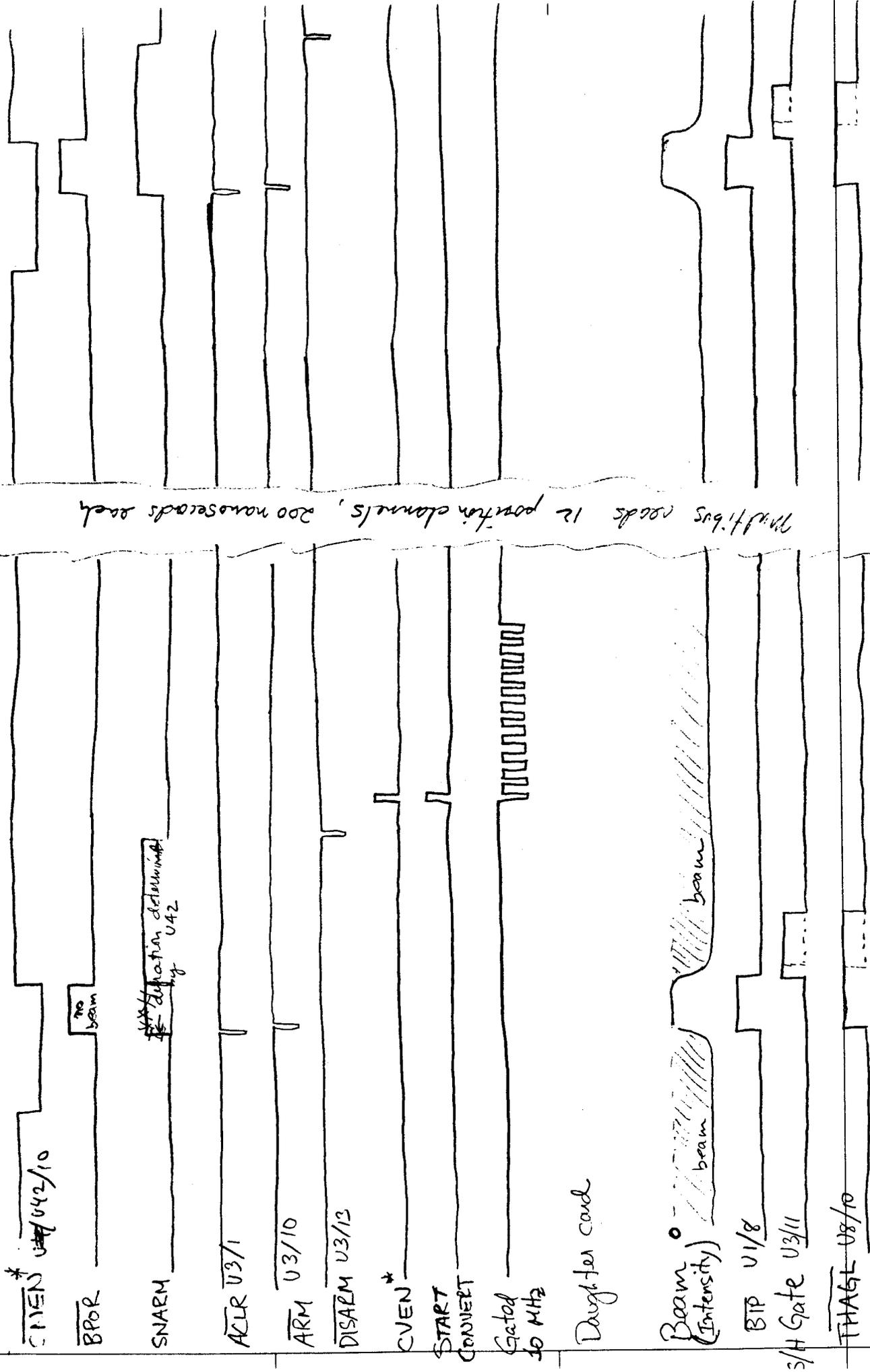


Fig 1

Analogy Box Snapshot Timing

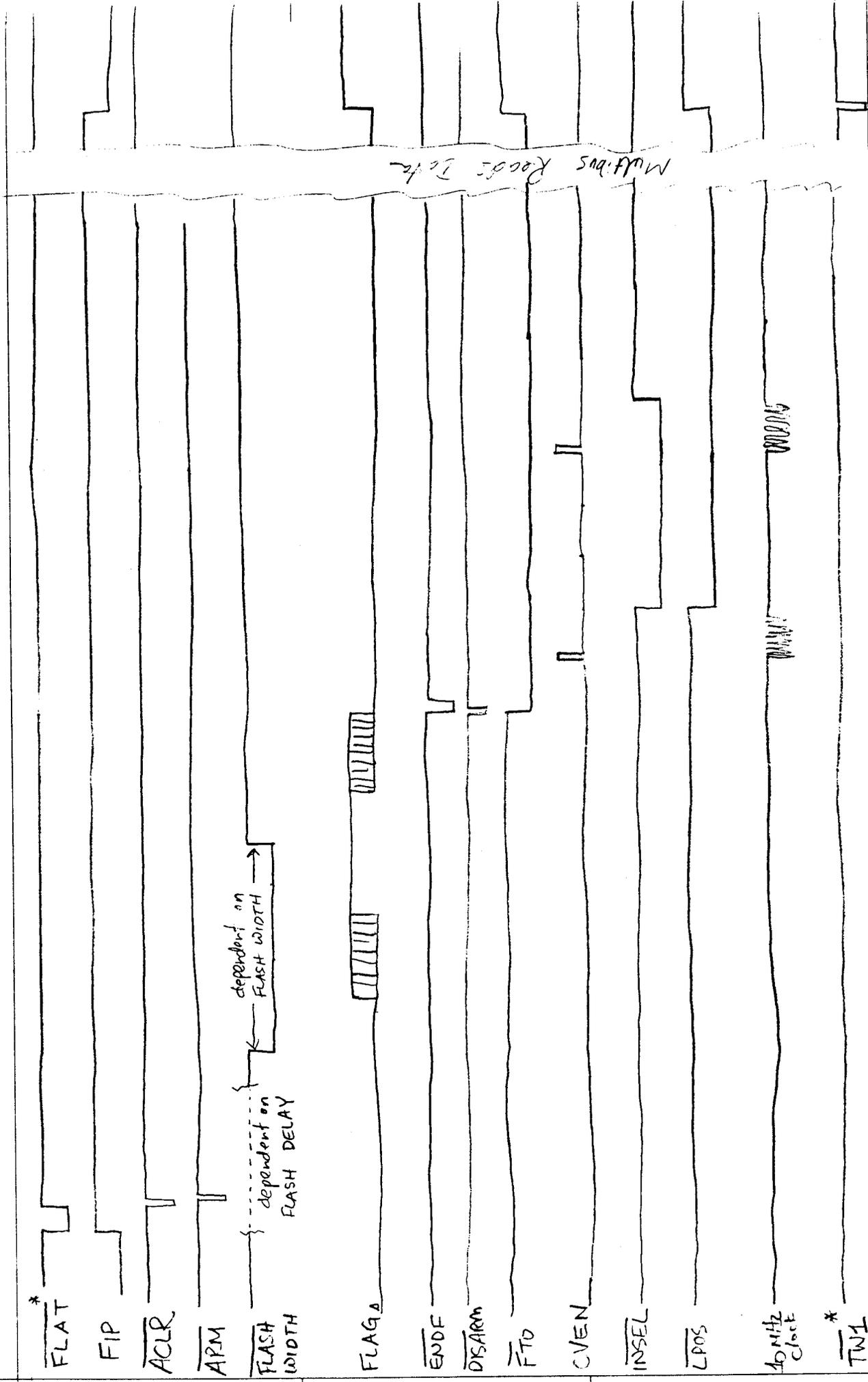
***** measurement holdoff time



Multibus needs 12 position channels, 200 nanoseconds each

signals with * originate

Analog Box Flash Timing



signals marked with asterisk (*) are generated by multibits