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Beam Loss Monitor System Description

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I. Overview:

A. Purpose:

The primary purpose of the BLM system is to protect the cryogenic magnets from quenching induced by beam loss in the Tevatron. Secondary uses are tuning and diagnostics.

B. General System Description:

The BLM system consists of two main components: BLM ion chambers and BLM electronics chassis.

1. Ion Chambers:

   The BLM ion chambers are argon filled glass ion chambers of approximately 100 cm^3 active volume. The glass chambers are inside of aluminum enclosures with input and output connectors. The packaged chambers are typically located at each spool piece around the ring. Chambers are described in more detail later.

2. Signal Cables:

   BLM chambers are connected via RG58 coaxial cables to their BLM electronics chassis in each house (service building).

   a. High Voltage:

      The BLM chassis supplies high voltage for operating the ion chambers ($\leq$ 3000 VDC). The HV cable is daisy chained to all detectors serving one house (8-9 chambers). Red RG58 and SHV connectors are used.

b. Signal Cables:

The radiation induced current in the BLM chambers is fed to the BLM chassis servicing them via green RG58 BNC cables. The signal cables are not daisy chained, they are brought back individually to the house.

3. Electronics Chassis:

The BLM electronics chassis processes signals received from the BLM chambers, and passes data to the BPM/BLM microprocessor via the external device buss. An abort signal is also passed to the abort chassis. The BLM log integrator outputs are made available to the house MADC. Each BLM chassis is capable of serving a maximum of 12 BLM chambers. The EDB is capable of serving two BLM chassis by using alternate addressing techniques. The standard system uses only one BLM chassis, however. The BLM electronic chassis is described in greater detail later.

II. BLM Ion Chambers:

The BLM ion chamber assembly consists of: the BLM ion chamber, a high voltage filter, and the BLM enclosure.

A. Ion Chamber:

The ion chamber is comprised of two cylindrical, concentric nickel electrodes forming approximately 100 cm^3 active volume. These are encapsulated in a glass envelope and filled with argon to 725 mm (Hg) absolute pressure. The inner (HV) electrode is supported by a single lead at one end, and the outer (signal) electrode by 3 leads on the opposite end. All leads are brought through reinforced glass seals in the envelope.

B. High Voltage Filter:

An RC pi filter constructed on the HV enclosure end connects via a coupling socket to the single center HV electrode lead. It has a time constant of 1 second. It is designed to allow a maximum ΔHV (on the chamber) of 10V at the maximum estimated dose expected to quench a magnet (10 rads); or a maximum ΔHV of 1.1V at the estimated maximum dose rate expected to quench a magnet (160 rads/sec). This filter also isolates the BLM chassis HV supply from each BLM in the daisy chain. A shorted BLM (worst case) is therefore only capable of causing a 0.03 mA load to the HV supply.

C. BLM Chamber Enclosure:

The BLM chamber enclosure consists of an aluminum cylinder, 2 1/2 in. O.D. x 8 7/8 in. long, with 2 - 1/4 in. thick aluminum end caps. One end cap contains the BNC signal connector and the teflon insulated socket/support structure for the 3 lead signal electrode end. The other end cap contains 2 SHV connectors (for HV daisy chain) and the pi filter assembly with the single HV electrode support socket.

D. Miscellaneous:

The nominal inter-electrode capacitance of the assembled BLM ion chamber is 3.3 pF. The chamber has a sensitivity of 70 ncoul/rad. The chambers are mounted to a bracket welded on each spool piece, with additional units mounted in various locations around the ring.

III. BLM Electronics Chassis:

The BLM box contains the following subsystems: low voltage power supplies, external device buss interface and address decoding, down loaded control registers and status latch, high voltage power supply, log integrator amplifiers, ADC, alarm/abort/status group, and service request circuit. The circuit resides in a 5 1/4" relay rack chassis. All subsystems except power supplies are on the mother board. The log integrators are daughter boards.

A. Low Voltage Power Supplies:

The low voltage supplies are mounted on an aluminum plate at the front of the chassis. The supplies are Lambda LOS series, wired as ±15V and +5V. The supplies are rated as follows: +5V, 6A; +15V, 2.8A; -15V, 1.4A. The model numbers are: LOS-Y-5, LOS-Y-15, and LOS-Z-15, respectively. The supplies are adjustable by screwdriver. On the mother board, a reference voltage is supplied using the +15V supply. It is generated at U14 and is adjusted by R93.

B. External Device Buss Interface and Addressing:

The following external device bus signals are used: D0-D7 (bidirectional), A0-A7, $\overline{\text{WST}}$, WEX, $\overline{\text{REX}}$, and $\overline{\text{SVRQ}}$ (service request described later).

1. Addressing:

Device select is accomplished by "anding" A7 and A6 at U82. A5 is used as the alternate addressing bit (E0-FF is the normal address). Device select equations are: $A7 \cdot A6 \cdot A5$= E0-FF, $A7 \cdot A6 \cdot \overline{A5}$= C0-DF. The jumper controlling this uses A5 (normal) or $\overline{A5}$ (alternate) at U75. A4 selects upper 16 bytes of the memory map, and $\overline{A4}$ the lower 16 bytes. The upper 16 bytes is the 16 channel ADC. A $\overline{SEL1}$ (U81-6) must be generated to access the ADC. For normal addressing, the address bit pattern must be 1111XXXX, where XXXX is the ADC channel. The 4 lower address lines go to the output address select lines of the dual port memory for the ADC (U33 and U44). The read write registers and status latch for down loaded data can be accessed when a $\overline{SEL0}$ (U81-8) is generated. The bit pattern would then be 1110XXXX, where XXXX is the address of the RWR. The 4 lower addresses for the RWR's go to two sets of 1 of 16 decoders consisting of U69, U70, U71, and U72. Here they are "anded" with WEX and $\overline{REX}$ to create individual $\overline{WEX}$ and $\overline{REX}$ for each RWR.

2. $\overline{REX}$, WEX, $\overline{WST}$:

Reading and writing to and from the chassis is accomplished by using $\overline{REX}$ (read external), WEX (write external), and $\overline{WST}$ (write strobe). REX, WEX, and $\overline{WST}$ within the addressing range of the chassis will generate their internal counterparts: $\overline{REX}$ (U81-11), WEX (U75-13), and WST (U75-1). The ADC is accessed by generating a $\overline{SEL1}$ (U7-5) and internal $\overline{REX}$ (U7-6). WEX and WST are not needed, as the ADC is read only. Individual $\overline{REX}$ and $\overline{WEX}$ for the RWR's are generated at U69, U70, U71, and U72 as described previously. The individual $\overline{REX}$ signals operate the tristate read back controls of the RWR's, consisting of U35, and U55 through U64, pins 1 and 19. Individual $\overline{WEX}$ signals select which RWR to write to. They are tied to the clock enable inputs of their respective D-flipflops (U45 through 54 pin 1) and clear status latch (U68-12 & 13). Internal WST is bussed to the clock inputs of the RWR's (U45 through U54 pin 11), and clear status (U68-9). WST can be common to all RWR's because data can only be written if there is an individual $\overline{WEX}$ signal for that RWR.

3. Data:

The bidirectional data of the EDB accesses the 16 channel ADC and the RWR's. U73 and U74 act as isolation between the ADC and the RWR's. The data from the dual-port memory of the ADC is placed on the buss during $\overline{\text{REX}}$ "and" $\overline{\text{SEL1}}$. The ADC cannot be written to. The RWR's consist of 74LS377 octal latches and 74LS244 octal tristate buffers. During $\overline{\text{REX}}$ "and" $\overline{\text{SEL0}}$, the buffers place the data from the "Q" outputs of the latches onto the buss. When writing to the RWR's during WEX "and" $\overline{\text{WST}}$ "and" $\overline{\text{SEL0}}$, the data from the buss is clocked into the latches. The status latch, addressed along with the RWR's, consists of 8 D-type flipflops (74LS74) and two inverting octal buss buffers (74LS540, U34, U35). During $\overline{\text{REX}}$, the data from the D-flipflops is inverted onto the buss (a "1" on the buss equals true). During WEX and $\overline{\text{WST}}$, data in the status latch can only be cleared, not set (a "1" on the buss equals clear).

C. Down Loaded Controls:

The down loaded controls consist of ten pairs of 74LS377's and 74LS244's (RWR's). Included here is the status latch because of its association with the RWR's. Their purpose is to set and read back control parameters for the BLM system. Their uses are as follows (normal address in parenthesis): high voltage (EF), MADC channel select (EE), high/low field select and service request mask (ED), high field alarm (E7), low field alarm (E6), high field abort (E5), low field abort (E4), detector mask high byte (E3), detector mask low byte (E2), status mask (E1), and special case, status latch (E0).

1. High Voltage:

The high voltage (EF) is set by RWR pair U52 and U62. The digital data drives a current output DAC (U42) into a current to voltage converter (U31). This voltage is applied to a power voltage follower (U65, Q7) which drives a DC-DC converter to make high voltage (+3000 VDC a + 0.5 mA). The HV is then made available at the rear panel via RG58/SHV flying lead. The HV is sampled with a voltage divider buffered by U67. The buffered sample feeds HV over/under comparator (U2), another voltage divider to the ADC, and a hardware overvoltage protection circuit (U66 and Q6). Primary over current protection is done by Q5, which is "ored" with HV over (U66, Q5) to shutdown the voltage follower U65. HV is adjusted by R134.

2. MADC Channel Select:

The MADC channel (EE) is selected by the lower 4 bits of RWR pair U53 and U63. These 4 bits are applied to the address inputs of the 16 channel analog multiplexer (U9). The analog input selected is buffered by U13 and made available at the rear panel via a BNC flying lead. Addresses 0 through B correspond to BLM log integrators 0 through 11. Addresses C, D, and E are Vref, +15V, and -15V. The output of the buffer is normalized to +5V for the nominal value of these inputs. Address F is the high voltage channel. Here, a high voltage of +3000V gives an output of +9V, proportional.

3. High/Low Field Select and Service Request Mask:

The high/low field select and SVRQ mask (ED) use bit 0 and bit 1 of the RWR consisting of U54 and U64. The high/low field select bit (bit 0) goes to two 16 line to 8 line digital multiplexers (U38, U39, U40, U41). A "0" on the high/low field select is low field, a "1" is high field. The SVRQ mask (bit 1) goes to U17-12. A "0" for this bit is unmask, a "1" mask.

4. High/Low Field Alarm/Abort Levels:

High/low field alarm and abort (E4, E5, E6, E7) group is dealt with as a unit because of their similarity and use. The high field alarm RWR (E7, U50 and U60) and low field alarm RWR (E6, U51 and U61) outputs go to a 16 line to 8 line multiplexer (U40, U41). The high or low field byte is selected by the high/low field select bit of address ED, bit 0 ("1" = high, "0" = low). The selected byte feeds a current output DAC (U29) which is followed by a current to voltage converter (U30). The voltage output of U30 is used as an analog input to the alarm comparator. The alarm comparison level is adjusted by R132. The high field abort RWR (E5, U48 and U58) and low field abort RWR (E4, U49 and U59) operate in a manner identical to high and low field alarm, with the following exceptions: The current output DAC and current to voltage converter are U27 and U28. The voltage output is adjusted by R128, and is used as an analog input to the abort comparator.

5. Detector Masks:

The detector masks are used to disable a malfunctioning BLM chamber from the system. In some cases, a malfunctioning log integrator can also be disabled. Once the channel has been masked off, that channel can no longer create alarms or aborts. The digitized output voltage of the log integrator may or may not be present in the ADC output depending on which way a jumper is placed on the log integrator board. Detector mask low byte RWR (E2, U45 and U55) services channels 0 through 7. Detect mask high byte services channels 8 though 11 (4 high bits not used). All detector masks are "1" = mask.

6. Status Mask:

The status mask RWR (E1, U47 and U57) is used to inhibit any event (alarm, abort, voltage over/under, missing heartbeat) from setting the status latches (U23, U24, U25, U26). The abort mask also masks the hardware abort on the rear panel. The actual masking is done by 74LS02's (U36 and U37) used as inverted input "ands". The output of the mask will go high and set the latch when both inputs (event and mask) are low. A "1" on the status mask RWR will mask that event. In practice, the status mask is used in conjunction with the status latch.

7. Status Latch:

The status latch group (E0) consists of U34, U35 (74LS540's), U23, U24, U25, and U26 (74LS74's). When the status is read, U35 inverts the "$\bar{Q}$" outputs of the latches onto the data buss. Thus, when an unmasked event occurs, it shows up on the buss as a "1". If the data, that has been read, is written back to the latch, only those bits that have been set will be cleared ("1" = clear). This allows any other event, occurring between reading and writting, to set the latch and not be lost by clearing the origional event. The mask (E1) can be used to ascertain whether a condition, that set the latch, is still present. Assume that one of the status latches is set, then cleared, then masked, then unmasked, then the status read again. That bit will be set again if the condition is still true.

D. Log Integrators:

The log integrator daughter cards are used to convert the wide dynamic range positive current from the BLM chambers into a voltage that is proportional to the log of the input current. The circuit is based on the log characteristics of the emitter-base junction of a transistor. The circuit employs a matched pair of NPN transistors (Q1, 2N2060) as the log elements. They are connected in a summing junction mode with U1 and U2 (CA3140AE's) to keep the input voltage at ground. Q2 acts only as low leakage protection diodes. A voltage divider, R3, R4, R5 (2K, 3K, 5K) provides 8V (Vbias) and 5V (Vref) to R6 and R7 ($5 \times 10^{9}\Omega$). The current from these resistors is applied to the inputs of U1 and U2. The current to U1 is $+1.6 \times 10^{-9}$A (Ibias), and the current to U2 is $+1.0 \times 10^{-9}$A (Iref). The current from the BLM chamber is terminated by R1 (51Ω), then passively integrated by C1 (.47 μF) and R2 (130K), giving a 1/16 second time constant. This input current is then applied to the input of U1 along with Ibias. The outputs of U1 and U2 drive a differential amplifier (U3, CA3140AE) with a gain of approximately 40. The circuit is temperature compensated by R10 (10K ohm sensistor). The output of U3 is the voltage equivalent of the log of the input current of U1, referenced to $+1 \times 10^{-9}$A. The quiescent voltage at this point is normally +0.5V (around 0D from the ADC). At $+1 \times 10^{-5}$A, the output will be approximately +10V (FF from the ADC). This output, from each log integrator, is made available at the rear panel via a BNC flying lead. The next stage (U4, CA3140AE) is basically a follower with two outputs that can be gated off. The output to the ADC is reduced by one half, by R21(2K) and another 2K on the mother board, to make it voltage compatible with the ADC. This output is jumper selectable to be maskable or unmaskable. The other output is an analog "or". This output, tied common to all log integrators, goes to the alarm/abort circuit. The log integrator with the highest voltage (greatest input current) at this point is the one that drives the alarm/abort comparators. In the event of a malfunctioning BLM chamber or a log integrator with a bad input stage this output can be masked off. This is done by applying a LSTTL "1" to the mask input, which forces the "or" output to a negative voltage. No alarms or aborts can then be generated by this channel.

E. ADC:

The ADC is an 8-bit, 16-channel multiplexed, analog to digital converter (U22, ADC0817CCN), with 16 bytes of dual port memory (U33 and U34, AM29705PC). The 16 inputs are the 12 log integrators, Vref sense (normalized to 1/2 ADC F.S.), +15V sense (normalized to 1/2 ADC F.S.), -15V sense (normalized to 1/2 ADC F.S.), and HV sense (normalized to +3000V equals 9/10 ADC F.S.). The diodes and resistors at the inputs to U22 are for protection. It is important to note that the ADC uses the +5V supply as its reference voltage. The control of the ADC chip is accomplished by the use of a sequencer consisting of U19 (74LS193), U11, and U20 (74LS138's). The sequencer performs the following functions: U20-15 increments the channel counter (U21), which advances the input multiplexer of U22 to the next channel. U20-14 sets flipflop U12-4 to start sampling, using U32 (sample and hold, AD582KD). Also at this time, the internal channel address is latched. After a time delay, U20-11 resets flipflop U12-1 to stop sampling and start holding. Immediately after this, a start convert pulse is generated (U20-10). There is then another delay to allow the ADC chip (U22) to do the conversion for that channel. After the delay, an update memory pulse is generated (U11-7). This pulse is narrowed to 50 nsec by the one shot (U12-8). If the ADC memory is being read ($\overline{\text{REX}}$ "and" $\overline{\text{SEL1}}$) during this time, the memory will not be updated. If the memory is not being read, a write memory pulse is generated at U8-6. At this time, the ADC data for this channel is written into the dual port memories (U33 and U44). The ADC clock is 20 MHZ to make 50 nsec pulses for the updating circuitry (U8). The 20 MHZ clock is counted down by U10 (74LS393) to make 625 KHZ for the ADC chip conversion clock, and to 78.125 KHZ for the sequencer. Since the sequencer is really a divide by 16 counter, it takes 204.8 µsec to convert one channel. Every 3.2768 msec, all 16 channels are updated in the memory. To read the ADC (can't write to it), $\overline{\text{REX}}$, $\overline{\text{SEL1}}$, and address FX (X is channel number) must be used. The "F" part of the address generates a $\overline{\text{SEL1}}$ that, when "anded" with $\overline{\text{REX}}$ at U7-5 and U7-6, interrupts updating of the ADC memory and places the data from the addressed channel onto the buss. Reading and writing of the ADC memory is done asynchronously. If the ADC stops converting, a missing heartbeat signal is generated at U43-5 (1/2 74LS123).

F. Alarm/Abort/Status Group:

The alarm/abort/status group consists of the comparators and signals that can set the status latches (E0). Specifically they are: $\overline{\text{abort}}$ (1/2 U1), $\overline{\text{alarm}}$ (1/2 U1), $\overline{\text{HV}}$ under (1/2 U2), $\overline{\text{HV}}$ over (1/2 U2), $\overline{\text{+15V o/u}}$ (U5), $\overline{\text{-15V o/u}}$ (U4), $\overline{\text{+5V o/u}}$ (U3), and $\overline{\text{missing heartbeat}}$ (U43).

1. Alarm/Abort Comparators:

The alarm and abort comparators (U1, LM393) use the analog "or" from the log integrators to compare to the preset alarm and abort levels from U30 and U28. When the comparison levels are exceeded, the outputs of the comparators will set the unmasked alarm/abort status latches. In addition, the unmasked abort will cause a hardware abort signal (U82-6) to be generated on the rear panel BNC. The abort signal can drive 50 ohms (74S140).

2. High Voltage Over and Under:

The high voltage over and under comparators (U2, LM393) sample the high voltage divider (U67-6) as their input. The comparison levels are 10V and 3V as determined by R31 (5.6K) and R30 (2.4K). A HV under signal is generated when the high voltage is less than +1000V, and a HV over when high voltage exceeds +3333V. These two signals set their associated unmasked status latches.

3. Low Voltage Power Supply Comparators:

The three low voltage power supply monitoring comparators (U5, U4, U3) use the low voltage power supply voltages normalized to +5V as their input. The comparison levels (+5.5V for over and +4.5V for under) are determined by the voltage divider consisting of R63, R64, and R65 (9.1K, 2K, and 9.1K). When the normalized supply voltage is over or under the preset level, the comparator generates the appropriate o/u signal, and sets its associated unmasked status latch. In addition, the front panel power supply monitor LED is turned off.

4. Missing Heartbeat Detector:

The missing hearbeat signal from the ADC section is generated at U43-5 when there is no longer an end of conversion pulse from the ADC chip (U22). The missing heartbeat signal sets its associated status latch.

G. Service Request:

The service request group consists of U16, U17, and U18. All of the status latch bits are "ored" at U16. Any status bit that is set can generate a SVRQ. This SVRQ is "nanded" with the SVRQ mask at U18-12 and U18-13 to create $\overline{\text{SVRQ}}$ for the EDB. At power-up, the service request is masked off, regardless of the contents of address ED. After the first write to ED, the actual condition of the SVRQ mask can be read. $\overline{\text{SVRQ}}$ is an open collector signal, to be "ored" with other devices on the EDB.

IV. References:

The documents concerning the BLM system have been assigned the reference numbers 1680.00 ES 158450 through 1680.00 TM 158499 (this document).