

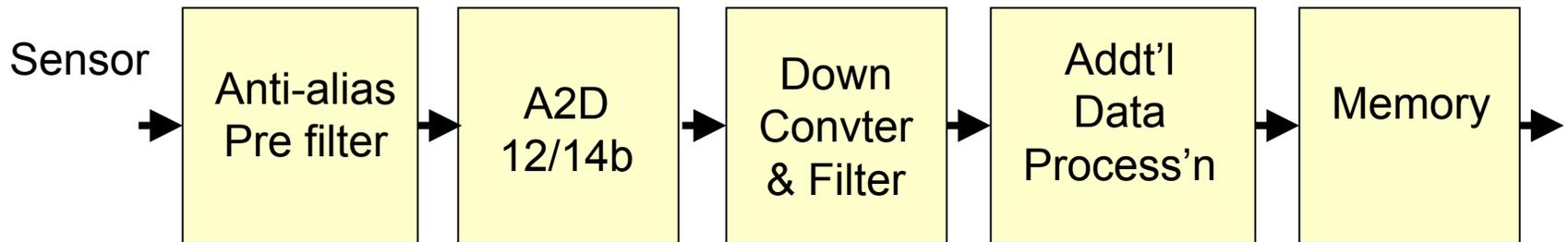
BPM Hardware

Vince Pavlicek CD/ESE

Hardware Outline

- Review the data processing architecture presented by Jim.
- Present the constraints we put on our search for candidate hardware.
- Present the search process and the current status.
- Outline the next steps.

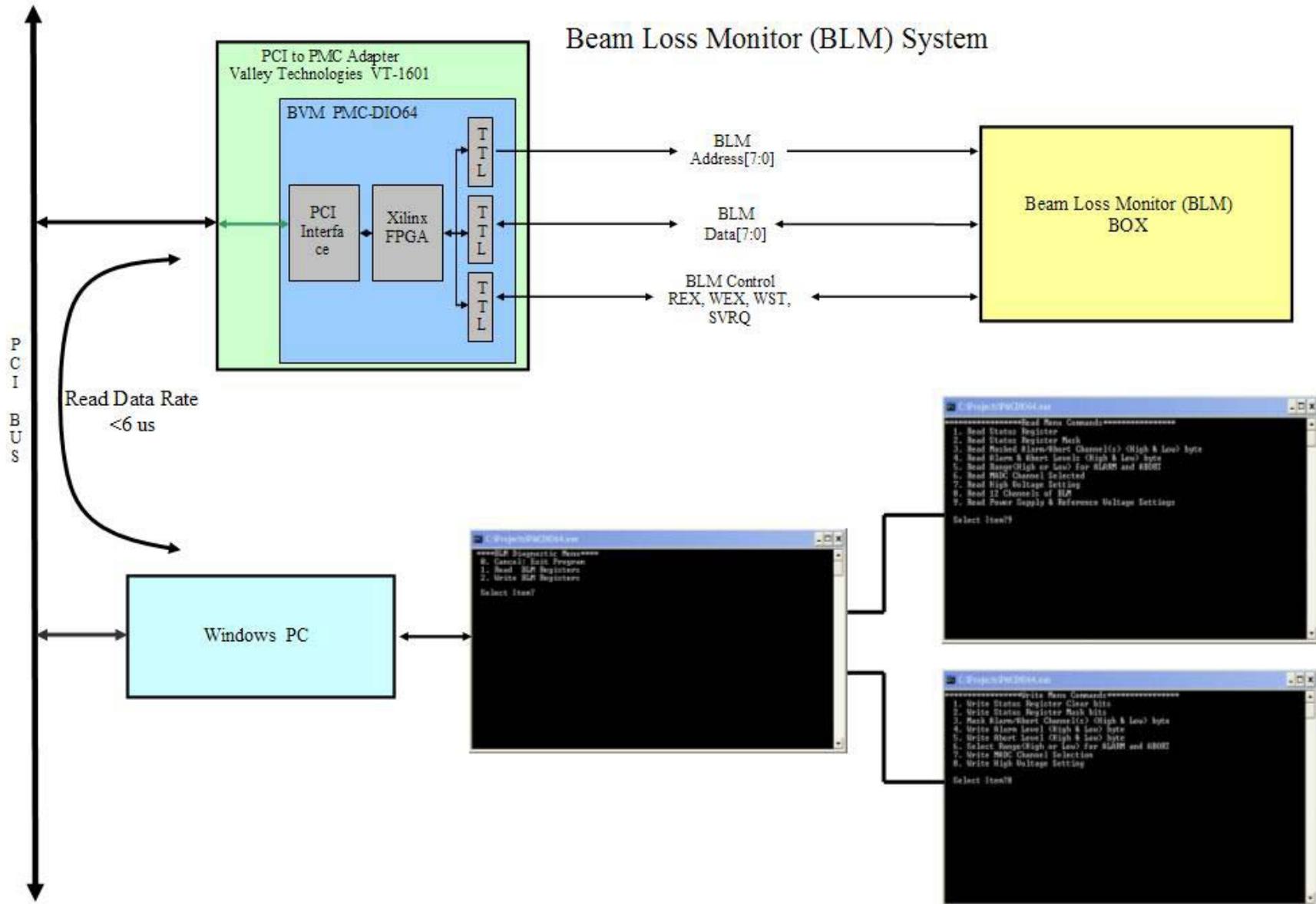
Architecture Block Diagram, Data Path



Initial Constraints

- ❑ The candidate hardware should be able to implement the chosen data processing architecture.
- ❑ We did not want to start from scratch with a new design.
- ❑ Therefore, we looked at current examples of BPM DA hardware.
- ❑ The BLM will not affect this selection as it will be independent of the BPM raw data path.

Beam Loss Monitor (BLM) System



Initial Hardware Field

- Recycler and NUMI Echotek boards
- MI damper boards
- E-Cool DSR boards
- BNL RHIC BPMs
- Commercially available Analog to Digital Converter and Digital Signal Receiver boards.

Summary First Candidates

Module	Channels and A2D	Data Processor	Form	Num	System Use	Stage
Echotek	8ch x 80 Msps x 14b	DDC	VME	120	Recycler, NUMI	Product
DSR	8ch x 65 Msps x 14b	DDC + DSP	VXI	25	Ecool, MI BPM	Product
Damper	4ch x 212 Msps x 12b	FPGA logic +DSP	"NIM"	5	MI damper, RR	Proto

Individual Issues

Module	
Echotek	Expensive, least flexible data processing, output FIFO limits flexibility.
DSR	Has some constraints on timing and data processing flexibility.
Damper	Most capable. Needs most engineering. I/O is DSP to Ethernet. Only 4 channels.

DSR=Digital Signal Receiver DDC=Digital Down Converter DSP=Digital Signal Processor

Added Candidates

- Add modified Echotek with output FIFO replaced by dual-port RAM.
 - Echotek2
- Add DSR board with faster DDC with new data buffers and DSP with larger memory.
 - DSR2

Summary Current Candidates

Module	Channels and A2D	Data Processor	Form	#	System	State
Echotek	8ch x 80 Msps x 14b	DDC	VME	120	Recycler	Product
Echotek2	8ch x 80 Msps x 14b	DDC	VME	--		
DSR	8ch x 65 Msps x 14b	DDC + DSP	VXI	25	Ecool, MI	Product
DSR2	8ch x 65 Msps x 14b	DDC + DSP	VXI	--		
Damper	4ch x 212 Msps x 12b	FPGA logic +DSP	"NIM"	5	MI damper, RR	Proto

Individual Issues

Module	Individual Issues
Echotek	Expensive, least flexible data processing, output FIFO limits flexibility.
Echotek2	Expensive, most direct data processing.
DSR	Some constraints on timing flexibility. Most under sampled data.
DSR2	Most under sampled data.
Damper	Most capable. Needs most engineering. I/O is DSP to Ethernet. 4 channels.

Module	Hardware Engineering Tasks	Design		Drafting		Board Fab		Board Checkout	
		FTE	Wks	FTE	Wks	FTE	Wks	FTE	Wks
Echotek	None	0	0	0	0	0	0	1	4
Echotek2	None	0	0	0	0	0	0	1	4
DSR Board	Some traces need to be added for triggering and reset. No major layout changes.	1	1	1	1	1	27	1	4
DSR2 Board	Digitizer and DDC changed to 80MHz versions. FPGA added to handle serial output of DDC, perform preliminary calculations, and interface with DSP.	1	4	1	12	1	27	1	4
Damper Board	DAC components used for dampers need to be removed. External communication circuitry needs to be changed from Ethernet to VME.	1	4	1	12	1	27	1	4
Timing, Cal, BLM	Total design of custom cards.	1	8	1	8	1	21	1	4

Module	On board software/firmware engineering	FPGA Program		DSP Program	
		FTE	Wks	FTE	Wks
Echotek	FPGA may need to handle different triggering schemes	1	3	0	0
Echotek2	FPGA needs new program to deal with data processing, memory management, and new backplane communication protocol.	1	7	0	0
DSR Board	DSP needs new program to deal with new data processing algorithms, different memory management, and different synchronization schemes.	0	0	1	7
DSR2 Board	New FPGA needs program to deal with data processing and DSP communication. DSP needs new program to deal with FPGA communication, new data processing algorithms, different memory management, and different synchronization schemes.	1	7	1	7
Damper Board	FPGA needs to incorporate a digital down converter process with digital filters. It must perform all data processing calculations and memory management. It needs to be modified for new communication protocol.	1	10	0	0
Module	Slot zero (front end) software engineering	Slot Zero Program			
		FTE	Wks		
Echotek	Needs robust, fast bus for continuous acquisition from BPM cards. Needs new program to deal with data processing, memory management, and triggering.	1	10		
Echotek2	Programming of ACNET parameters and implementation of diagnostics communication. Also will need to perform data processing that FPGA is unable to perform.	1	4		
DSR Board	Programming of ACNET parameters and implementation of diagnostics communication.	1	4		
DSR2 Board	Programming of ACNET parameters and implementation of diagnostics communication.	1	4		
Damper Board	New hardware. Requires MOOC interface programming, ACNET parameters, and diagnostics communication.	1	7		

M&S

Numbers	# of BPMs	Total # of signals	Spares	Houses	Spare Crates	
	236	944	142	27	2	
Numbers	Total channels	Total crates	Board/crate timing, cal, BLM	Board Cost of timing, cal, BLM	Total cost timing, cal, BLM	Note: Est. for front-end analog filter
	1086	29	1	\$4,000	\$116,000	\$40/chan

Module	Cost/card	Chan/card	Total Cards	Cost/crate & slot zero controller	Total crates & slot zeros	Analog Filters	Total M&S
Echotek	\$7,400	8	\$1,004,550	\$9,000	\$261,000	\$43,440	\$1,424,990
Echotek2	\$7,600	8	\$1,031,700	\$9,000	\$261,000	\$43,440	\$1,452,140
DSR Board	\$1,900	8	\$257,925	\$12,600	\$365,400	\$43,440	\$782,765
DSR2 Board	\$1,900	8	\$257,925	\$12,600	\$365,400	\$43,440	\$782,765
Damper Board	\$2,200	4	\$597,300	\$9,000	\$261,000		\$974,300

More Spreadsheets

- We have several spreadsheets to help us understand the costs and effort involved with each candidate.
 - Description, engineering, software and M&S were already shown.
 - Summary to First Crate
 - Fabrication
 - Summary to Full system

What's Next

- ❑ The Modified Echotek board is the candidate we will focus on and within the following steps we will pick a point to begin production.
- ❑ We verify proton/antiproton processing with a representative module.
- ❑ We need to understand how we will trigger the boards in all the modes and how we will generate those signals.
- ❑ We need to understand calibration.