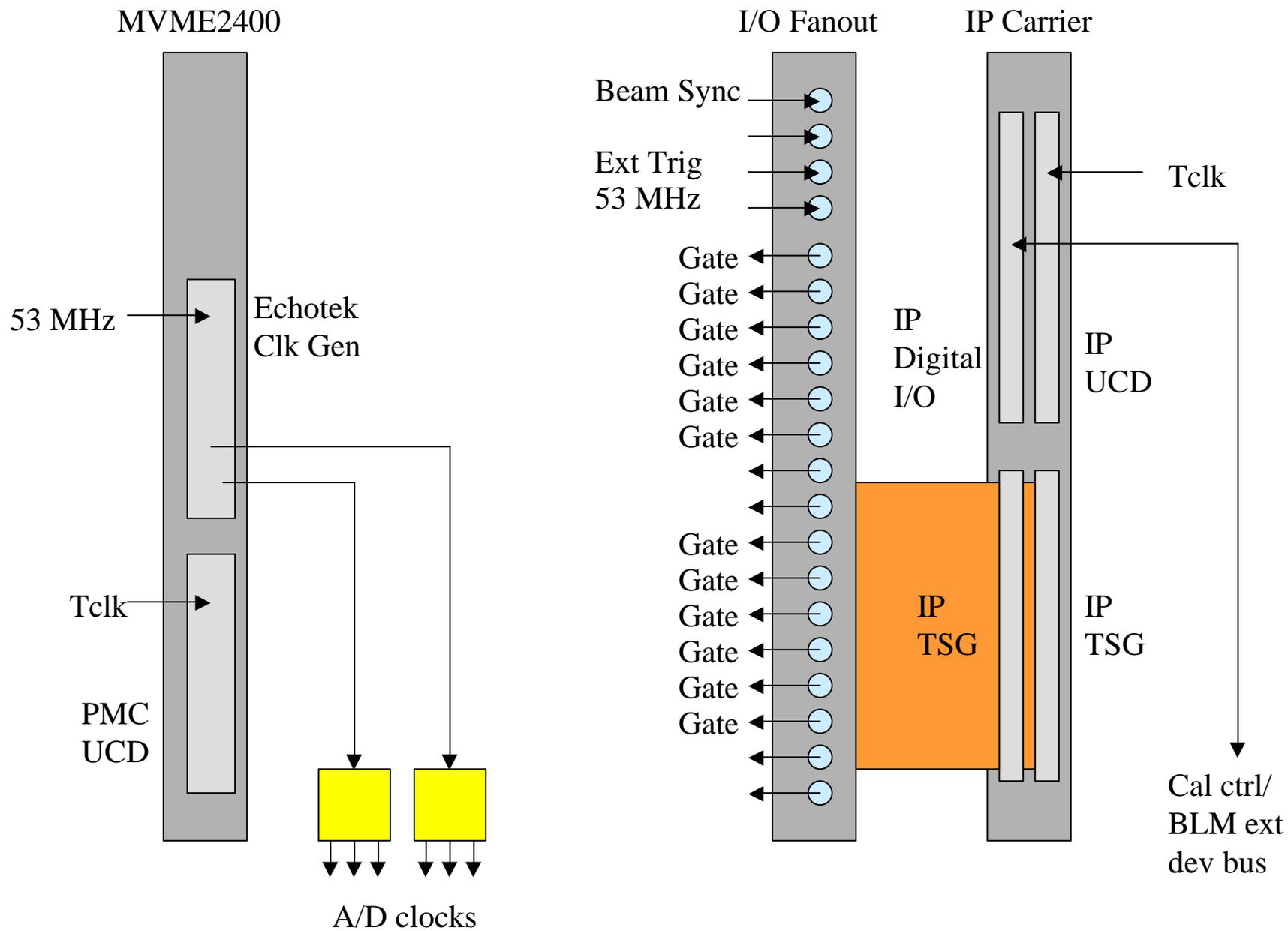


Current (recycler) timing/trigger system appears to be sufficient for TeV BPMs

- add injection event to beam sync
- TSG FPGAs nearly full, but dropping MDAT decoder and 2 of 6 gates frees ~30% space
- could run TSGs at 7.5MHz (instead of 53)
- IP Digital I/O board can drive BLM ext dev bus and calibration



Existing (recycler) timing system

Need to re-layout I/O fanout board to include latest revisions

- suggested additions/changes

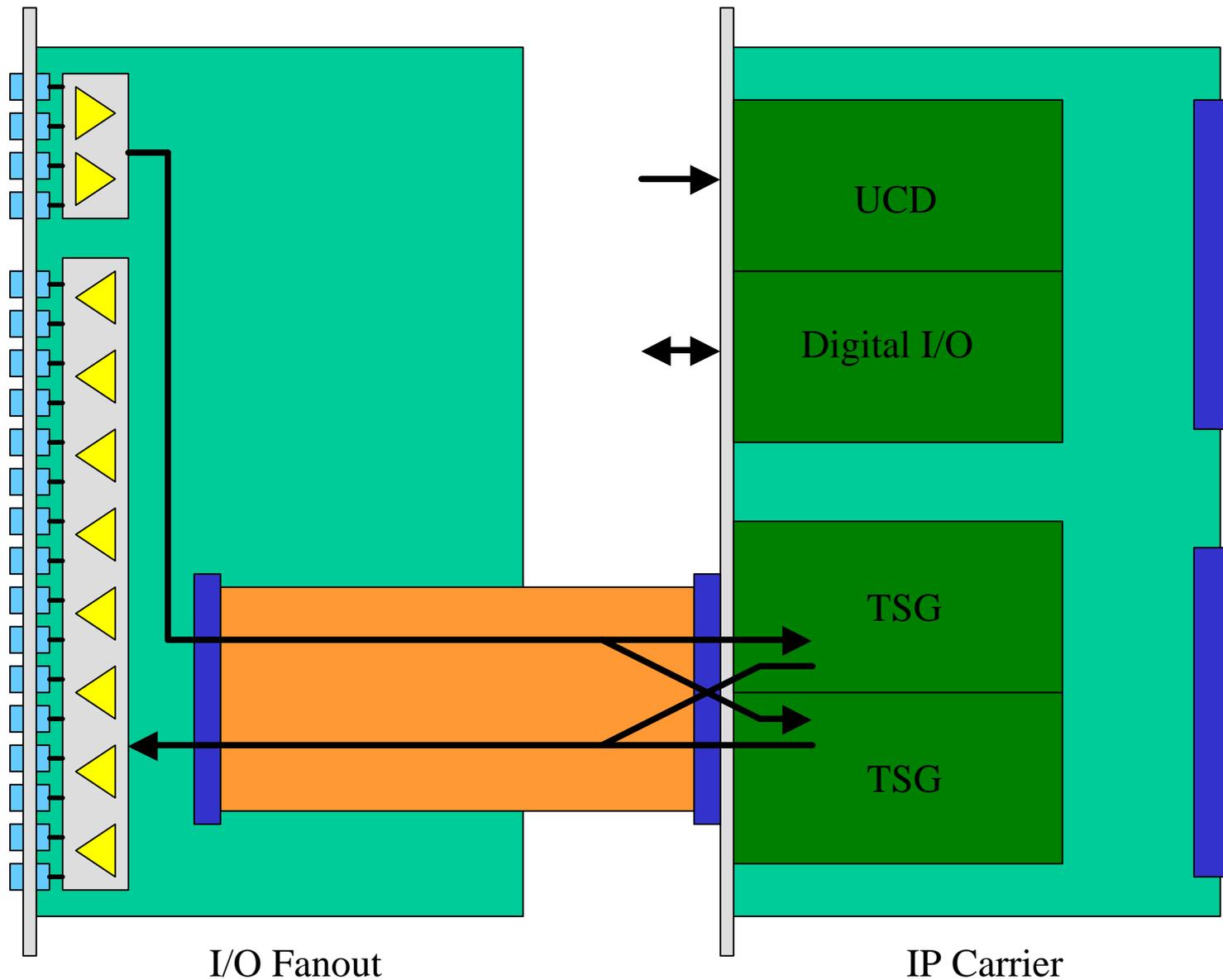
modify number of clock inputs and gate outputs

A/D clock generator?

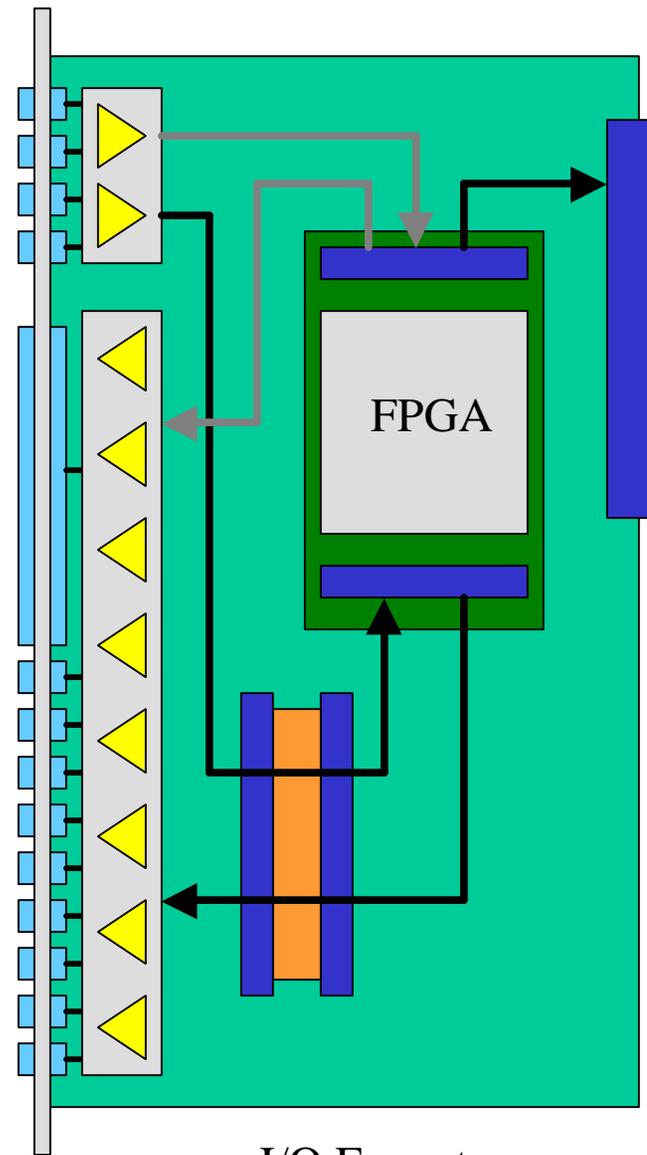
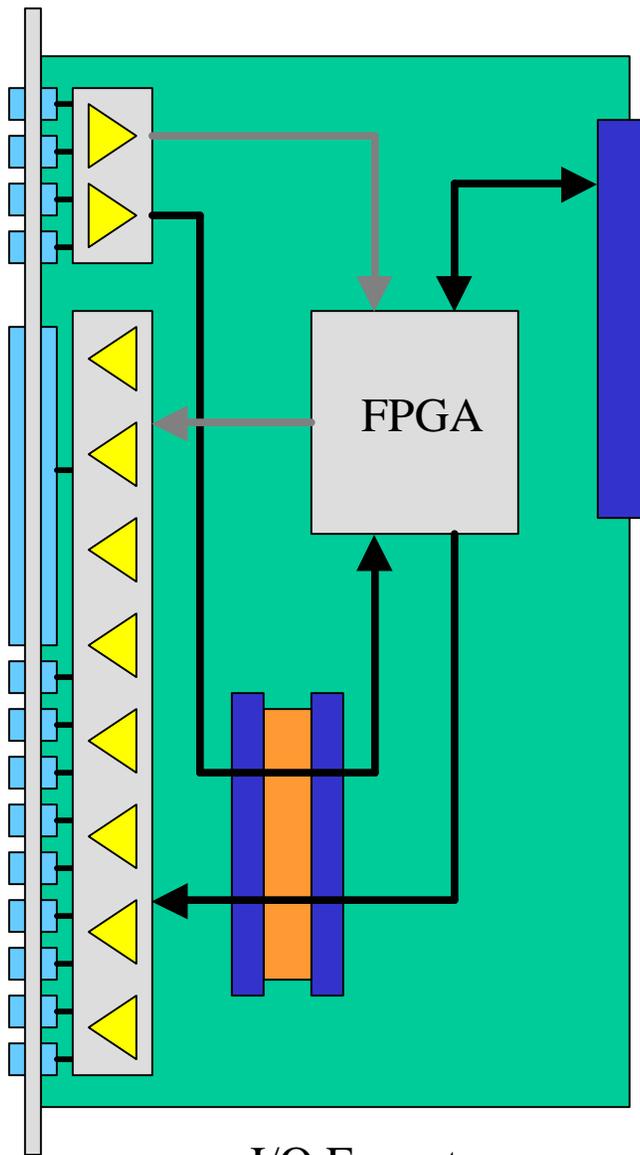
53 MHz repeater

FPGA to incorporate functions currently on IP carrier
(TSGs, Tclk UCD, Digital I/O, VME interface)

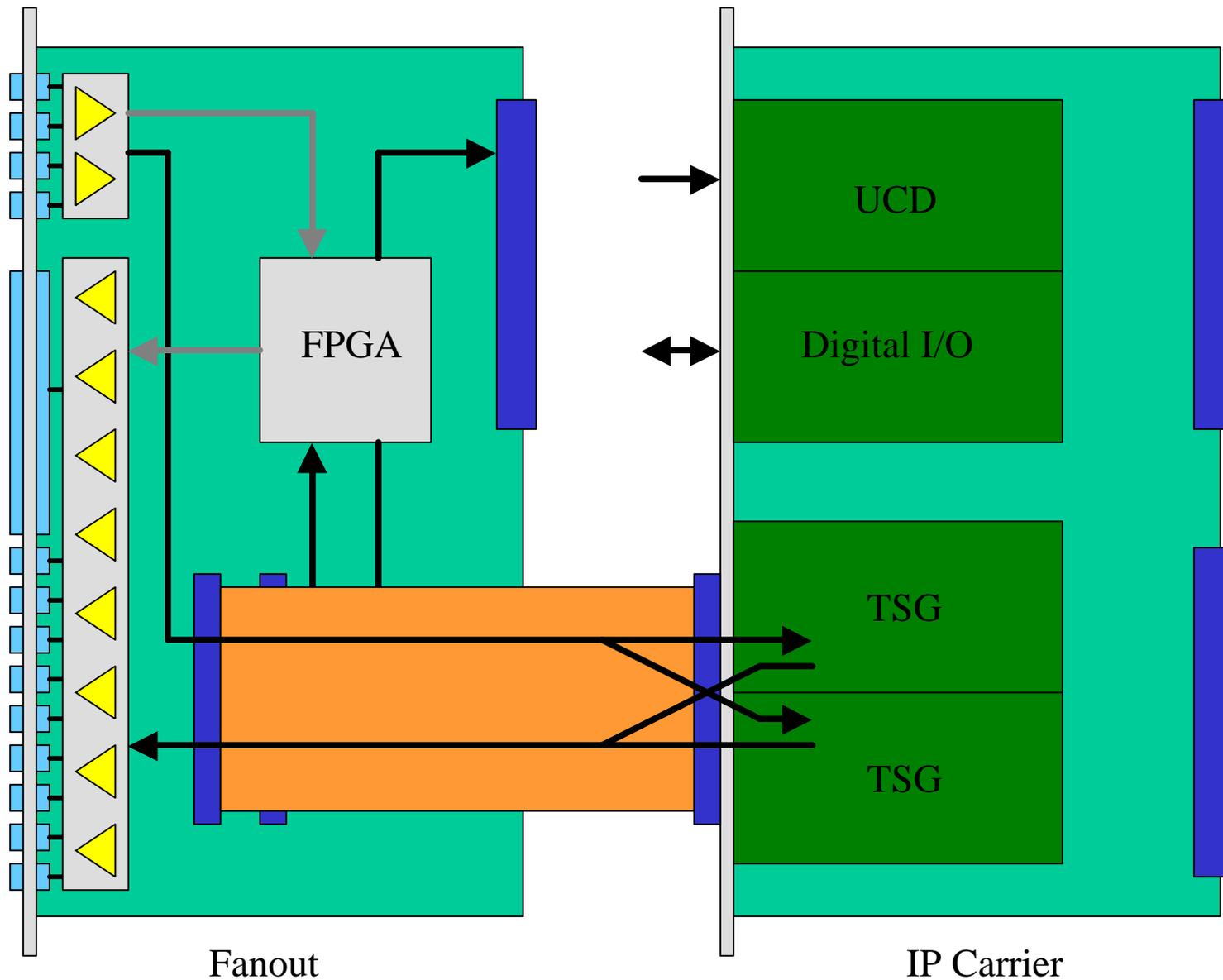
Tclk, beam sync simulator



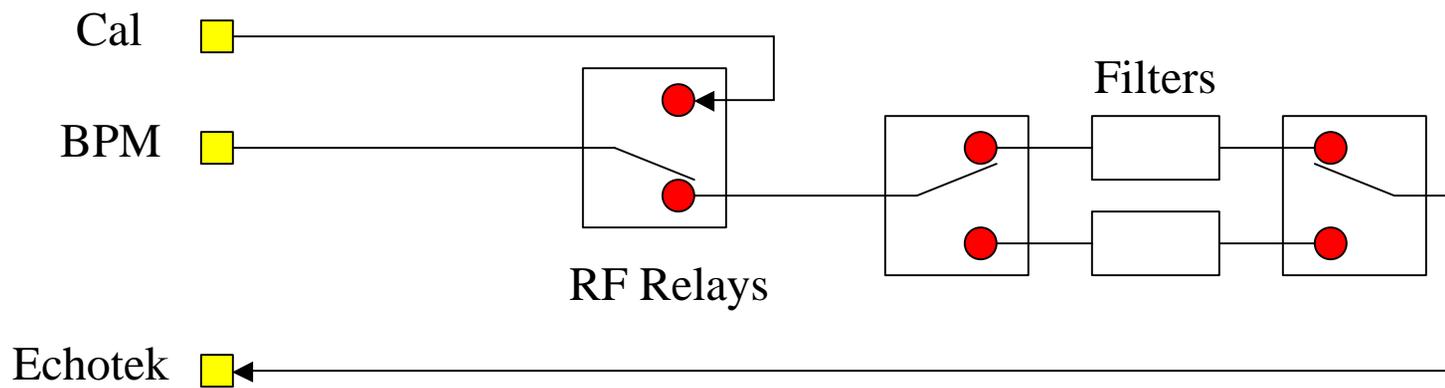
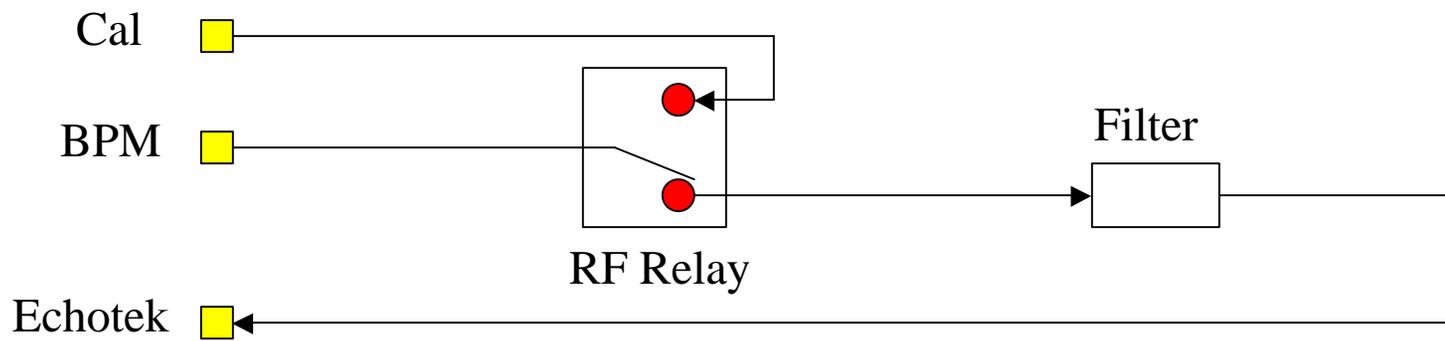
Option 1 Re-layout I/O Fanout board to current revision (no changes) [5 weeks]



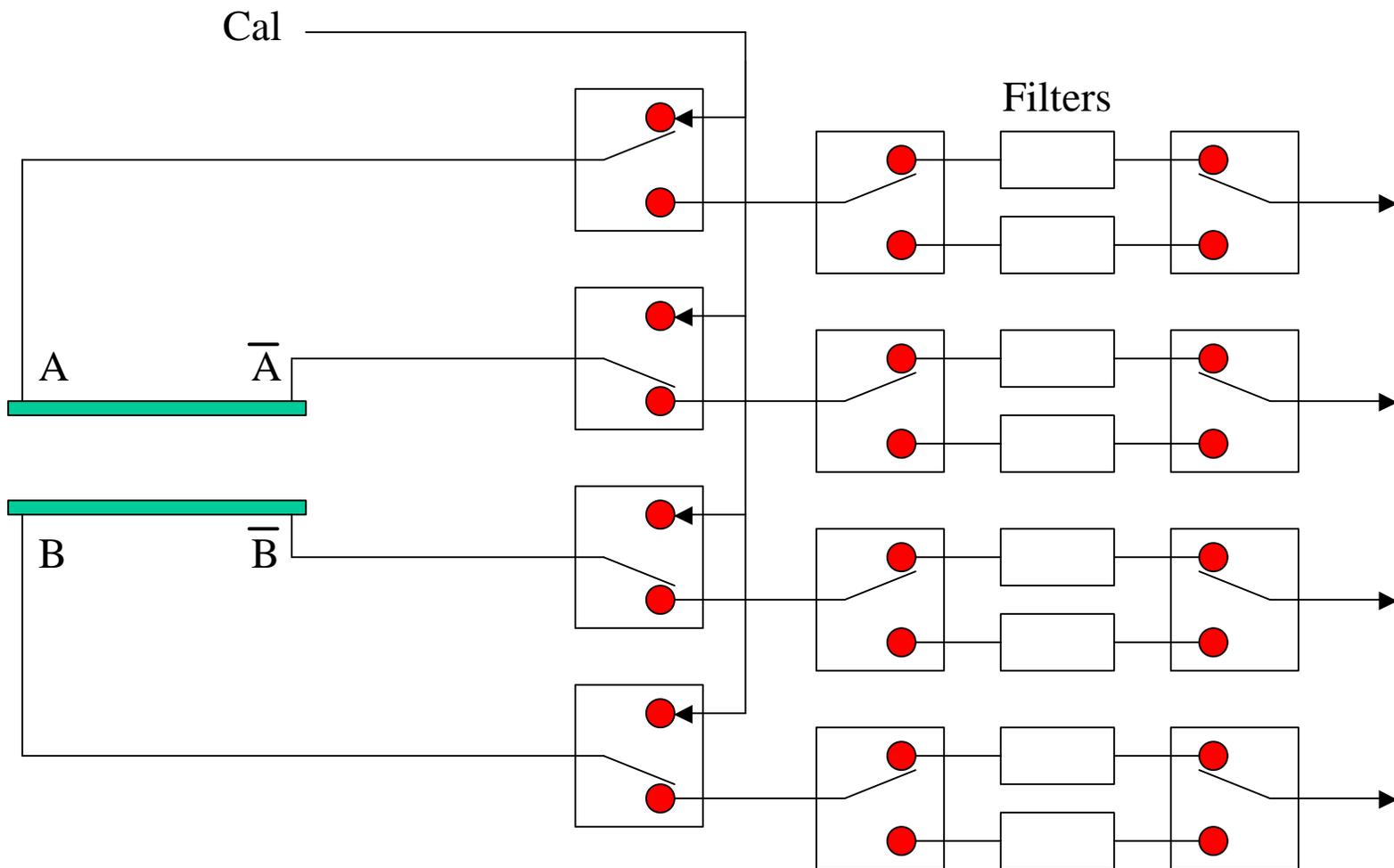
Option 2 Re-layout I/O Fanout board with on-board or mezzanine FPGA [6-7 weeks]



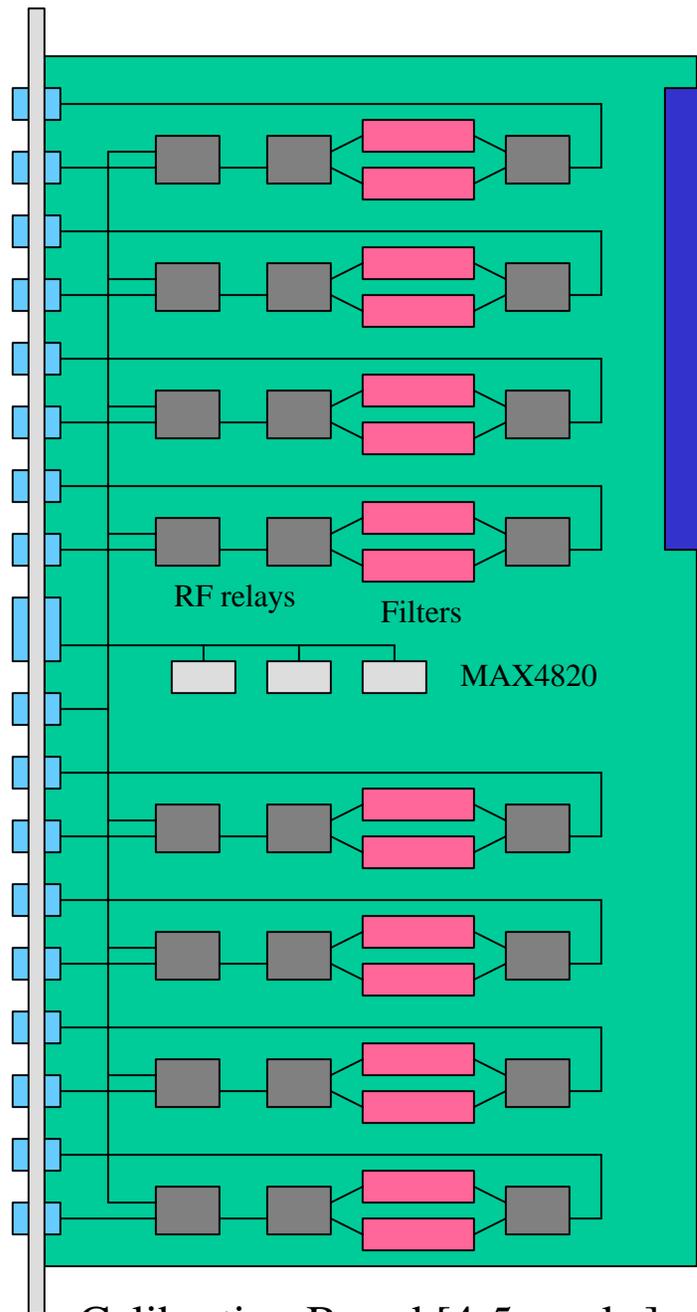
Use existing IP version until firmware is ported to new FPGA



Calibration select (optional filter select)



Calibration signal applied to any one of four BPM ports can be monitored on other three ports.



Calibration Board [4-5 weeks]

