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Electronic Design Document

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Abstract

This document contains the specification for the Beam Position Monitor (BPM) upgrade data acquisition hardware. Expected operating modes and interactions with the BPM software are described. Analog signal processing, timing system and diagnostic circuits are specified in this document. Calibration and diagnostics procedures are described.

The Beam Loss Monitor (BLM) upgrade has become a separate project. References to the BLM system in this document are included where necessary to provide information about the functionality of the existing system. It is expected that the BLM upgrade project will supersede and replace functions described in this document before the BPM hardware is complete.

Overview

This document describes the hardware needed for the data acquisition component of the Tevatron Beam Position Monitor (BPM) upgrade project. The data acquisition (DA) hardware will digitize the analog position signal from the BPM sensors, digitally filter the signals and make them available to a VME front-end computer. The DA could also provide the interface to the Beam Loss Monitor (BLM) circuitry through the External Device Bus (EDB) to replace the functionality of the existing system. Figure 1 shows the functional block diagram and the different elements involved with the BPM upgrade project.

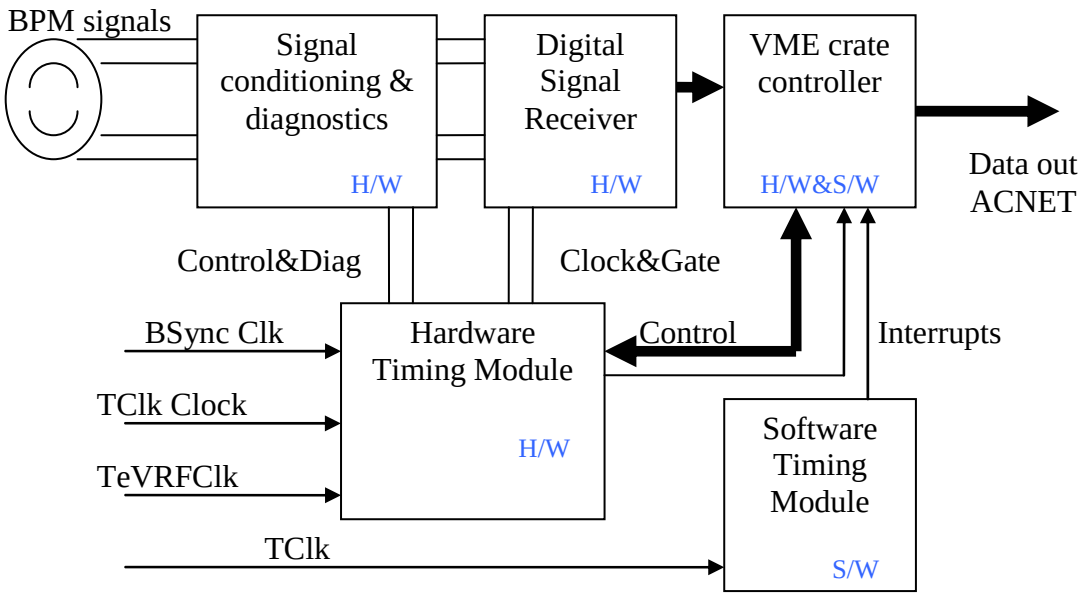


Figure 1 BPM Front End Functional Block Diagram

The hardware functions described in Figure 1 are implemented in four modules that match the hardware blocks above. The signal conditioning and diagnostics are implemented on the Filter module being designed at FNAL. The Digital Signal Receiver (DSR) is a Commercial-Off-The-Shelf (COTS) module from Echotek Corporation, the ECDR-GC814/8-FV2. The timing functions are implemented on the VME Timing Generator Fanout module designed at FNAL. The VME sub rack controller is a COTS Single Board Computer from Motorola Corporation, the MVME2400

Beam Position System

Sensor

The Tevatron BPM sensors[1 and 2] are two opposing curved stripline plates approximately 18 cm long along the beam and oriented to partially surround the beam. Each plate subtends approximately 110 degrees of the full circle around the beam. The circular aperture of the pair (the diameter of the opening) is 6.6 cm. There are connections at both ends of each plate, one connection emphasizing the proton direction of flight and the other the anti-proton direction. The signal taps are at the ends of the individual plates. The convention for the naming of the four signals from a specific BPM sensor are a letter designator for each of the two plates, the A plate, and the B plate, and whether it is the proton end or the anti-proton end. Each of the four BPM signals is treated identically in this Data Acquisition (DA) system except for a resistive attenuator which matches the sensor voltage to the input voltage range of the Echotek module and can also be used to approximately match the proton and anti-proton signal amplitude ranges. The signal of interest is the amplitude variation of the sensor signals as the beam position moves in the sensor but the amplitudes are also proportional to the number of particles passing through the sensor and to the bunch length. In 2004 the bunch size based variation of the amplitude of the proton signals at the proton outputs is approximately 5 times as large as the anti-proton signal at the anti-proton outputs. The 236 Tevatron sensors are on the end of quadrupole magnets in the beam tunnel and the BPM DA electronics modules are in service buildings around the ring. 200 to 300 meter long RG-8 cables bring the sensor signals to the DA system and the Tevatron Filter board.

BPM Data Acquisition System

The BPM signals pass through the Tevatron Filter board for amplitude conditioning and band pass filtering. The filter is centered at the 53.104 MHz accelerator RF frequency with a bandwidth of approximately 10 MHZ. The filter specifications are in Beams Document #1165. This module also has the capability to switch in a diagnostic signal and drive that signal out to the sensor or back toward the Echotek module input. By sequentially driving one output of a sensor and digitizing the other three sensor signals the general condition of that sensor and its associated cable plant can be determined.

Short coaxial cables move the signals from the Tevatron Filter board outputs to the Echotek commercial digital signal receiver module that is the Analog to Digital converter and main signal processing element. On the module, the sensor signals are converted from analog to digital representation, passed to a Digital Down Converter (DDC) signal processing chip for base banding, filtering and then placed in memory that is accessible through the VME backplane bus. The data movement is controlled by firmware in a reprogrammable FPGA device on the module. The VME sub rack controller is a Motorola MVME2400 type processor that controls the data acquisition process. The software that resides on the front-end microprocessors, also referred to as the Data Acquisition (DA) software, is described in Beams Document #860, Tevatron BPM

[1] The Tevatron Beam Position and Beam Loss Monitoring Systems (Beams-Doc-806)
[2] Fermilab Energy Doubler Beam Position Detector (Beams-DOC-809)

Upgrade Software Specifications for Data Acquisition. The system timing is controlled by the VME BPM Timing Generator Fanout module. The TGF timing is based on three Tevatron timing signals. 1) the Tevatron RF Clock (RFClk) at 53.104 MHz which is synchronous to the Tevatron beam, 2)Tevatron Beam Sync (TVBS), running at 7.5 MHz synchronous with the RFClk and containing some Tevatron commands and the encoded turn marker, encoded as 0xAA, and 3) Tevatron Clock (TClk) running at 10 MHz and containing accelerator-complex-wide commands.

The sensor front-end electronics depicted in Figure 1 are contained within a VME sub rack holding a series of pairs of Tevatron Filter boards and BPM VME digitizing boards, the BPM Timing Generator Fanout card, the sub rack controller and, if necessary, BLM interface hardware. Figure 2 illustrates the organization of the cards in the BPM VME sub rack. One sub rack can hold the necessary electronics needed for a service building (sometimes called a house). There are 30 service buildings or houses around the Tevatron ring, 27 of them contain BPM electronics and each BPM house has up to 6 BPM digitizing boards. There are also up to 23 BLM digitizing boards in separate analog crates. Table 6 is the current organization of BPM and BLM sensors relative to the service buildings.

The BPM digitizing modules are Echotek module ECDR-GC814/8-FV2, and each module digitizes signals from 8 channels. An individual BPM sensor generates information on 4 channels – the A and B plates for the proton end of the sensor and the A and B plates for the antiproton end. Therefore one Echotek module will be capable of accepting signals from two BPM sensors. The digitized output that results from each channel of the digitizing module may be sent on for further processing or be used to generate a calculated position when processed with data from the matching plate channel. The details are in the Software Specifications document. If the output is the digitized and filtered signal data, each channel is actually represented by two components: a real (Q) and imaginary (I) part. The digital filtering on the Echotek module can also be disabled allowing a raw, oscilloscope type view of the signal.

The operation of the Echotek module is controlled by two inputs that are common for all eight channels. They are the CLK and SYNC signals. The digitizing clock paces the Echotek module and comes from the BPM Timing Generator Fanout (TGF) Module. A phase-lock-loop on the Timing module creates a clock output that has a fractional relationship to the Tevatron RF clock frequency. TeV RF is approximately 53.104 MHz. The Echotek clock is $7/5^{ths}$ or approximately 74.346 MHz. This means that the 53.104 MHz signal is technically under-sampled but the signals-of-interest are modulated onto that RF signal and filtering and signal processing techniques allow the module to extract those signals-of-interest. The digitization process can be gated, singly triggered or triggered for a specified number of samples by the SYNC signal. SYNCs are generated in the TGF and normally initiated with respect to the Tevatron-wide TCLK signal which carries Main Control Room (MCR) commands and state information. There are two TCLK decoders in a given sub rack; one on the sub rack controller, implemented in a PMCUCD module mounted on a PMC slot and one implemented within the TGF Module. The TCLK decoder on the TGF can initiate digitizing sequences enabled on selected TCLK commands and can add fixed delays relative to the Tevatron turn marker

($AA), with a resolution of one RFClk period, in order to remove cable delays (with a resolution of one RFClk period) or to time-in similar actions between the widely separated service buildings around the Tevatron ring. The TGF card is capable of finer delay resolutions using the digitization clock or optional Phase Lock Loop outputs.

The ACNET/MOOC software infrastructure and applications can also be triggered by interrupts generated by the same TCLK signals that are decoded by the PCMUCD card and this is discussed in detail in front-end software design document (#1067).

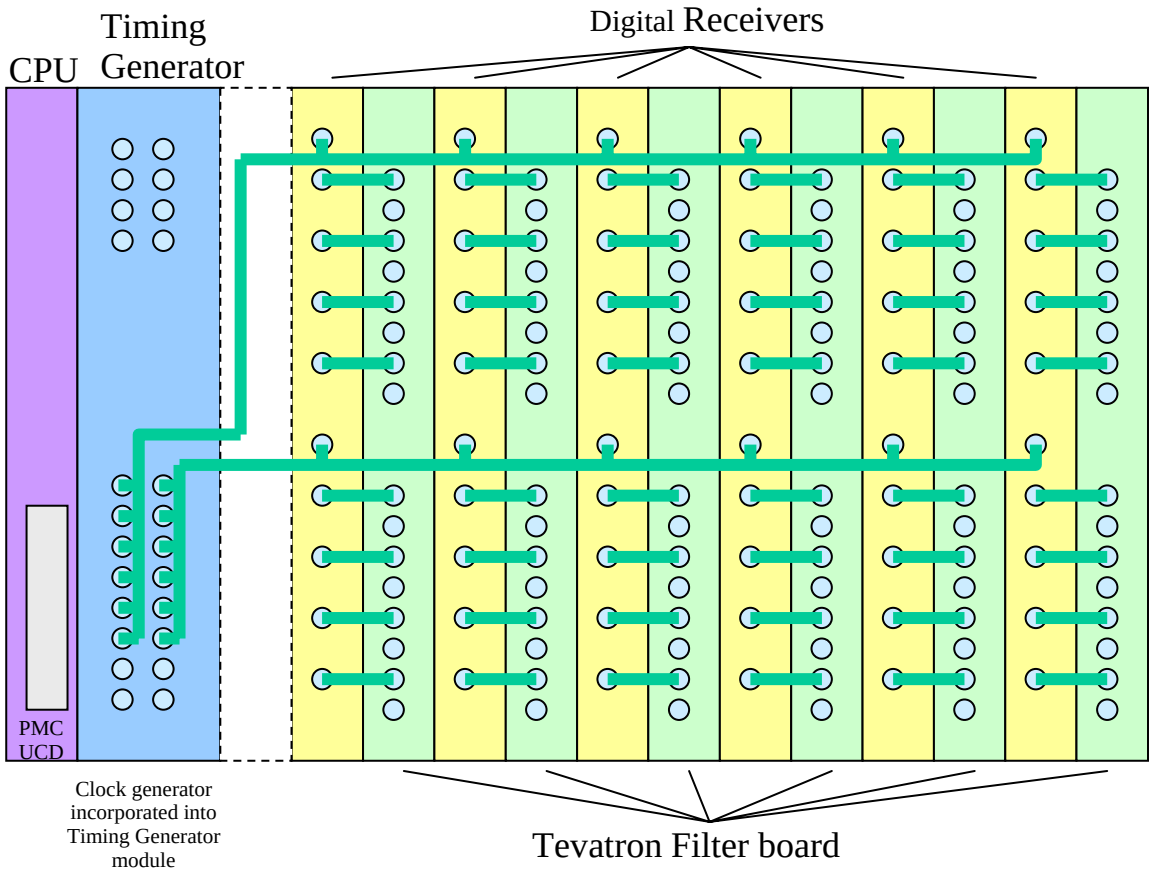


Figure 2 Sub Rack Module, Example Configuration

BPM Requirements

The requirements for this system are based on the system requirements documented in Tevatron BPM Upgrade Requirements Document (Beams Doc #554). A summary of the functional requirements are:

- Continuous closed orbit sampling with ~ 1 kHz of IF bandwidth and 500 Hz measurement rate.
- Closed orbit position should be stable for single bunch, multiple bunches and uncoalesed bunches.
- Turn-by-turn sampling with ~ 100 kHz of IF bandwidth and 47 kHz measurement rate. Store 8192 points/turn-by-turn request.
- Simultaneous measurement of protons and pbars. Measure pbars with closed orbit sampling and proton de-convolution (no change from closed orbit sampling) or use short gate sampling. Short gate sampling is a technique uses to separate proton signals from anti-proton signals on the same sensor lines. The technique is described in Beams Document #1200.

Data Acquisition

Functional Overview

The communication between the front-end processor and the Echotek modules happens through the VME backplane. If necessary, BLM data is exchanged through a digital I/O interface on the TGF board or as an I/O daughter board on the sub rack processor.

Data coming from the BPM are stored into a set of buffers in the sub rack controller. The depth and number of logical buffers that reside on the sub rack controller is defined in the Front-end Software Design Document (Beams Doc #1067). Some of the buffers, most notably the turn by turn data, is first stored in memory on the Echotek boards and then transferred to the sub rack controller on demand, as the processor/backplane does not have the bandwidth to acquire it in real time. The actual physical implementation of the sub rack controller buffers will be described in the front-end software design document.

Tevatron Filter board

The Tevatron Filter board conditions the signals from the Tevatron BPM sensors for input to the Echotek DSR Module. It also provides for injecting a diagnostic signal back into the sensor, into the Echotek Module, or both. Schematics for the Filter Card can be found in the Tevatron Filter board Appendix.

The Filter Card has eight channels so that one module is required for each Echotek Module. Each channel (Figure x) consists of an attenuator network, a band pass filter, and two relays. The BPM signals enter and exit via SMB connectors on the front panel.

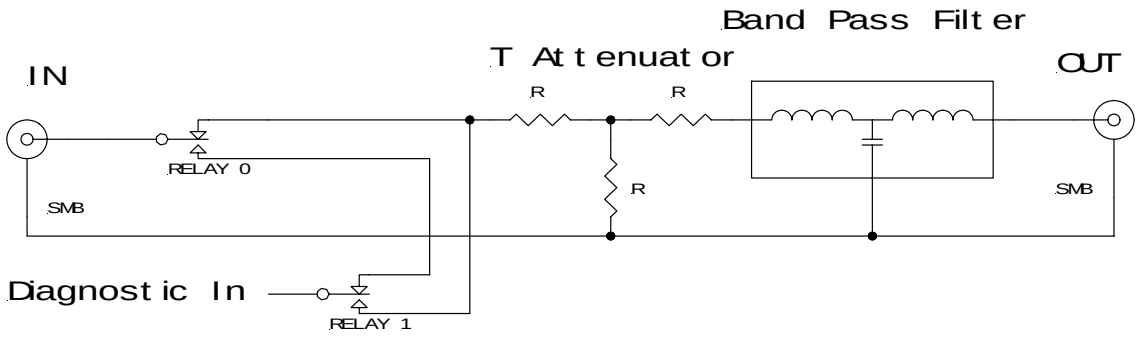


Figure 3 Filter Card BPM Channel Block Diagram

The Timing Generator Fanout Card (TGF) controls the relays and provides the diagnostic signal via bused TTL lines on the VME backplane. The Filter Card has a three position DIP switch to set the card address. This allows up to eight modules per sub rack. The TGF Card interface consists of the following lines:

- TFO_A (0-2) – Module Address lines from the TFG.
- TFO_CS* – Card Select line From the TFG, active low.
- TFO_CLK – Clock line from the TFG (2 MHz maximum).
- TFO_DOUT – Serial Data from the TFG.
- TFO_DIN – Serial Data to the TFG.
- TFO_RST* – Reset signal from the TFG, active low.
- TFO_DIAG – Diagnostic signal from the TFG.
- TFO_SP (0-3) – Spare outputs from the TFG.
- TFO_SPIN – Spare input signal to the TFG.

The TFG configures the relays by sending a 16 bit serial word to the Filter Card. It Drives the address lines and Chip Select (A (0-2), CS*) to select a module and then clocks out the 16 serial bits RC (0-15). The Most Significant Bit (MSB) (RC15) is shifted in first as shown in Table 1. The TFG then raises the CS* line to complete the operation. The state of the relays is changed on the rising edge of the CS* signal. The table matches the two relays, the input relay (R0) and the test signal relay (R1) for each channel, as shown in Figure 3 with the RCn bit that controls it. If the bit is a one the relay is activated and switches to the normally open connection. Otherwise it is in the normally closed position.

Table 1

Ch8		Ch7		Ch6		Ch5		Ch4		Ch3		Ch2		Ch1	
R1	R0	R1	RO	R1	R0	R1	R0	R1	R0	R1	R0	R1	R0	R1	R0
RC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RC0

The Filter Card receives the TTL diagnostic signal from the TFG, buffers it, sends it through a low pass filter and then distributes it on a bus to buffers on each of the eight channels.

The Filter Card has the following LEDs on the front panel:

- SEL – Indicates that the card is currently being address by the TFG (yellow).
- SW (0-2) – Indicates the setting of the address switches (green).
- 5V, 12V, -12V – Power supply indicators (green).

[Add front panel pictures and signal descriptions]

Echotek Data Converter Module

The Echotek module ECDR-GC814/8-FV2 is the baseline data converter. This module belongs to a general type of modules called Digital Signal Receivers (or Radios) (DSR). These modules have high speed digitizers that convert the analog, usually radio frequency, inputs into digital information very early in the signal processing. This reduces the amount of analog circuitry in the system.. The subsequent digital circuitry is used to down convert or base band the RF information, removing the high frequency carrier (53 MHz in this case) and revealing the information modulated onto that carrier, 48 KHz revolution information, 20 KHz betatron signals etc. The base banded signals are filtered in n stages of digital FIR filters and the output data is stored in a buffer memory on the module. The sub rack processors can readout the data memory over the sub rack VME backplane.

The data sheets for module are in the Appendix as Echotek DSR Module.

[Add front panel pictures and signal descriptions]

Timing Generator Fanout (TGF) Module

The Timing Generator Fanout (TGF) is a double width, 6U VME card that generates timing signals that control and initiate acquisition of the BPM signals. The timing signals are based on inputs from the accelerator controls clock system. These signal inputs include the Tevatron RF Clock (RFClk), Tevatron Beam Sync clock (TVBS) and the Tevatron event clock (TCLK).

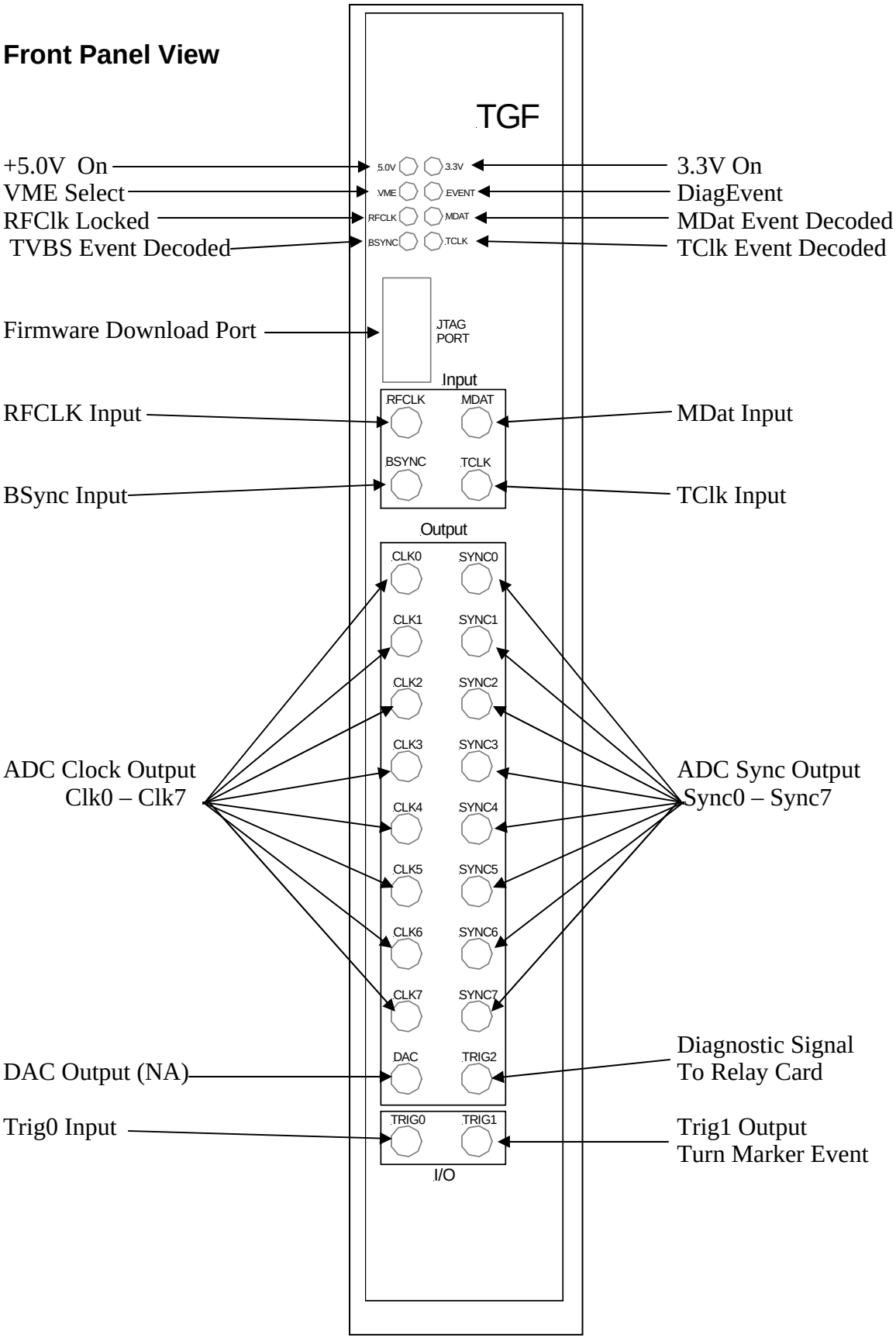
The RFClk is the synchronization time base for the major functionality of the TGF. The RFClk is used to over sample and decode the TVBS and TCLK signals.

The TVBS base frequency is one seventh of the RF Clock (7.5 MHz) Tevatron events are encoded are encoded as an eight bit serial byte onto this carrier and can be extracted from it. An important event is the revolution timing mark (0xAA). This event allows synchronization with the pattern of particles circling around the Tevatron ring. During colliding mode, particle bunches are spaced by 2.5 MHz in batches of 12, and for uncoalesed mode they are spaced by 53 MHz in batches of 30.

The TCLK signal is very similar to TVBS with a 10MHz carrier frequency and from it the module can extract a large number of events from the Main Control Room usually indicating changes in the state of the Tevatron. The TGF can be programmed to respond to any of up to sixteen selectable events at a time and interrupt the sub rack controller.
For each Echotek DSR module the TGF creates a digitization time base clock that paces the data conversions and filtering on the board. It also supplies a trigger signal for control of the data acquisition. For the Tevatron BPM system, the TGF multiplies the RF clock frequency by exactly 7/5 to produce the digitization clock. The RF frequency shifts as the energy of the beam changes. At approximately 980 GeV the RF clock frequency is typically 53.10468 MHz which produces a digitization rate of 74.346552 MHz. The normal range of the RF clock is 53.103xxx to 53.104xxx. [The TGF module can also generate other multiples of the RF Clock for the digitization clock, 10/7ths for example. Any multiple other than 7/5ths is created within the FPGA so the quality of the clock signal is less than that of the signal generated by the on-board clock oscillator.]

Digitization triggers will be triggered by and/or delayed from the revolution timing mark so that the acquired data are related to the particle bunches and measurements in separate service buildings are synchronized to each other as necessary.
The sub rack controller can be programmed to read out BPM values based on a specific TCLK signal (e.g. TCLK $77 which is a TeV Flash command). The sub rack controller does not receive Tevatron Beam Sync (TVBS) events. In the sub rack controller, the preparation for digitization and read out is signaled by an arm event. An arm event is usually originated by commands from the MCR. For example, a turn by turn measurement could be armed by a TCLK command or state change and then started on the next ‘AA’ turn marker plus a pre-programmed delay. More information is below in Data Acquisition .

Front Panel View



Also see installation document #1512.

Front Panel I/O Description

The Timing Generator Fanout Module inputs are:

- RFCLK – Tevatron RF Clock (very close to 53.10468 MHz). The RFClk must have signal level greater than 200mv and capable of driving an ac coupled 50-ohm termination.
- TVBS – Tevatron Beam Sync is an approximately ~7.5 MHz carrier with a modified Manchester encoding of Tevatron beam specific events. TVBS must be capable of driving 50-ohms with a signal level greater than +1.2v.
- TCLK – Tevatron Clock, a 10 MHz carrier modulated by a fixed protocol of bit patterns that can carry commands and data events to electronics across the accelerator complex. TClk must be capable of driving 50-ohms with a signal level greater than +1.2v.
- MDAT – A 10 MHz carrier modulated like TCLK to carry additional data and events. TClk must be capable of driving 50-ohms with a signal level greater than +1.2v. Not required for the BPM project.
- An External Trigger Input – One possible use of this input trigger is to permit the TVBS decoding to be bypassed by creating a hard trigger rather than a decoded trigger. Currently used for testing and future expansion.
- (Opt.) BLM External Device Bus – actually bidirectional but predominately a readout link for data from the Analog Box that processes the signals from the BLM sensors. Not required for the BPM project.

The Timing Generator Fanout Module outputs are:

- A2D Clock signals [0-7] – the digitization clock to the Echotek modules. These regenerated clock outputs are based on a signal that is phase locked to the RFClk with a frequency of RFClk multiplied by 7/5. Output levels are >700mv into 50-ohms.
- A2D Sync signals [0-7] - the synchronization output for a sequence of digitization. The Sync output signals have a pulse width of ~50ns and are capable of driving a 50-ohm termination.
- Diagnostic clock – A 53.104 MHz clock or pulse-train (selectable via VME register offset=0x100) to the Filter/Diagnostic board for the diagnostic functions. This signal is routed on the VME backplane.
- An External Trigger Output (Trig1)–Allows an external device to be triggered from an internal firmware trigger condition such as a decoded BSync event. Used for testing and future expansion.
- An External Trigger Output (Trig2)–Same as the diagnostic clock.
- DAC Output –14-bit DAC for testing and possible future expansion
- VME Interrupts for signaling the sub rack controller.

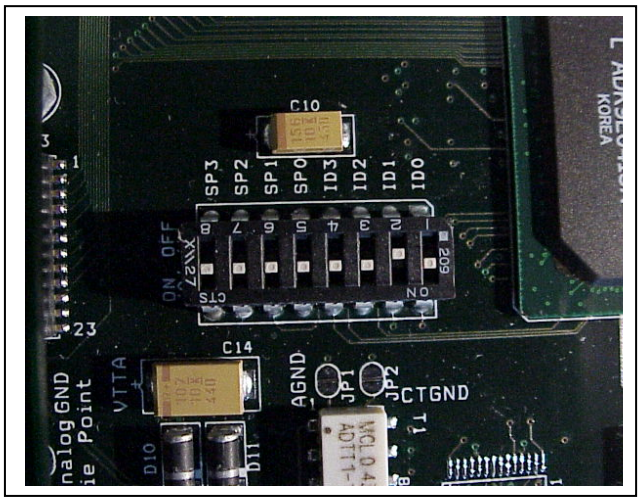
- Backplane connections that allow the TGF to control the Tevatron Filter boards. These lines will also allow a level of auto-detection on a per sub rack basis so that the TGF will 'know' how many Filter boards there are to control.

The A2D Sync signal variations are:

- TCLK trigger direct
- TCLK + programmable delay
- TCLK + repeated programmable delay
- TVBS trigger direct AA (turn marker) detect.
- TVBS + programmable delay
- TVBS + repeated programmable delay
- External Input Triggered – Similar to above TCLK or TVBS except it is a direct trigger and bypasses the Manchester decoding section.

VME Base Address Selection

The VME interface section of the TGF is capable of 16-bit address and data only. The VME base address is selectable via a four position dip switch labeled ID3 – ID0 as shown below. For the BPM project, only ID1 will be turned off and all the others will be on. This gives a base address of 0x2000 where ID3 – ID0 controls the upper 4-bits of the VME address.



TGF Firmware

The overall TGF firmware will not be changeable remotely. The board will need to be directly connected to the programmer workstation or laptop to change the firmware. However the functional programmability is controlled by the following registers that are accessible over the VME bus by the sub rack controller. All registers are 16 bits wide although the effective width is noted. Also note that anything labeled MDAT below has

not been implemented in the current version of the TeV BPM firmware and there are no plans to implement MDAT decoding in the future.

BPM Timing Generator Fanout - Register Map from Offset = 0h

Table 2	**REGISTER**	**MAP**	
I/O Address	**Register Name**	**Effective width**	
0x00	Acquisition Bucket Delay 0	11-bits	R/W
0x02	Acquisition Bucket Delay 1	11-bits	R/W
0x04	Acquisition Bucket Delay 2	11-bits	R/W
0x06	Acquisition Bucket Delay 3	11-bits	R/W
0x08	Acquisition Bucket Delay 4	11-bits	R/W
0x0A	Acquisition Bucket Delay 5	11-bits	R/W
0x0C	Acquisition Bucket Delay 6	11-bits	R/W
0x0E	Acquisition Bucket Delay 7	11-bits	R/W
0x10	Gate Count 0	11-bits	R/W
0x12	Gate Count 1	11-bits	R/W
0x14	Gate Count 2	11-bits	R/W
0x16	Gate Count 3	11-bits	R/W
0x18	Gate Count 4	11-bits	R/W
0x1A	Gate Count 5	11-bits	R/W
0x1C	Gate Count 6	11-bits	R/W
0x1E	Gate Count 7	11-bits	R/W
0x20	Not Used	11-bits	R/W
0x22	Not Used	11-bits	R/W
0x24	Not Used	11-bits	R/W
0x26	Turn Scaler for Background	11-bits	R/W
0x28	Mdat Type	8-bits	R/W
0x2A	Mdat Frame Value	16-bits	R/W
0x2C	Mdat scale factor		Read
0x2E	Pre-Trigger Delay All	6-bits	R/W
0x30	Control	See Table 4	R/W
0x32	Status	See Table 5	Read Only
0x34	BSync Turn Event	8-bits	R/W
0x36	BSync Start Event	8-bits	R/W
0x38	Diagnostics Counter	16-bits	Read Only
0x3A	Diagnostic Counter w/ wait		Wait on read
0x3C	MDAT Data sampled on Start		
0x3E	BSync Clear Timestamp Event	8-bits	R/W
0x40	First Turn Timestamp (Wrd0)	Quad Word	Read Only
0x42	First Turn Timestamp (Wrd1)	Quad Word	Read Only
0x44	First Turn Timestamp (Wrd2)	Quad Word	Read Only

0x46	First Turn Timestamp (Wrd3)	Quad Word	Read Only
0x48	TurnsCount (Low)	Low+High=32	Read Only
0x4A	TurnsCount (High)	Low+High=32	Read Only
0x4C	BSync Turn # Missing (Low)	Low+High=32	Read Only
0x4E	BSync Turn # Missing (High)	Low+High=32	Read Only
0x50	Switch		Read Only
0x52	TimeStamp Counter	Low word	Read Only
0x54	Turns Counter	Low word	Read Only
0x56	TClk TimeStamp Event	8-bits	R/W
0x58	TClk TimeStamp Wrd0	Quad Word	Read Only
0x5A	TClk TimeStamp Wrd1	Quad Word	Read Only
0x5C	TClk TimeStamp Wrd2	Quad Word	Read Only
0x5E	TClk TimeStamp Wrd3	Quad Word	Read Only
0x60	Irq Vector Reg 1	See Figure 4	R/W
0x62	Irq Vector Reg 2	See Figure 4	R/W
0x64	Last Interrupted TClk Event	8-bits	Read Only
0x66	TClk IRQ #Wrds Pending	8-bits	
0x68			
0x6A			
0x6B			
0x6C			
0x70	IRQ1 Source Mux	See Table 3	R/W
0x72	IRQ2 Source Mux	See Table 3	R/W
0x74			
0x76			
0x78			
0x7A			
0x7C			
0x7E	Memory Address Register		R/W
0x80	TClk Event0	8-bits	R/W
0x82	TClk Event1	8-bits	R/W
0x84	TClk Event2	8-bits	R/W
0x86	TClk Event3	8-bits	R/W
0x88	TClk Event4	8-bits	R/W
0x8A	TClk Event5	8-bits	R/W
0x8C	TClk Event6	8-bits	R/W
0x8E	TClk Event7	8-bits	R/W
0x90	TClk Event8	8-bits	R/W
0x92	TClk Event9	8-bits	R/W
0x94	TClk Event10	8-bits	R/W
0x96	TClk Event11	8-bits	R/W
0x98	TClk Event12	8-bits	R/W
0x9A	TClk Event13	8-bits	R/W

0x9C	TClk Event14	8-bits	R/W
0x9E	TClk Event15	8-bits	R/W
0xA0	BSyncEvent(00_0F) Found		R/W
0xA2	BSyncEvent (10_1F) Found		R/W
0xA4	BSyncEvent (20_2F) Found		R/W
0xA6	BSyncEvent (30_3F) Found		R/W
0xA8	BSyncEvent (40_4F) Found		R/W
0xAA	BSyncEvent (50_5F) Found		R/W
0xAC	BSyncEvent (60_6F) Found		R/W
0xAE	BSyncEvent (70_7F) Found		R/W
0xB0	BSyncEvent (80_8F) Found		R/W
0xB2	BSyncEvent (90_9F) Found		R/W
0xB4	BSyncEvent (A0_AF) Found		R/W
0xB6	BSyncEvent (B0_BF) Found		R/W
0xB8	BSyncEvent (C0_CF) Found		R/W
0xBA	BSyncEvent (D0_DF) Found		R/W
0xBC	BSyncEvent (E0_EF) Found		R/W
0xBE	BSyncEvent (F0_FF) Found		R/W
0xC0	TClkEvent(00_0F) Found		R/W
0xC2	TClkEvent (10_1F) Found		R/W
0xC4	TClkEvent (20_2F) Found		R/W
0xC6	TClkEvent (30_3F) Found		R/W
0xC8	TClkEvent (40_4F) Found		R/W
0xCA	TClkEvent (50_5F) Found		R/W
0xCC	TClkEvent (60_6F) Found		R/W
0xCE	TClkEvent (70_7F) Found		R/W
0xD0	TClkEvent (80_8F) Found		R/W
0xD2	TClkEvent (90_9F) Found		R/W
0xD4	TClkEvent (A0_AF) Found		R/W
0xD6	TClkEvent (B0_BF) Found		R/W
0xD8	TClkEvent (C0_CF) Found		R/W
0xDA	TClkEvent (D0_DF) Found		R/W
0xDC	TClkEvent (E0_EF) Found		R/W
0xDE	TClkEvent (F0_FF) Found		R/W
0X100	FilterCard Control Register	See Table 7	R/W
0X102	Relay Data, Card 0	See Table 8	R/W
0X104	Relay Data, Card 1	See Table 8	R/W
0X106	Relay Data, Card 2	See Table 8	R/W
0X108	Relay Data, Card 3	See Table 8	R/W

0X10A	Relay Data, Card 4	See Table 8	R/W
0X10C	Relay Data, Card 5	See Table 8	R/W
0X10E	Relay Data, Card 6	See Table 8	R/W
0X110	Relay Data, Card 7	See Table 8	R/W
	ID ROM	8-bit	R only
0X400	x0054, "T"	8-bit	R only
0X402	x0047, "G"	8-bit	R only
0X404	x0046, "F"	8-bit	R only
0X406	x0000, " "	8-bit	R only
0X408	x0056, "V"	8-bit	R only
0X40A	x0045, "E"	8-bit	R only
0X40C	x0052, "R"	8-bit	R only
0X40E	x0053, "S"	8-bit	R only
0X410	x0049, "I"	8-bit	R only
0X412	x004F, "O"	8-bit	R only
0X414	x004E, "N"	8-bit	R only
0X416	x0000, " "	8-bit	R only
0X418	x0032, "2"	8-bit	R only
0X41A	x002E, "."	8-bit	R only
0X41C	x0030, "0"	8-bit	R only
0X41E	x002E, "."	8-bit	R only
0X420	x0032, "5"	8-bit	R only
0X422	x0020, " "	8-bit	R only

Table 3	**IRQ SOURCE MUX**	**I/O Address 0x70...0x72**	
DATA	SOURCE		
0x00	Null		
0x01	Start Event		
0x02	Revolution Event		
0x03	MDAT Type Match		
0x04	Turn Counter Trigger Out		
0x05	Delay Timer Enabled		
0x06	Delay Timer Trigger		
0x07	Delay Timer Terminal Count		
0x08	Turn Counter Trigger		
0x09	Periodic timer (BGFlash rate)		
0x0A	TClk Event Match	16-bits	R/W

INTERRUPT STATUS/ID REGISTER DETAIL (Eight instances)

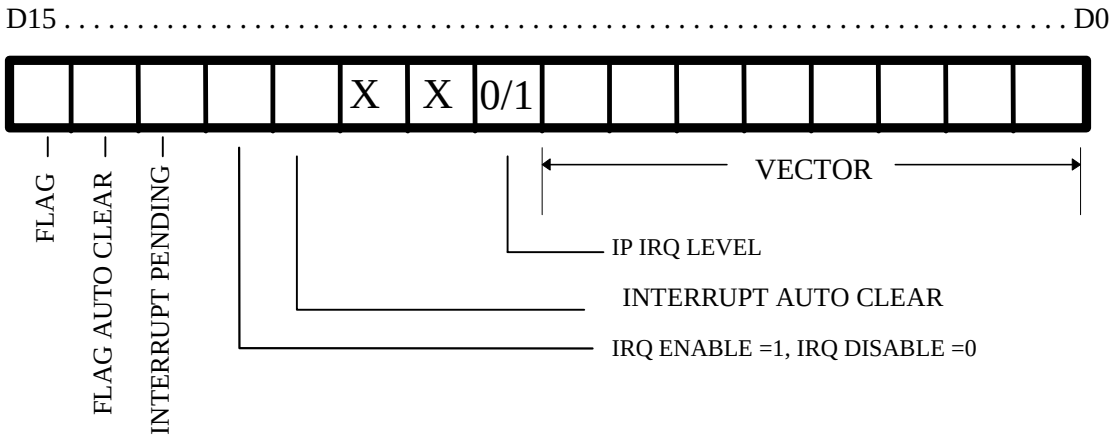


Figure 4

Table 4	**CONTROL AND MODE REGISTER**		**I/O Address 0x30**
DATA			
Low Byte			
0xXX01	Control[0]	Enable Pre-Trigger Counter	Zero = Disabled, One = Enabled
0xXX02	Control[1]	Enable Delay Timer	Zero = Disabled, One = Enabled
0xXX04	Control[2]	Not Used	
0xXX08	Control[3]	Not Used	
0xXX10	Control[4]	Trigger Source	Zero = PreTrigger, One = External, Two = Start Event
0xXX20	Control[5]	Trigger Source	
0xXX40	Control[6]	"Start" Source	Zero = Start Event, One = Null, Two = Turn Scaler (periodic)
0xXX80	Control[7]	"Start" Source	
High Byte			
0x01XX	Control[8]	Not Used	
0x02XX	Control[9]	Enable TClk	Zero = Disabled, One = Enabled**
0x04XX	Control[10]	Enable Beam Sync	Zero = Disabled, One = Enabled
0x08XX	Control[11]	Not Used	
0x10XX	Control [12]	Single/Repetitive ADC Sync Out	Zero = Repetitive, One = Single
0x20XX	Control[13]	Not Used	
0x40XX	Control[14]	Reset TClk IRQ Pending	Zero = Disabled, One = Enabled
0x80XX	Control[15]	Reset TSG	Zero = No action, One = Reset

** Proposed Change

Control Register Comments:

Control(7:6)
When equal to "00", the Start Source is the BSync start event register (0x36) is equal the decoded BSync serial input.
When equal to "01", No Start Source.
When equal to"10", Start is generated when the turn scaler counter (0x26) is equal to zero. The Turn scaler counter is decremented by the decoded BSync Turn event.

Control(12)
When equal to a zero, an ADC_Sync Out pulse is generated for each event trigger (BSync event or external trigger) repetitively. When equal to a one, an ADC_Sync Out pulse is generated for the first event trigger after writing to the control register. Default is zero for repetitive mode.

Table 5	**STATUS REGISTER BIT DEFINITIONS**	**I/O Address 0x32**
DATA	DESCRIPTION	
Bit-0	Turn Marker	
Bit-1	Start Marker	
Bit-2		
Bit-3		
Bit-4	BSync Parity Error	
Bit-5		
Bit-6		
Bit-7		
Bit-8	Turn Counter Enabled	
Bit-9	53MHz present	
Bit-10	BSync Present	
Bit_11	TClk Present	

Table 7	**FilterCard Control Register BIT DEFINITIONS**	**I/O Address 0x100**
DATA	DESCRIPTION	
Bit-0	FilterCard Start/Done Card 0	Note 1
Bit-1	FilterCard Start/Done Card 1	Note 1
Bit-2	FilterCard Start/Done Card 2	Note 1
Bit-3	FilterCard Start/Done Card 3	Note 1
Bit-4	FilterCard Start/Done Card 4	Note 1
Bit-5	FilterCard Start/Done Card 5	Note 1
Bit-6	FilterCard Start/Done Card 6	Note 1
Bit-7	FilterCard Start/Done Card 7	Note 1
Bit-8	FilterCard R/W	Note 2
Bit-9	FilterCard Enable Diagnostic Signal	
Bit-10	Diagnostic Signal Type	Note 3
Bit-11	RelayState0	
Bit-12	RelayState1	
Bit-13	RelayState2	
Bit-14		
Bit-15	FilterCard Global Reset	

Note 1: After loading relay information into the Filter Card Data Registers (0x102 – 0x110) (xx) and setting a one in the corresponding FilterCard Start/Done l register bit will immediately start sending the serialized data to the appropriate Filter/Relay Card. When the transfer of data is complete the start bit will be cleared automatically by the FPGA Firmware.

Note 2: The FilterCard R/W bit (Bit-8) is currently write capable only and read capability will be implemented in the future. Default is zero for writes to Filter Card.

Note 3: The Diagnostic Signal Type can be set to a continuous 53MHz clock when set to a logic zero or a 53 MHz clock pulse train of seven pulses triggered from the BSync turn event when set to a logic one. Default is a continuous 53MHz clock.

Table 8	**FilterCard Data Register** Table 8		
Ch #	**MSB Data LSB**	**Source**	**Destination**
1	xx xx xx xx xx xx xx 00	BPM	Digitizer
1	xx xx xx xx xx xx xx 01	Diagnostic	BPM
1	xx xx xx xx xx xx xx 10	Diagnostic	BPM & Digitizer
1	xx xx xx xx xx xx xx 11	Diagnostic	Digitizer
2	xx xx xx xx xx xx 00 xx	BPM	Digitizer
2	xx xx xx xx xx xx 01 xx	Diagnostic	BPM
2	xx xx xx xx xx xx 10 xx	Diagnostic	BPM & Digitizer
2	xx xx xx xx xx xx 11 xx	Diagnostic	Digitizer
3	xx xx xx xx xx 00 xx xx	BPM	Digitizer
3	xx xx xx xx xx 01 xx xx	Diagnostic	BPM
3	xx xx xx xx xx 10 xx xx	Diagnostic	BPM & Digitizer
3	xx xx xx xx xx 11 xx xx	Diagnostic	Digitizer
4	xx xx xx xx 00 xx xx xx	BPM	Digitizer
4	xx xx xx xx 01 xx xx xx	Diagnostic	BPM
4	xx xx xx xx 10 xx xx xx	Diagnostic	BPM & Digitizer
4	xx xx xx xx 11 xx xx xx	Diagnostic	Digitizer
5	xx xx xx 00 xx xx xx xx	BPM	Digitizer
5	xx xx xx 01 xx xx xx xx	Diagnostic	BPM
5	xx xx xx 10 xx xx xx xx	Diagnostic	BPM & Digitizer
5	xx xx xx 11 xx xx xx xx	Diagnostic	Digitizer
6	xx xx 00 xx xx xx xx xx	BPM	Digitizer
6	xx xx 01 xx xx xx xx xx	Diagnostic	BPM
6	xx xx 10 xx xx xx xx xx	Diagnostic	BPM & Digitizer
6	xx xx 11 xx xx xx xx xx	Diagnostic	Digitizer
7	xx 00 xx xx xx xx xx xx	BPM	Digitizer
7	xx 01 xx xx xx xx xx xx	Diagnostic	BPM
7	xx 10 xx xx xx xx xx xx	Diagnostic	BPM & Digitizer
7	xx 11 xx xx xx xx xx xx	Diagnostic	Digitizer
8	00 xx xx xx xx xx xx xx	BPM	Digitizer
8	01 xx xx xx xx xx xx xx	Diagnostic	BPM
8	10 xx xx xx xx xx xx xx	Diagnostic	BPM & Digitizer
8	11 xx xx xx xx xx xx xx	Diagnostic	Digitizer

Sub Rack Processor Module

The sub rack controller CPU board is responsible for establishing the communication link between user applications and the Echotek modules. All control and data transferred to/from the BPM modules pass through the sub rack controller.
The processor chosen for this system is a Motorola MVME2400-0361 with 512MB of on-board memory. The processor will run the VxWorks embedded operating system which is widely used throughout the lab. The ESS department in the Computing Division has a MVME 2400 data sheet on its web site.

Sub Rack Cables

Interconnection cables are an important facet of this upgrade. The signal cables moving sensor outputs around the electronics must not distort, attenuate or add noise to the signals of interest. Also the signals from the two outputs of each side of a sensor must travel through cables that have the signal delay matched to better than 50 picoseconds. This is approximately one degree of phase shift at 53 MHz. The timing cables also have a similar delay matching specification so that clock and gate delays within a sub rack are uniform. The chosen default cable is double-shielded RG-400. The short jumpers between the Filter board and the Echotek DSR are RG-316 because of their flexibility requirement. The Cable Specifications are Beams Document #1257.
The connectors chosen for the cables are a mixture of SMA and SMB style connectors which have excellent signal characteristics at 53 MHz. Connections to existing systems use the SMA style. Where the connectors are too close together, the SMB style connectors are used because they snap on and off rather than requiring a nut be tightened.

Sub Rack Channel Organization

The organization of the channels is an issue that affects several aspects of the Data Acquisition and the hardware constrains the organization in some ways. For instance there is a single trigger input to each Echotek module which might limit the range of operations that are available to those eight channels at any time. The main organization choices and channel granularities are listed below.

Channel Granularity = 8 channels -- Proton on a single module, anti proton on another
Channel Granularity = 4 channels -- A group of four contiguous channels process proton signals, the remaining four channels on a module are anti-proton signals.
Channel Granularity = 2 or 1. -- Many ways to interleave the species of particles.

Data Acquisition Operations

BPM Measurement types

Rewrite this for the hardware perspective of bandwidth and data rate. There are two different types of measurements that can be made from the data in the digitizing cards. The data types are:

- Closed Orbit Measurements, also called Frame data. Frame data is an average of *n* measurements. The average is *usually* based on 8, 16, 32 or 64 single turn measurements, and is configurable. Frame data is the only data measurement made in normal operation mode. **Note:** the number used in the averages for normal operation mode is not necessarily the same number as in injection mode.
- Turn Data is the instantaneous single value (i.e., not averaged over n readings) of the sensors once the trigger is received. The BPM DA must operate in a Turn by Turn mode (TBT) where a large number (8192) of sequential turns are sampled without missing a turn. Then the DA can stop sampling, read-out the data from the Echotek modules and do whatever processing and telemetry is necessary. Normal TBT mode is continuous cycling between TBT sampling and readout activities.
- A third mode is a variation on Turn by turn mode where a single measurement is acquired by

It is important to note that for turn measurements, all BPMs are triggered relative to the same bunch. However, for a closed orbit measurement, the specific bunches used in the averaging can be different across BPMs.

The data acquisition system must support systematic triggering of *N* events for both of these data types. For turn buffers, the arrays are of N consecutive measurements (i.e., Turn by Turn). On the other hand, closed orbit buffers are built by a *number of* triggers of a specific type.

The measurement types require different setups in the Echotek DDC modules, and, therefore have a time penalty associated with changing setup. In general the data acquisition modes must switch to acquire a different type of measurement.

BPM Data Acquisition Modes

There are different modes of BPM data acquisition. These modes are currently mutually exclusive due to the necessity to configure the filters and timing in the Echotek modules for a specific mode. However, the Echotek module appears to have the capability to run two filter processes in parallel. This capability will be explored because it would be advantageous to be able to run two modes simultaneously. The modes are:

- Closed Orbit operation.
- Injection
- Turn by Turn
- Diagnostic
- Calibration
- Raw Data
- Fail-Safe (not specified yet)
- Turn-by-turn (same for 1st turn) 100 kHz bandwidth
- Closed Orbit Short Gate Sample Closed Orbit
- Narrowband (current A1 configuration) 1kHz bandwidth

[added by Jim, lets settle on what modes there are and what we call these.

Old email: After talking with Jim Steimel, it looks like the modes should be as follows:

Raw ADC Counts, Turn by Turn, Closed Orbit (narrow band), Closed Orbit (short gate)

This would also remove the necessity for the separate narrow band/short gate switch. Also, there will ultimately be a "Safe Mode", but that is as yet undefined.

Brian]

The modes are described in more detail in the following sections. The buffers are described in the Software specifications document.

Closed Orbit operation

This is the default mode of the data acquisition system. The TGF is set up to delay from the turn marker a fixed amount and to sample the signals for a number of turns. This is the burst count. The 53 MHz signal from the BPM sensors is sampled by the 74 MHz digitization clock. These digital samples are down converted using a 21 MHz clock in order to select the modulation signals riding on the 53 MHz sensor signal. The resulting signal is band limited at 48 KHz to approximately 100 Hz bandwidth which averages together many turns of the accelerator particles. The resulting samples come out of the Echotek module at a xx Hz rate. The samples are stored in the output memory of the Echotek module until the burst count is reached. The sub rack controller is then interrupted and the data is readout to be handled by the sub rack controller software.
This mode is armed by a selected BSync start event, the TGF waits for a pre-trigger turn marker delay and then the TGF generates a sync output plus bucket delay for each of a

programmable number of turn counts. There are delay and count registers for each of the eight TGF sync outputs allowing individual control of each Echotek module. See Table 2, addresses 0x00 thru 0x1E above.

Turn by turn

Turn by turn mode is used to take a sample every turn of the particle bunches in the accelerator, approximately every 21 microseconds. The 53 MHz signal from the BPM sensors is sampled by the 74 MHz digitization clock. These digital samples are down converted using a 21 MHz clock in the Echotek DDC chip in order to select the modulation signals riding on the 53 MHz sensor signal. The resulting signal is additionally band limited to produce a sample per turn. 8K consecutive turns are taken and stored in the Echotek output buffer when a turn by turn request is made. At the end of the sampling the sub rack controller is interrupted and the data is readout to be processed by the sub rack controller software.
This mode is a special case of closed orbit mode. When it is armed by the turn marker BSync start event, the TGF waits for a pre-trigger turn marker delay (usually zero) and then the TGF generates a sync output plus bucket delay and stops because the count must be set to one. As above see Table 2 for delay and count registers for each of the eight TGF sync outputs.

Injection

Injection is a special type of turn by turn mode used to sample the first pass of a particle bunch. It is most often used when proton bunches are first introduced into the Tevatron. Only one sample is taken per data acquisition cycle and the timing of the data is set up carefully before the particles arrive at the BPM sensor. Injection mode needs to be disabled and re-enabled on request because there are times when closed orbit data is preferred during proton injection.
The arming and triggering of the mode has not yet been specified.

Diagnostic Mode

Normal or turn by turn modes can be used. The diagnostic signal is enabled and the relays in the Tevatron Filter board are activated to either inject the diagnostic signal out the input connector toward the sensor or out the output connector toward the Echotek module. Multiple channels can be driven at the same time but the data collected will be hard to interpret if more than one of the four connections to a specific BPM sensor has the diagnostic signal imposed on it. The best configuration is for one of the four connections to be driven and the four associated Echotek channels are recorded. If the signal is directed toward the sensor, the specific Echotek channel that was disconnected from the sensor should have no input and show local background noise while the other three channels of that sensor will have diagnostic signal that is coupled through the sensor itself. This will test the wiring to the sensors and the sensor itself. If all four connections to the sensor are diagnosed this way a complete picture of the health of the sensor and its wiring will be collected. If the diagnostic signal is directed toward the

Echotek input that channel can be tested and a general calibration collected. All of the Echotek connection to the Filter/Diagnostic board can be tested this way.

Appendix

Installation

Installation in the service buildings will be done on a least interference basis at first until the new system proves it has a reasonable accuracy and reliability. The order of installation has been defined as: A3, B3, C3, D3, E3, F2, B0, D0, A2, B2, C2, D2, E2, A4, B4, C4, D4, E4, A1, B1, C1, D1, E1, A0, F3, F4 and F1.

Quantities of sensors:

Table 6

Service Building	BPMs	BPM Modules	BLMs
A0	4	2	12
A1	10	5	9
A2	9	5	9
A3	8	4	8
A4	9	5	8
B0	6	3	22
B1	10	5	9
B2	9	5	9
B3	8	4	8
B4	9	5	12
C1	10	5	12
C2	9	5	9
C3	8	4	8
C4	9	5	8
D0	6	3	23
D1	10	5	9
D2	9	5	9
D3	8	4	8
D4	9	5	8
E1	10	5	9
E2	9	5	9
E3	8	4	8
E4	11	6	11
F1	12	6	12
F2	9	5	9
F3	8	4	8
F4	9	5	8

Schematics, Layouts and drawings.

Timing Generator Fanout Module

Schematic: Beams Document #1260
Layout: Beams Document #1261
Bill of Materials: Beams Document #1265

Tevatron Filter board

Schematic: Beams Document #1244
Layout: Beams Document #1259
Bill of Materials: Beams Document #1264

Analog Filter Specifications

Beams Document #1065

Cable Specifications

Beams Document #1257

Sub rack Specifications

Beams Document #1245

Beam Loss Monitor Notes

The BLM analog circuitry and digitizers are in separate analog crates and the data is readout into the VME sub rack through a bus interface designed into the Timing Generator Fanout Module or through a COTS digital I/O PMC board. The BLM appears [3]as a read-write memory block over the External Device Bus (EDB). The VME sub rack processor writes to specific memory locations to set up and control the BLM hardware and reads from specific locations to acquire BLM data and status.

BLM Operations

The BLMs are functionally simple devices with relatively long time constants from the BPM perspective. They are self paced and require very little control. BLM values are read out periodically on triggers as programmed in the DA application. The data are always available although they may not have updated since the previous read. There is no need for mode switching for BLMs and there are no turn by turn requirements. The BLM sub rack is read out through an External Device Bus (EDB), a parallel, bidirectional connection. The control, configuration and readout of the BLM devices is done through memory mapped registers within the EDB address space.
The External Device Bus is described in Beams document #772, Beam Loss Monitor System Description. The register structure is described in Beams document #764, BLM Data Structures and General Information.

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[3] BLM Data Structures and General Information (Beams-Doc-764)

The upgrade project will provide the functional connection through the crate control through the EDB to the BLM Analog sub rack such that the BLM system appears identical to the existing system.

Echotek DSR Module

Data Sheet attached.

ECHOTEK CORP.

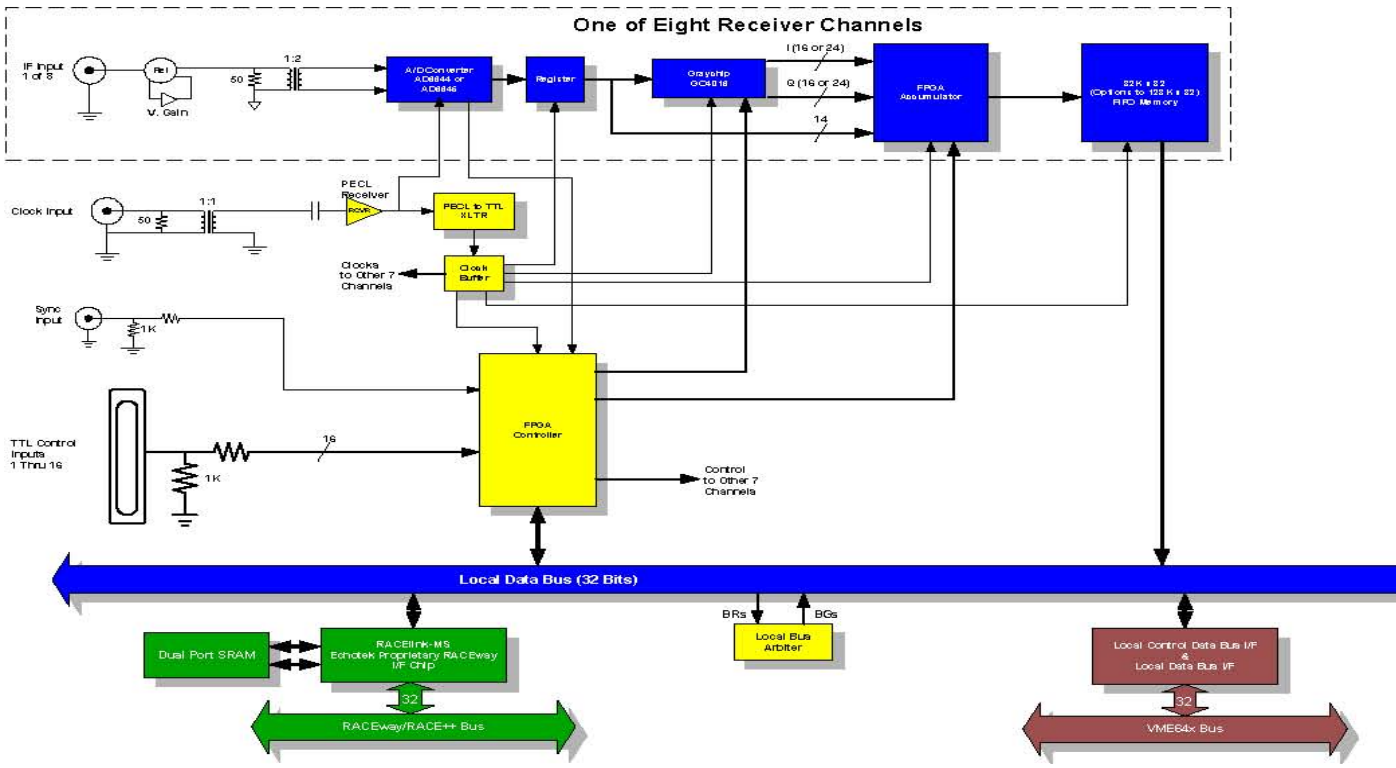
EIGHT CHANNEL
ANALOG TO DIGITAL CONVE
WITH DIGITAL RECEIVER

ECDR-GC814

FEATURES

* 8 IF INPUTS
* SIMULTANEOUS SAMPLING
* EIGHT ANALOG TO DIGITAL CONVERTERS (ANALOG DEVICES AD 14 BIT, 65 MSPS, OR AD6645 FOR SAMPLING RATES TO 105 MHz)
* SFDR > 90 dB FS
* 8 RECEIVER CHANNELS (GRAYCHIP GC4016)
* DECIMATION RANGE 8-16K/CHANNEL
* HEADER INSERTION
* VME 64X, SINGLE SLOT
* RACE++™ OUTPUT
* ALSO AVAILABLE AS TWO OR FOUR CHANNEL MODEL
* AVAILABLE AS A/D CONVERTER ONLY AS AN 8, 4, OR 2 CHANNEL
* VARIABLE GAIN (~ -10 TO +20 dB)

ECDR-GC814 BLOCK DIAGRAM



ECHOTEK CORPORATION 555 SPARKMAN DRIVE #400 HUNTSVILLE, AL 35816 PHONE 256 721 1911 FAX 256 721 9266 E-MAIL: sales@echotek.com

ECDR-GC814

This analog to digital converter and digital drop receiver board provides eight channels of 14 bit, 105 MHz analog to digital conversion and digital processing suitable for wideband and narrowband down conversion and filtering in a single 6U VME slot. Data decimation range of each receiver channel is user programmable from 8 to 16384. The receiver section of each channel may be bypassed to output raw A/D data.

Data Inputs

Up to eight analog signals may be input to this board via front panel SMA connectors. Each signal is converted using Analog Devices AD6644, 14 bit, 65 MHz A/D converters or AD6645 for sampling rates to 105 MHz. Direct digitization for IF's > 200 MHz are supported. These high quality analog to digital converters exhibit Spur Free Dynamic Ranges in excess of 90 dBFS.

Clocks

The A/D clock is provided by the user via front panel SMA connector. This clock signal (sine wave into 50 ohms) is buffered and distributed to all eight channels so that all channels are sampled simultaneously.

Other Inputs

The user may also input a sync signal through the front panel and up to 16 bit wide digital word - normally used to insert a header into the data stream or for tagging data.

Receiver Channels

The digitizer outputs from each A/D converter interfaces to the input crossbar switch on the Graychip GC4016 multi-standard quad digital down converter chip. A receiver channel block diagram is shown below for clarity - the Graychip GC4016 contains four such channels that can be combined as mentioned below, only one Graychip 4016 channel or channel combination is output per receiver channel on the ECDR-GC814.
The ECDR-GC814 supports the various channel combination configurations allowed by the Graychip 4016, that is: Sample Accumulator:

A	No channels combined. In this mode, each channel supports decimations from 32 to 16384.
B	Channel pair combinations supports decimations of 16 to 8192 while in this mode
C	Four channel combination resulting in one wideband output channel:
	- supports decimations of 8 to 4096 while in this mode.

The output of the receivers or the A/D converter (in receiver bypass mode) is directed to an FPGA that outputs the sum of a programmed number of samples. The output may be the sum of 1, 2, 4, 8, 16, 32, 64, 128, or 256 raw A/D samples or I's or Q's.

FIFO Buffer

Data is output from the sample accumulator to each channel's FIFO buffer. The FIFO buffer is 16K x 32 bits (by default) and may be configured at the factory as large as 128K x 32 bits.

Data Output

Data, raw A/D output, complex receiver data, or either of the quadrature components, is output via the RACE++ interface. The data may also be output via the VME64X interface - but this interface was designed to be used for control in real time and, therefore, is not optimized for high speed data transfer.

Operating Modes

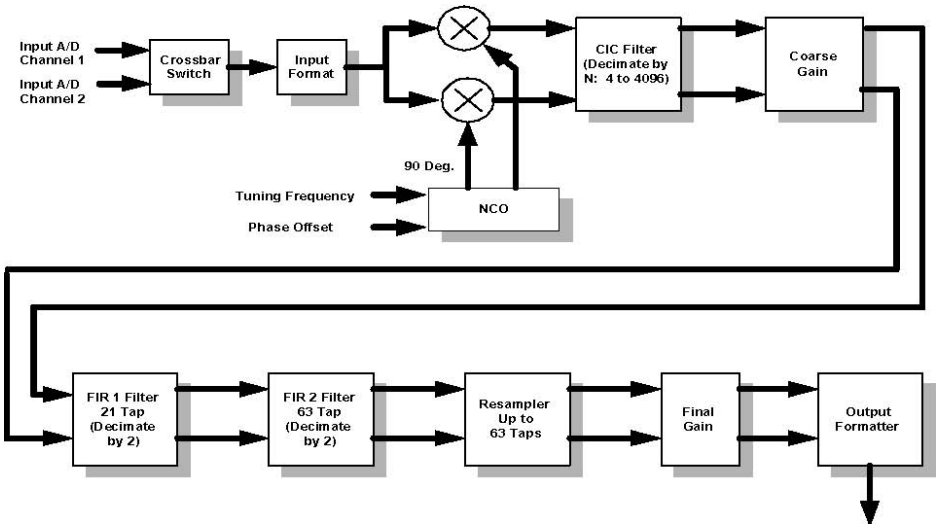
The ECDR-814 supports both CW and pulsed system applications. The board may be controlled in one of two basic operating modes:
Gate Mode - Data acquisition occurs when the gate signal is active. The gate signal may be provided via external front panel input or a software write.
Counted Burst - A preprogrammed number of samples are acquired and processed with each occurrence of an external trigger pulse. This trigger pulse also has a software bit counterpart associated with it.

Set-Up and Control

All set-up and control registers are accessible via the VME interface. Additionally, the RACE++ interface may be programmed by either VME or RACE++ and can be a RACE++ master or slave.

Driver Support

Drivers are supplied for VxWorks Operating Systems.



Ordering Information

Model	Part Number	Ruggedization	Options
ECDR-GC814/8	12-0050/CC334A	Commercial	65 MHz A/D, 16K FIFO
ECDR-GC814/8	12-0050/CC335	Commercial	65 MHz A/D, 128K FIFO
ECDR-GC814/8-80	12-0050/CC450	Commercial	80 MHz A/D, 16K FIFO
ECDR-GC814/8-80	12-0050/CC512	Commercial	80 MHz A/D, 128K FIFO
ECDR-GC814/8-105	12-0050/CC495	Commercial	105 MHz A/D, 16K FIFO
ECDR-GC814/8-105	12-0050/CC496	Commercial	105 MHz A/D, 128K FIFO
ECDR-GC814/4	12-0057/CC339	Commercial	65 MHz A/D, 16K FIFO
ECDR-GC814/4	12-0057/CC337	Commercial	65 MHz A/D, 128K FIFO
ECDR-GC814/4-80	12-0057/CC494	Commercial	80 MHz A/D, 16K FIFO
ECDR-GC814/4-80	12-0057/CC451	Commercial	80 MHz A/D, 128K FIFO
ECDR-GC814/4-105	12-0057/CC477	Commercial	105 MHz A/D, 16K FIFO
ECDR-GC814/4-105	12-0057/CC497	Commercial	105 MHz A/D, 128K FIFO
ECDR-GC814/2	12-0058/CC350	Commercial	65 MHz A/D, 16K FIFO
ECDR-GC814/2	12-0058/CC498	Commercial	65 MHz A/D, 128K FIFO
ECDR-GC814/2-80	12-0058/CC420	Commercial	80 MHz A/D, 16K FIFO
ECDR-GC814/2-80	12-0058/CC340	Commercial	80 MHz A/D, 128K FIFO
ECDR-GC814/2-105	12-0058/CC499	Commercial	105 MHz A/D, 16K FIFO
ECDR-GC814/2-105	12-0058/CC500	Commercial	105 MHz A/D, 128K FIFO
'LED OPTION:			
ECDR-GC814/8-DC	12-0107/CC426	Commercial	65 MHz A/D, 16K FIFO
ECDR-GC814/8-DC	12-0107/CC431	Commercial	65 MHz A/D, 128K FIFO

Model Part Number Ruggedization Options

ECDR-GC814/4-DC 12-0108/CC427 Commercial 65 MHz A/D, 16K FIFO
ECDR-GC814/4-DC 12-0108/CC432 Commercial 65 MHz A/D, 128K FIFO

ation Levels	Temp (°C)	emp (°C)	Vibration	ck	dity	Notes
	with 300ft./ rflow		from 10 to 2000Hz random soidal from 5 to 500 Hz	aw tooth, uration	RH	Grade, cooled by blown air, for use in be s and software development applications

814/2-DC	12-0109/CC428	Commercial	65 MHz A/D, 16K FIFO
814/2-DC	12-0109/CC433	Commercial	65 MHz A/D, 128K FIFO