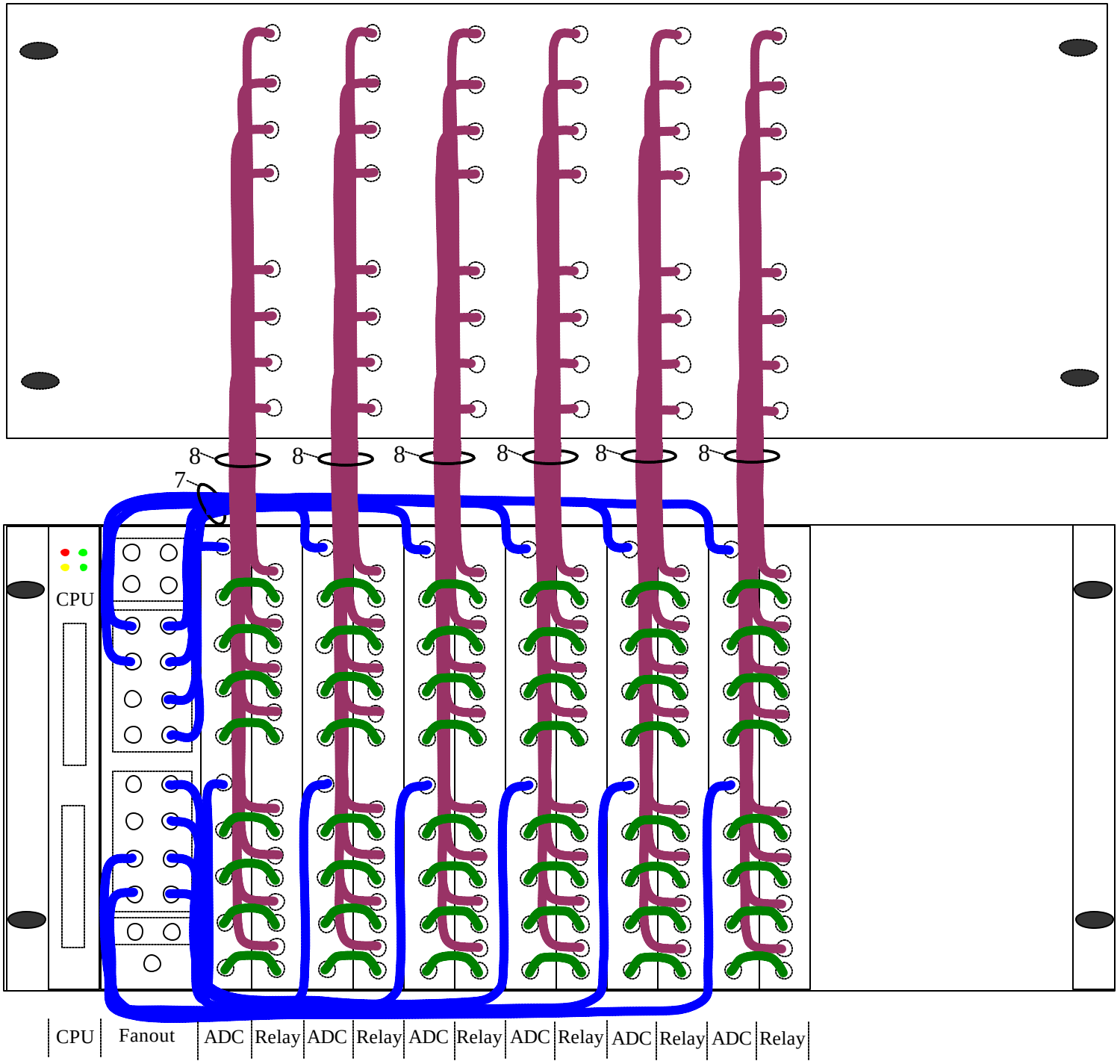
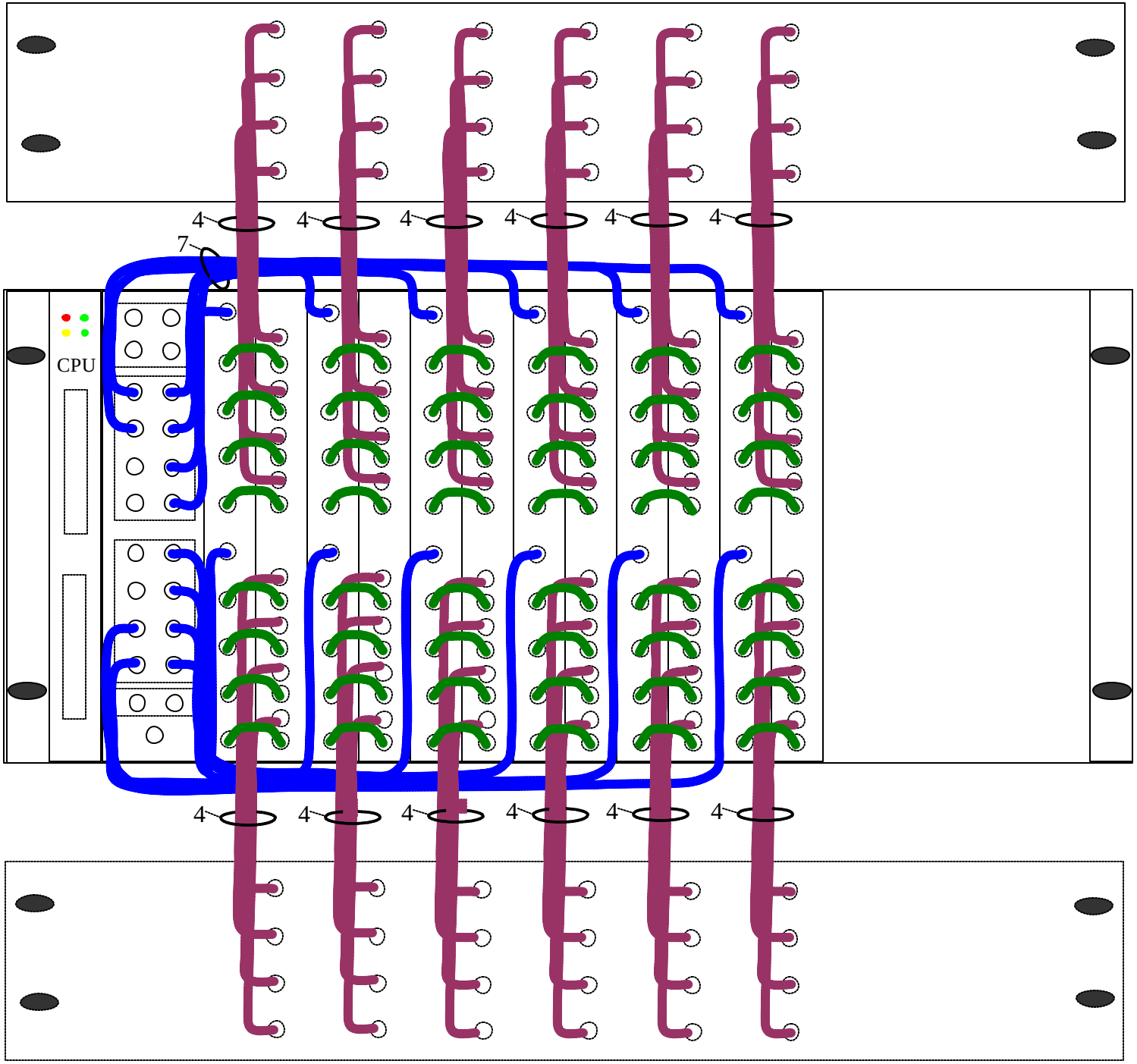
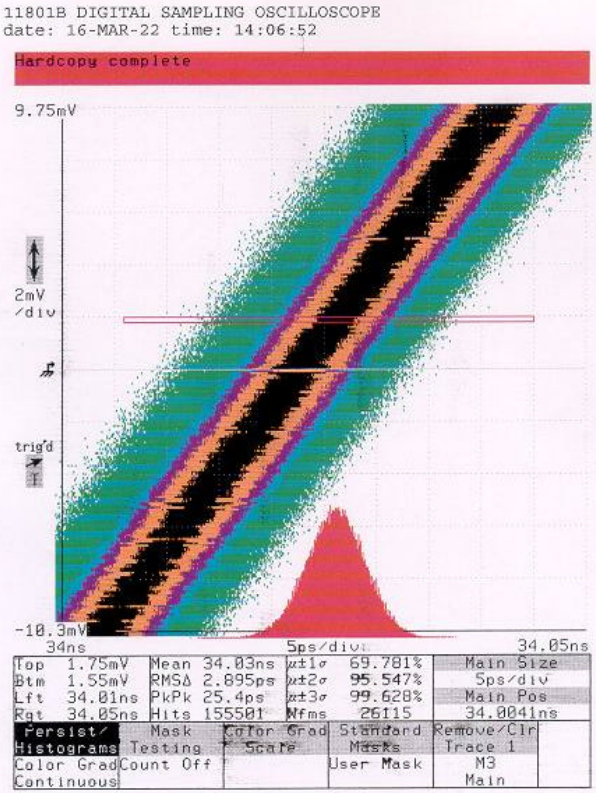

8
8
8
8
8
8
7
CPU
CPU
Fanout
ADC
Relay
ADC
Relay
ADC
Relay
ADC
Relay
ADC
Relay
ADC
Relay


4
4
4
4
4
4
7
CPU
4
4
4
4
4
4

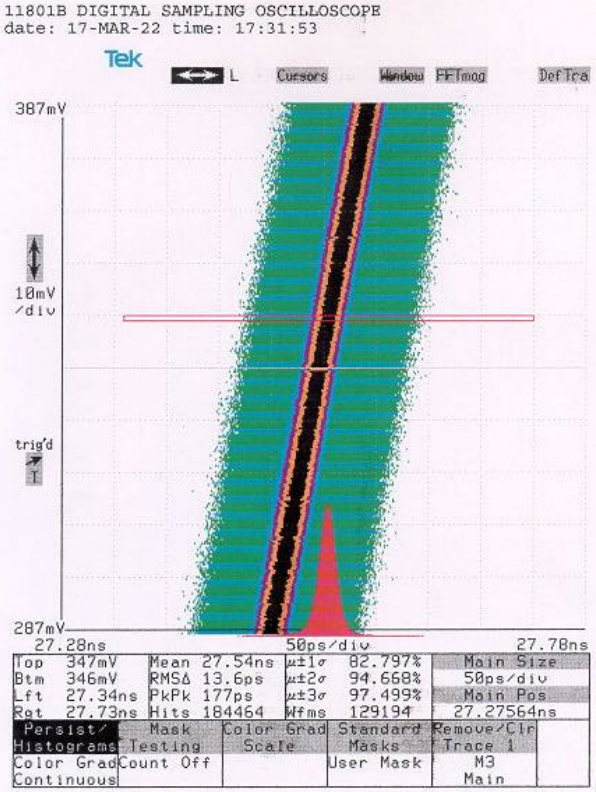
Accelerator Clock Jitter
Measurement

Conner Winfield
Free running



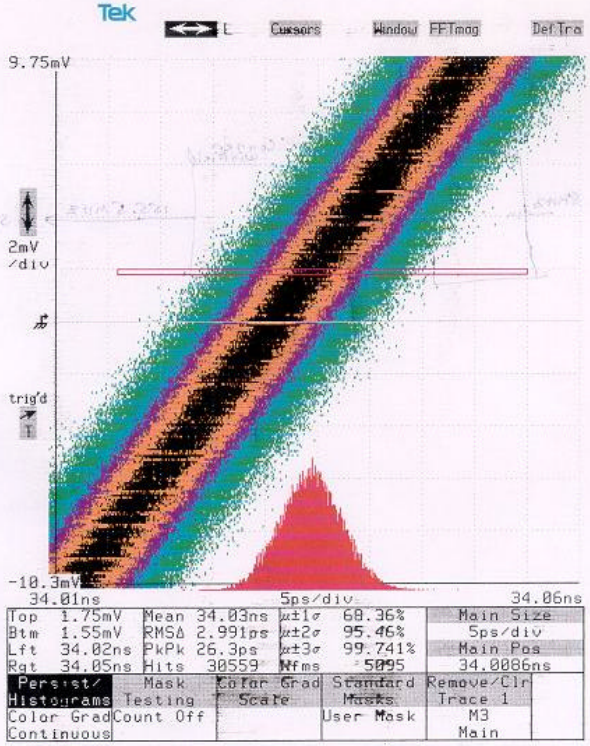
Conner Winfield Jitter
Free Running

Conner Winfield
input clock jitter

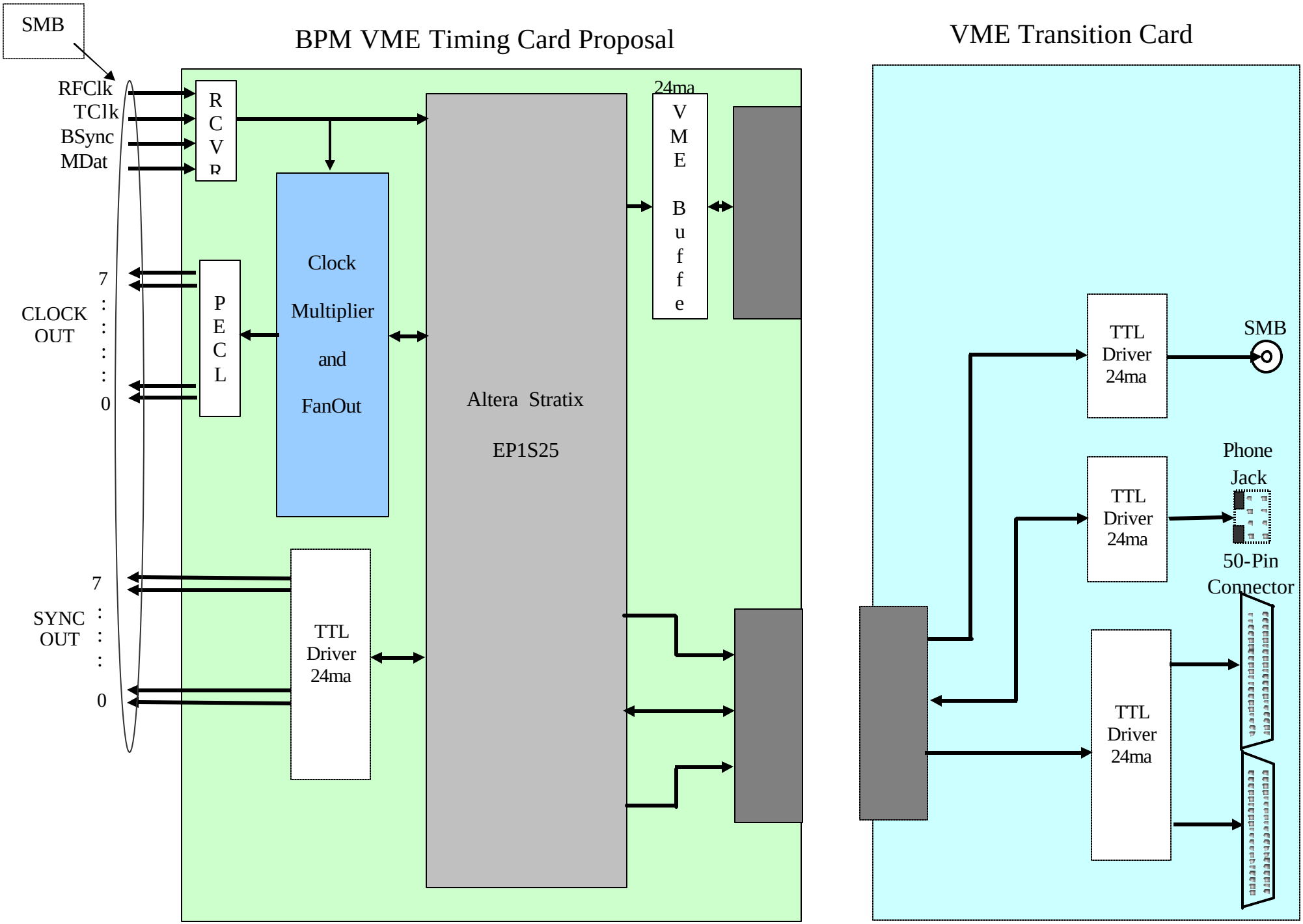


Conner Winfield
Input Clock Jitter

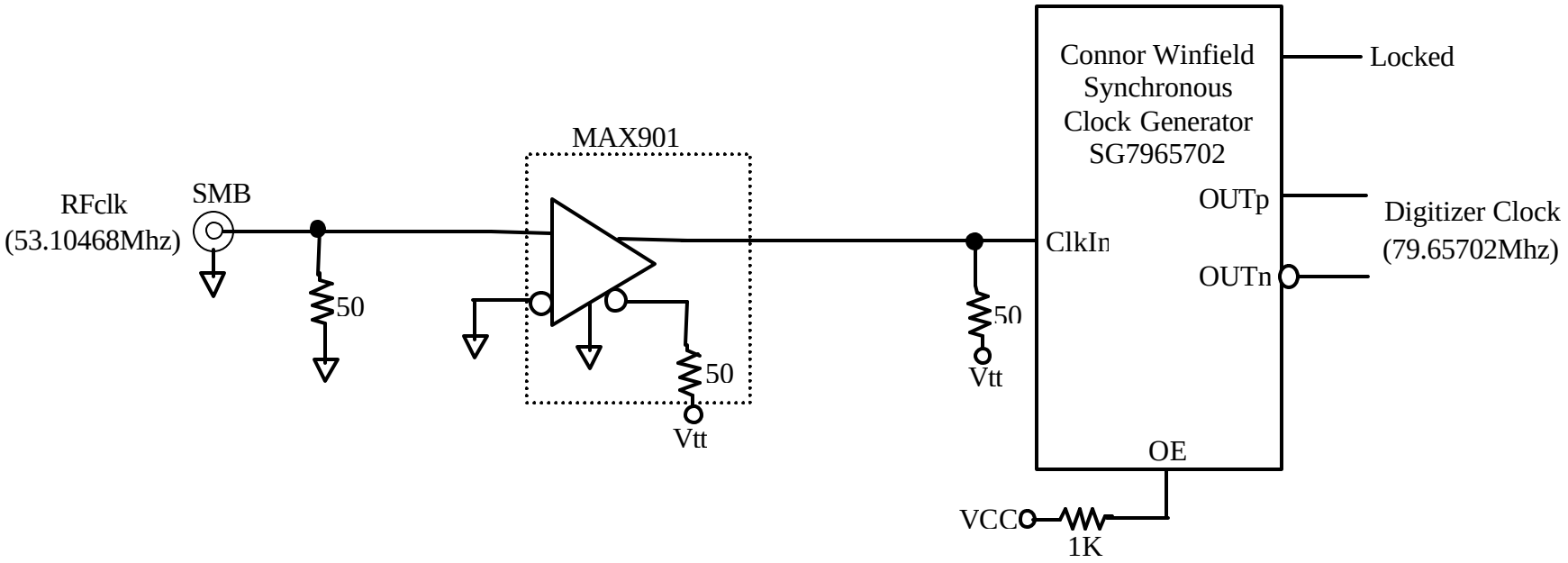
Conner Winfield
output = 155.5 MHz
Locked To 51.84 MHz



Conner Winfield
Output Clock Jitter
Locked to Input


BPM VME Timing Card Proposal
VME Transition Card
SMB
RFClk
TClk
BSync
MDat
R
C
V
R
24ma
V
M
E
B
u
f
f
e
Clock
Multiplier
and
FanOut
P
E
C
L
7
:
:
:
:
0
CLOCK
OUT
Altera Stratix
EP1S25
7
:
:
:
0
SYNC
OUT
TTL
Driver
24ma
TTL
Driver
24ma
SMB
TTL
Driver
24ma
Phone
Jack
TTL
Driver
24ma
50-Pin
Connector

Clock Generation
(79Mhz)



Clock Fanout Section