Tevatron
Beam Loss Monitor (BLM) Replacement Project

System Description

Review 4/19/04

Alan Baumbaugh (PPD/EED)

BLM Review

- General Comments on the old BLM system:
- The existing BLM system is ~ 23 years old.
- The existing BLM aborts fast ~ 50-100 microseconds.
- The existing BLM updates data slowly ~ 3 milliseconds.
- The existing BLM has two abort levels, high and low field.
- The existing BLM is read out via the old BPM system using the EDB (External Device Bus).
- The existing system has up to 12 Channels per crate.
- There are ~ 35 systems in the Tevatron and a like number in Booster and Main Injector.
- The existing BLM is NOT allowed to Abort Colliding beam.
- The BLM system has performed well and had a good long life.

BLM Review

- BLM Replacement Project Cast of Characters:
  - Stephen Pordes (AD/DH)
  - Alan Baumbaugh (PPD/EED)
  - Kelly Knickerbocker (PPD/EED)
  - Craig Drennan (AD/BS)
  - Jonathan Lewis (PPD/CDF)
  - Marvin Olson (AD/ID)
  - Alberto Marchionni (AD/MID)
  - Bill Haynes (CD/CEPA)
  - Charles Nelson (PPD/EED)
  - et.al.

BLM Review

- BLM Replacement Considerations:
- The new system should:
- Provide the same or increased dynamic range as the old system.
- Maintain a variety of circular buffers to aid in the reconstruction and diagnostics of abort events and aperture scans.
- Provide an array of machine states and associated abort types and limits.
- Respond to TeV Clock events.
- Respond to MDAT state events.
- Provide the same or enhanced “Flash”, “Profile”, and “Display” frames.
- Interface to the “Old” and “New” BPM system to ease installation for both hardware and software compatibility.
- Use same rack space, connectors, cables, and I/O protocol.
- Compatibility with Main Injector, and Booster is desirable.

BLM Review

- BLM Replacement Considerations:
- The New system should:
- Provide the same robust performance and reliability as the old system.
- Fit in same space, use same connectors and cables as old system.
  - This forces us to use a 3U crate
- Be reliable enough to Abort the Colliding Beam.
- Provide multiple abort types and thresholds for each Tevatron state.
  - 1) Instantaneous Loss
  - 2) Fast Loss
  - 3) Slow Loss
  - 4) Very Slow loss
- Provide for abort multiplicity for each abort type.
- Provide adequate resolution and dynamic range.
- Provide adequate time stamps to allow synchronization with the BPM system.

Tevatron BLM Review

- BLM Replacement Philosophy:
- The basic philosophy we have chosen is to integrate and digitize at a sufficiently high rate to allow the system to be flexible, capable of measuring losses over a wide range of time intervals, ~12 microseconds to many seconds. The Tevatron would be 21 microseconds.
- Different time scales are handled by firmware and software which adds measurements together to create sliding sums, instead of different digitizer cards for different machines.
- Abort limits are compared against the sliding sums.
- Each abort type will have an abort multiplicity associated with it, this is the minimum number of channels requesting an abort before the actual abort line is pulled.
- We will support 64 different machine states, and will have abort thresholds and multiplicities for each of these. Each state also has an abort mask for each channel. Masked off channels are not allowed to abort but are still read out.

Tevatron BLM Review

- BLM Replacement Philosophy (cont.):
- New system will use same cables, connectors, and rack space as old system.
- The machine states can be switched by TCLK events or MDAT data.
- We will store a variety of circular buffers for event diagnostics.
- All data time stamped with microsecond resolution for synchronization with BPM system.

- Front End:
- The front end will use a dual integrator with 2 channels, A and B, operated in a “Ping- Pong” mode, so that we have no dead time or missing losses.
- We will digitize the integrator output to 16 bits.
- We will keep 32-bit sliding sums.

Tevatron BLM Review

- BLM Replacement Performance:
- Provide high dynamic range ~ 285 Rad/sec. down to 0.087 microRad/sec. We could double these numbers and cover up to 570 Rad/Sec.
- Noise level with 600 ft. RG-58 cable ~ 5.6 microRad in 1 millisecond. (These measurements were done on the bench.)
- 16-Bit ADC with 32-Bit sliding sums.

- Provide "Gapless" History of losses:
  - 1) 0.8 seconds at 20 microsecond interval
  - 2) 8 seconds at 1 millisecond interval
  - 3) 800 seconds at 100 millisecond interval

System Reliability

- The System will include monitors for Temperature, and Voltage for all power supplies.
- The system will fail “gracefully” -- it will NOT assert the abort line if it loses power.
- It will continue to monitor losses without Host input.
- Card Slots and Cards are “Keyed” so only correct card can be installed.
- System will include self-test features.

Tevatron BLM Review

- BLM Replacement System Components:
- CPU
- Digitizer Cards
- Clock Decoder and Controller Card
- I/O Card
- Abort Controller Card
- Chassis & Power Supplies

Tevatron BLM Review

- CPU Card:
- Controls everything in the crate and moves and maintains data.
- CPU (Zilog eZ80), a 50 MHz, 24 bit Z-80. Programmed in either C or Assembly.
  - Chosen due to past experience and existing code.
  - CPU is upgradeable if needed to any PC-104 module (e.g. PowerPC) (Adapter required)
- Flash Program Memory (1 Megabyte)
  - Contains operating code
- Static RAM Memory (7 Megabyte)
  - Contains abort limits and settings array
  - Circular data buffers

Tevatron BLM Review

- CPU Card Software:
- Programmed in C and/or Assembly. Assembly preferred.
  - Handles all circular buffers except raw measurement (hardware).
  - Loads parameters into digitizer, and abort control cards based on machine state.
  - Receives TCLK and MDAT events.
  - Gets settings via I/O Card for each machine state, abort type, multiplicity, mask, and threshold. These are stored locally and will keep working if the external data link is lost.
  - Keeps snap shot buffer in RAM.
  - Keeps slow snap shot buffer in RAM.
  - Maintains “Flash”, “Profile”, and “Display” frame buffers (response to TCLK).

Tevatron BLM Review

- Digitizer Card:
- 2 Loss Monitor Channels
- Each Channel has a Dual Charge Integrator (Burr Brown ACF2101)
  - Operated in ping-pong mode
  - Alternately integrating or being readout and reset
- A 16-Bit SAR ADC
- An FPGA
  - Controls integrator
  - Reads ADC
  - Stores readings (raw measurements)
  - Keeps running sums
  - Does abort threshold comparisons and sends results to Abort CNTL.
- An MADC output for each channel
- 128 kByte RAM for storing 32k raw measurements in circular buffer

Tevatron BLM Review

- Clock Decoder and controller Card:
- TCLK decoder to allow system to receive encoded clock events
- MDAT receiver to get machine state changes
- Real Time Clock for Data Tagging (Set via I/O from Host)
- 32-Bit microsecond counter referenced to TCLK reset events for fine time stamping and for synchronizing with BPM
- An FPGA to control the digitizer cards to keep all digitizers in sync
  - This also sets time for sampled measurements. (Snap Shot Buffers)
- A single time stamp buffer in sync with the 32k data buffers on the digitizer cards for time stamping Raw Measurement data

Tevatron BLM Review

- I/O Card:
- Standard EDB (External Device Bus) A8/D8 compatible with existing BPM
- Extended EDB A16/D16 Bus compatible with the new BPM system
- The Host downloads data to the BLM via the EDB to set alarm thresholds, multiplicities, etc.
- In the Tevatron the Host is a card in the BPM Crate
- 2 Megabytes of RAM for buffering data to Host

- This card may have a 10/100 BaseT interface for stand alone operation

Tevatron BLM Review

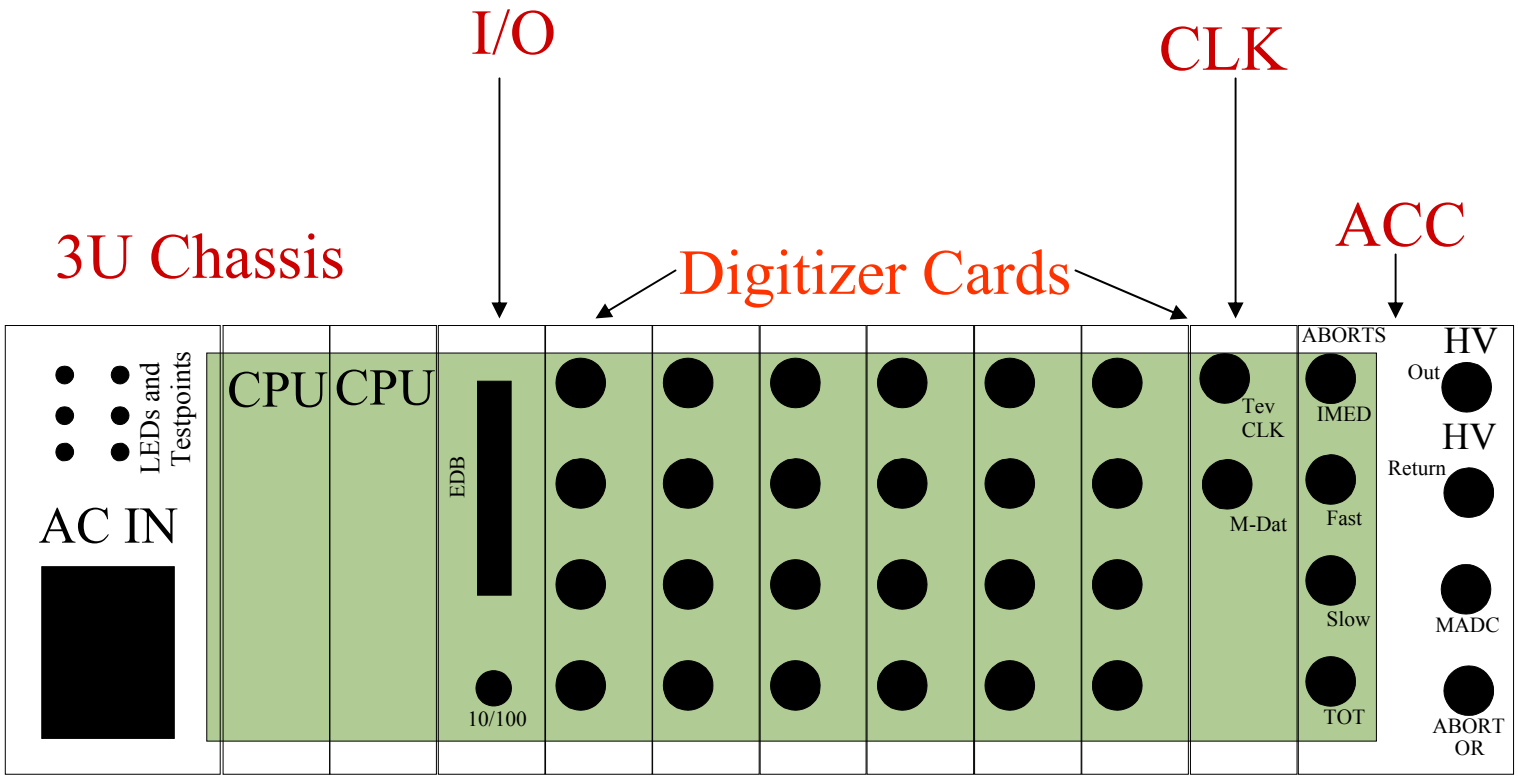
- Abort Controller Card:
- An FPGA which receives abort info from the digitizer cards, compares against abort masks and multiplicities and makes the abort signals.
- Aborts are formed in < 20 microseconds
- TTL Abort signals are driven off board on 50 ohm cables.

- This card also has the HV power supply and HV (out and return) read back
- Special selectable MADC output produced by CPU

Tevatron BLM Review

- Chassis and Power:
- Power Supplies
- Card Cage
- Custom Backplane
- Fans and Filters
- Temperature Sensors and Voltage monitors

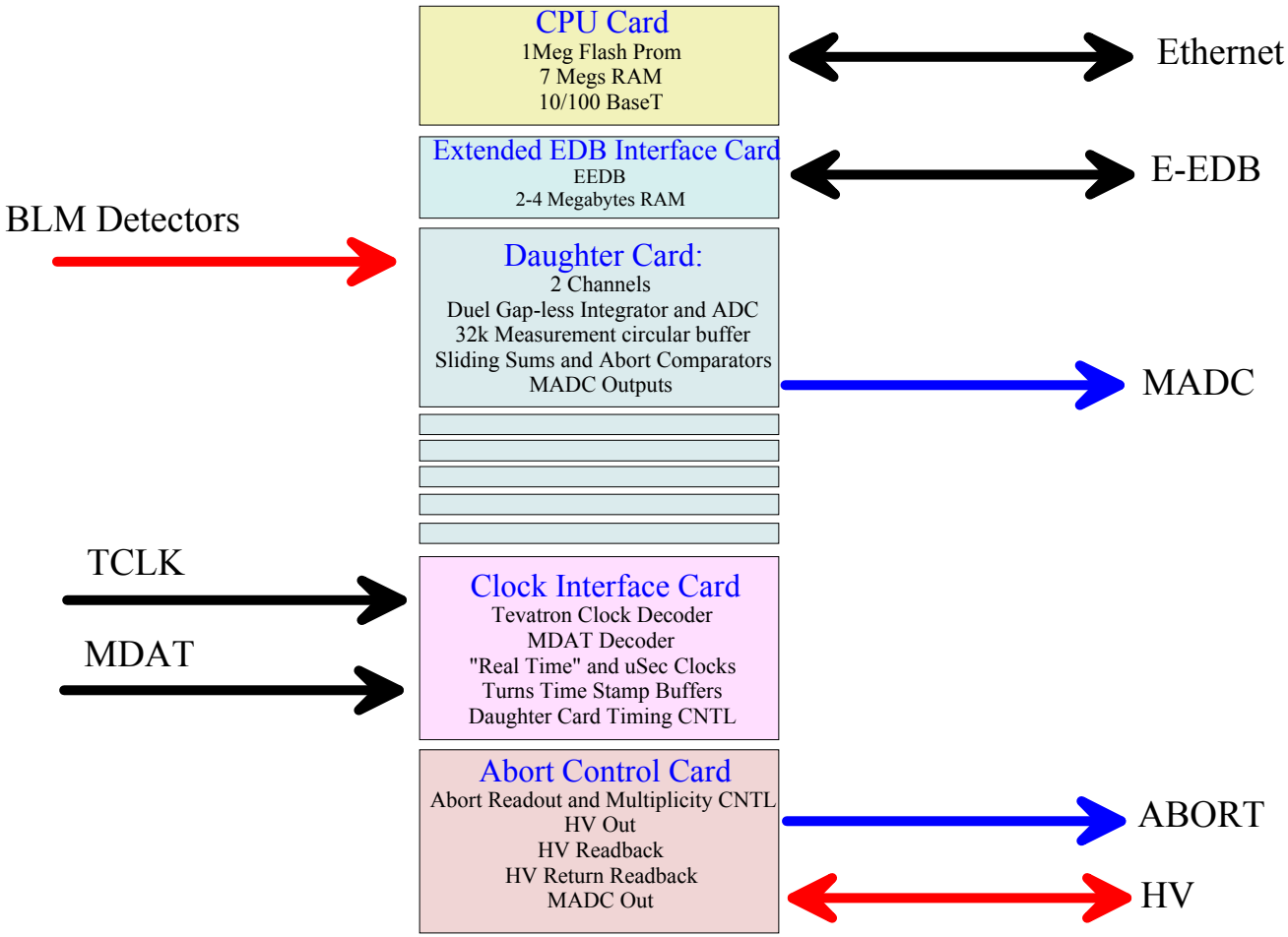
- Due to the requirement that the new system fit into the same rack space where the old system was, we have chosen a 3U Eurocard format.
- The card size will be 3U x 220.0 mm (3.937” x 8.661”)
- These requirements, and the need for point-to-point abort lines, did not allow us to use a standard backplane.



Rack Rear View

Green is Backplane

BLM Overview



Tevatron BLM Review

A 24 bit address space is adequate

BLM Memory Allocation

Digitizer Card Addressing

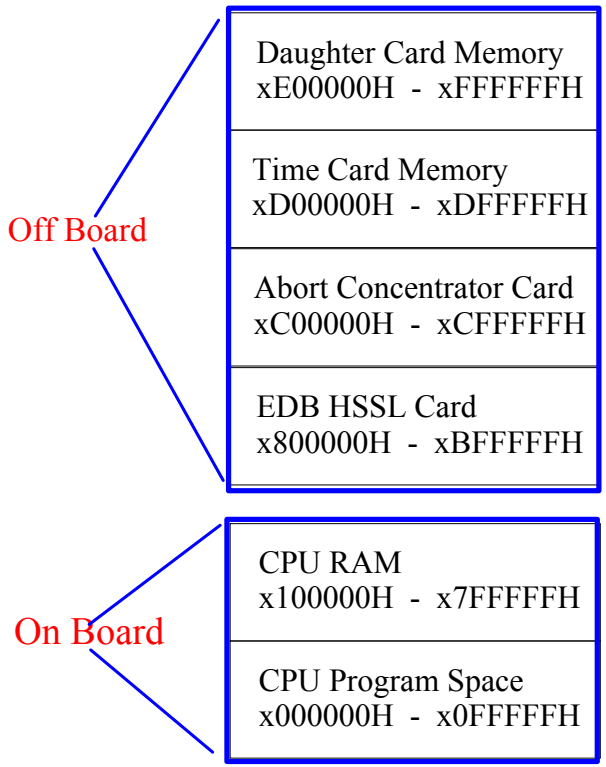
3 Bits Card Address
1 Bit Channel select
1 Bit Data/TBT
16 Bits Ram Address
daughter cards 2MB address space

Time Card

1 Bit Data/Cntl
3 bits time byte select
16 Bits Ram Address
time card 1 MB

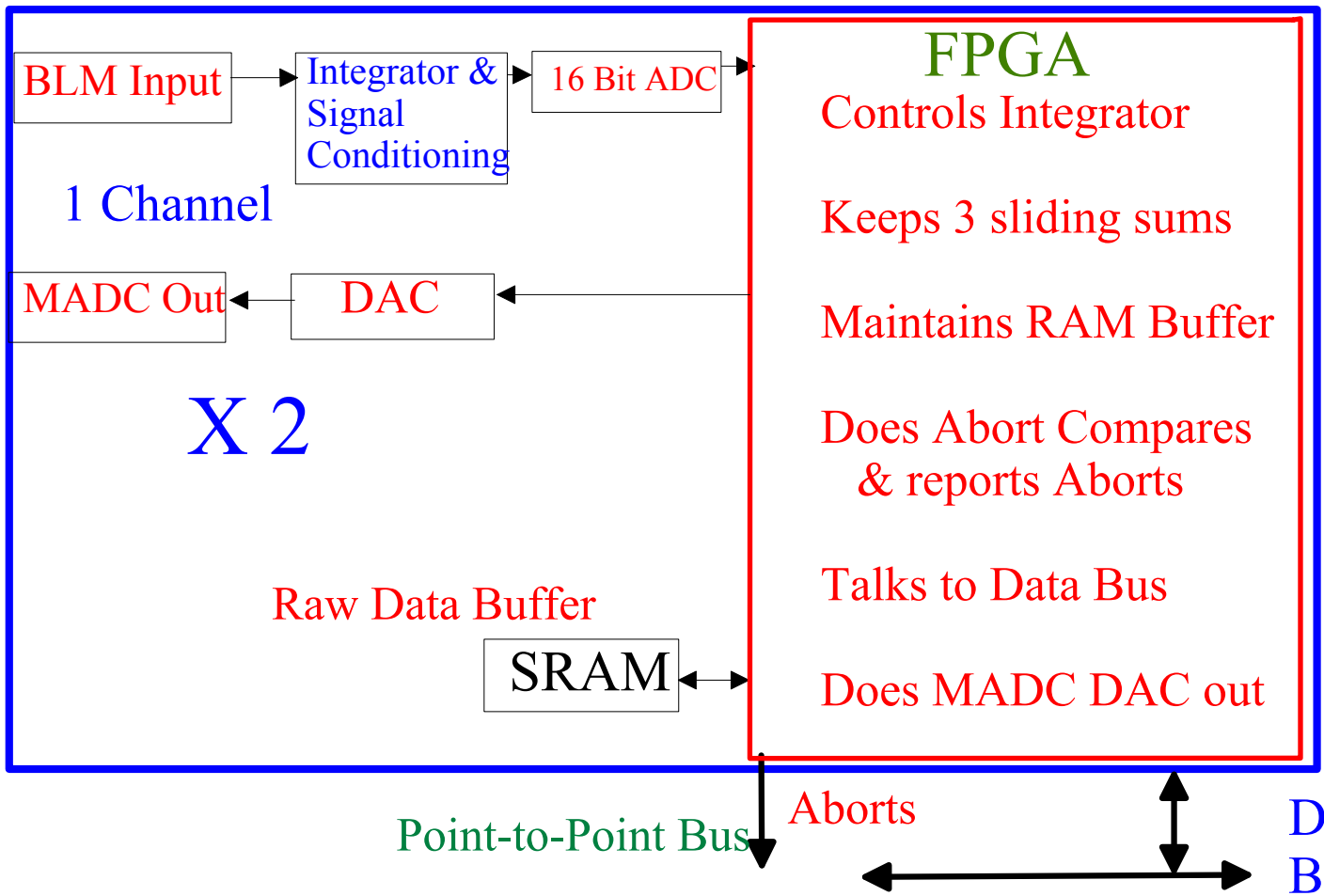
Abort Con Card 1MB
EDB Con Card 4 MB

CPU Prom 1MB
CPU RAM 7MB



BLM Digitizer Card

3U x 220 x 6hp Eurocard 2 Channels/card

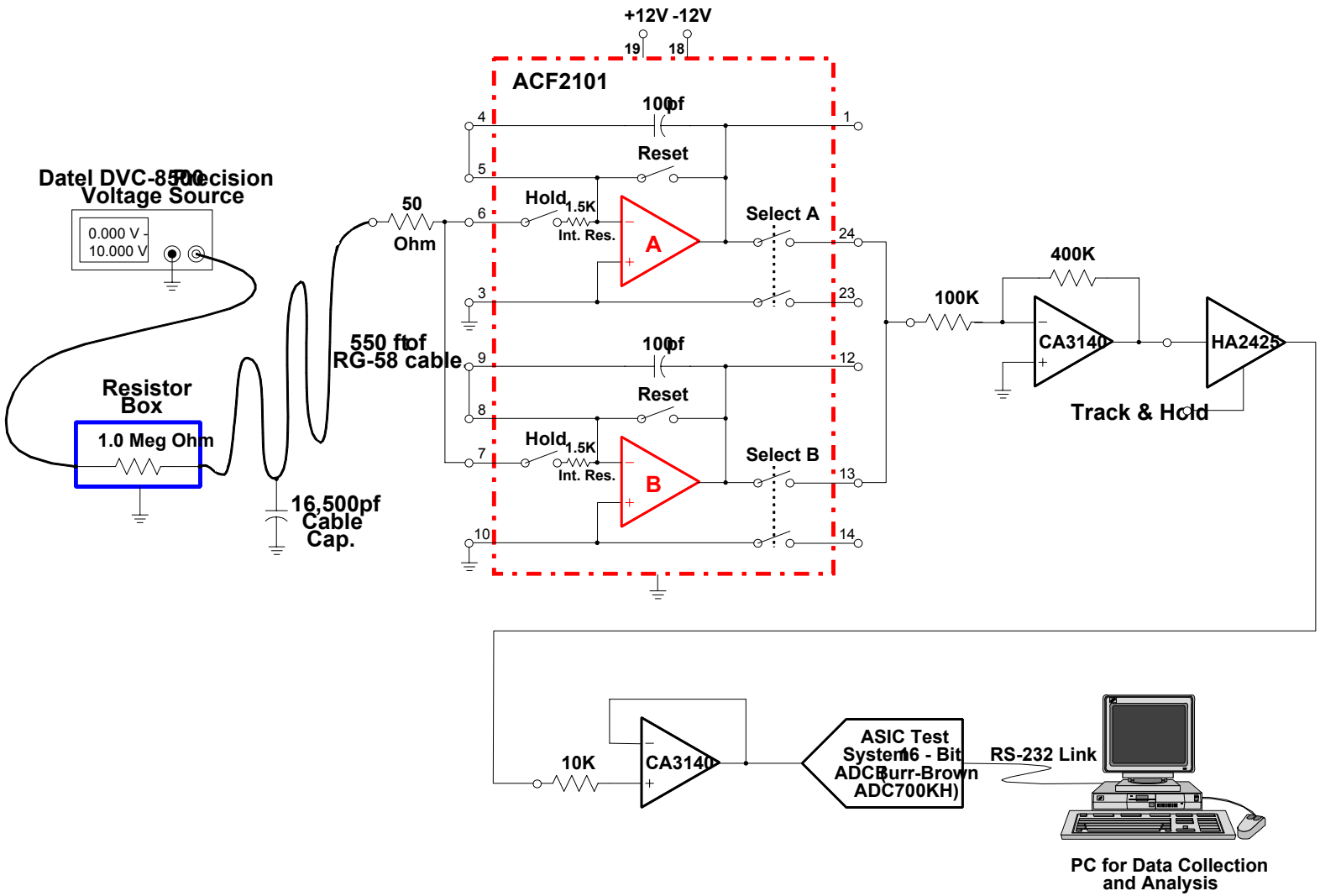


Front end Testing

- The ACF2101 was not optimized for large input capacitances. Before we could continue, we needed to know the ACF2101 would work in ping-pong mode with long (600 ft.) cables and the capacitance involved.
- We used a beamline BLM card which had an ACF2101 integrator on board, although we had to make several modifications to this card.
- We used our existing ASIC test stand to take data and make measurements.
- We ran the integrator output to a 16-bit ADC and setup the timing to be the same as the final system.

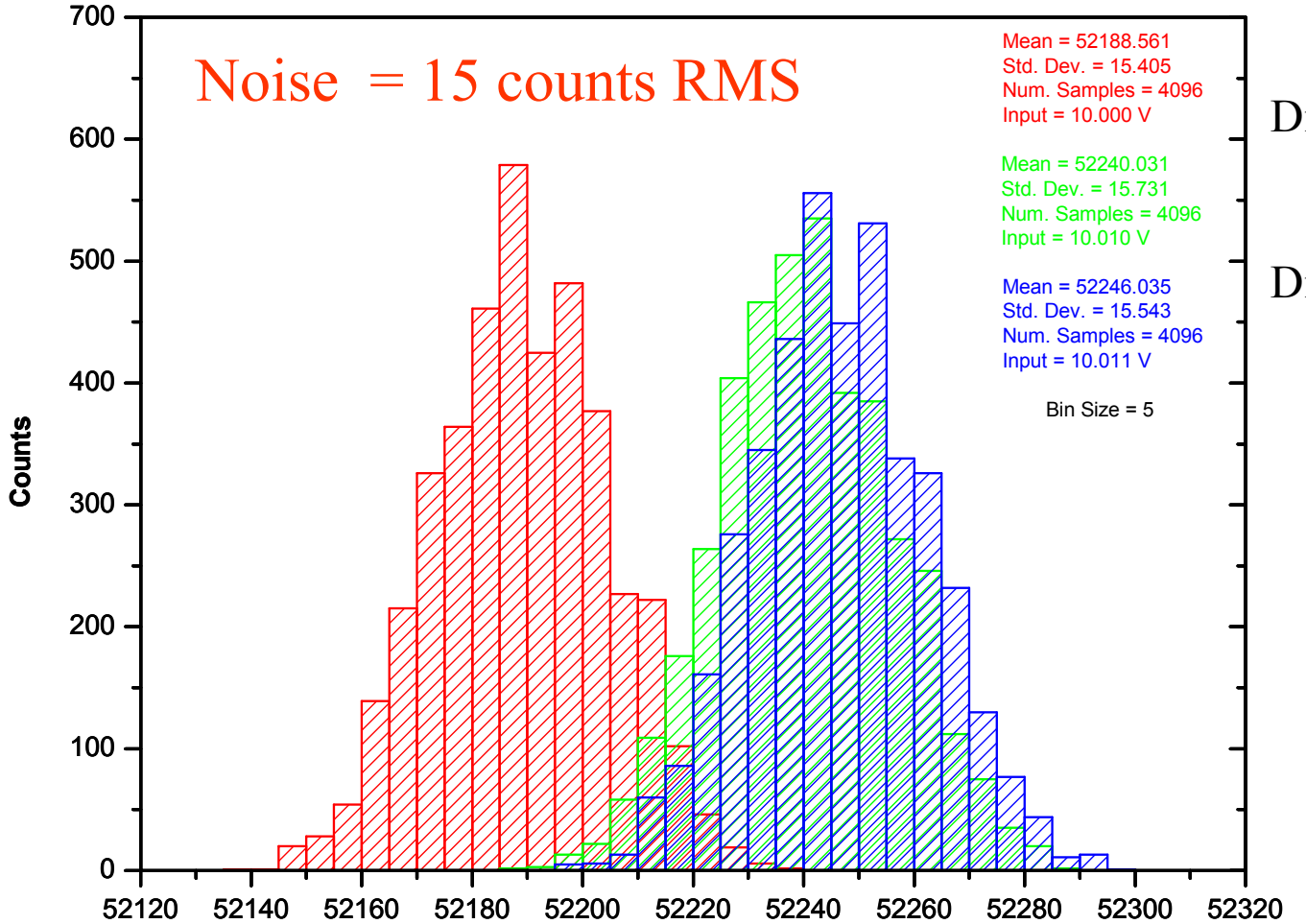
ACF2101 Test Setup Schematic

(Long Cable Configuration)



Linearity and resolution

200.0 pC = 52188 200.2 pC = 52240 200.22 pC = 52246



Diff = 52

Diff = 6

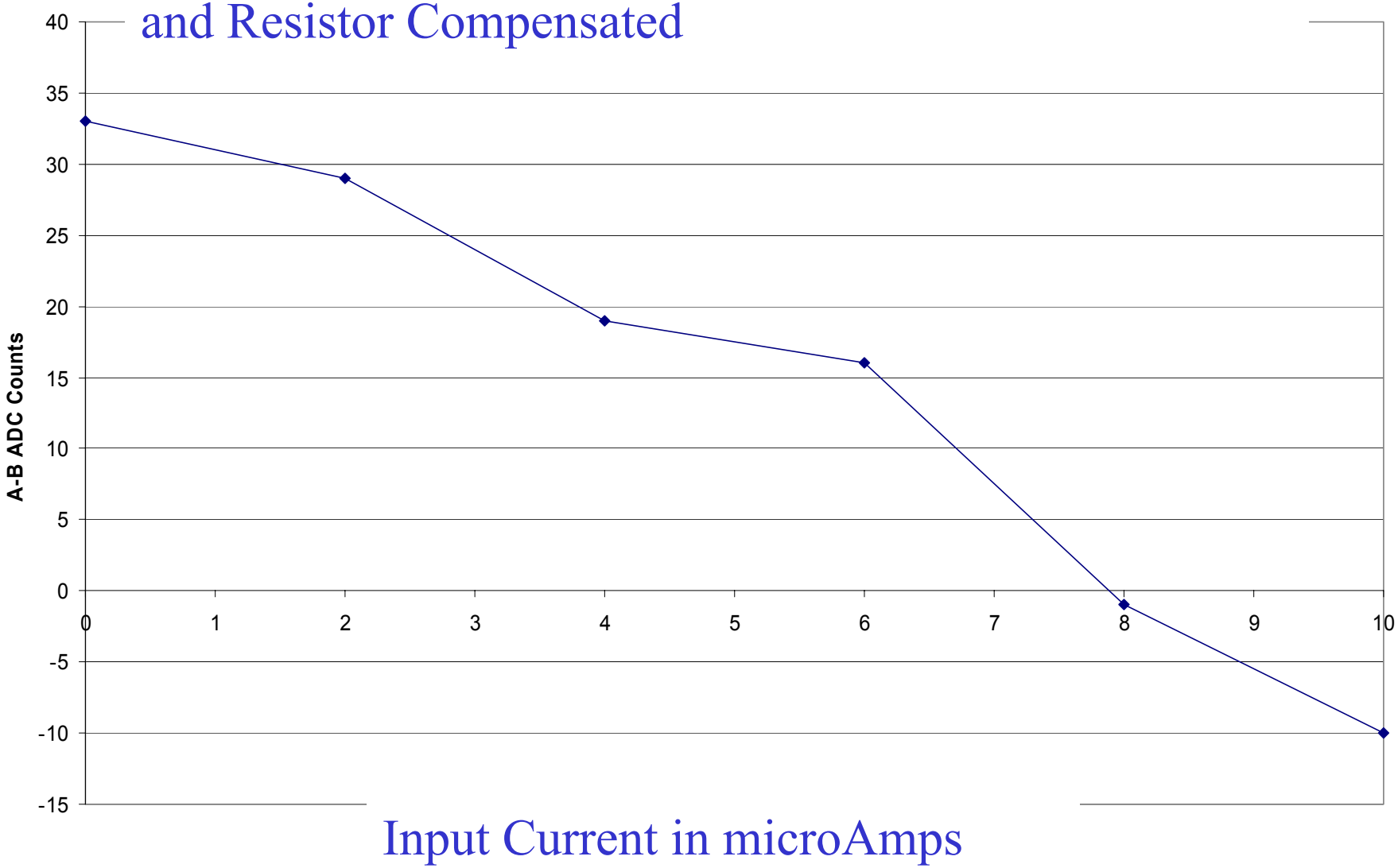
Ch. A, 550 ft. Cable, Input 10 + .000V, .010V, .011V, Sync ADC, (Files: BLM_A_L_100XX.DAT)

Figure 8.

Front end Testing Results

- The ACF2101 performed quite well although there were effects of the A and B channel differences which, with long cables cause shifts in the measured signal, effectively separating A and B. This is due to slight differences in the input voltage and switch resistance.
- We were able to remove these differences with a simple resistive network.
- This will require an initial calibration and setting of each dual integrator prior to being put into service.

A-B Channel Data vs Input, Long Cable Offset Nulled and Resistor Compensated



Tevatron BLM Review

- Cost Estimates/Guestimates

Chassis, CPU, HV etc:

Crate & Power	$500
Backplane	$300
HV Supply	$200
CPU Board	$500
Timing/CNTL	$400
E-EDB I/O	$400
Abort Control	$300
Connectors/LEDs	$200
Total/Chassis	$2800
Quantity = 40	
Total	$112,000

• Digitizer Cards:

PCB	$100
Connectors	$30
FPGA	$30
RAM	$65
ADC	$40
Mech Hardware	$65
Analog Parts	$50
Assembly	$50
LEDs	$10
Total/Card	$430
Quantity = 200	
Total	$86,000

M&S Cost = $198,000 without contingency

Prototyping, Instrumentation and Testing = $30,000

Talk stops here..

Extra slides start here…

Tevatron BLM Review

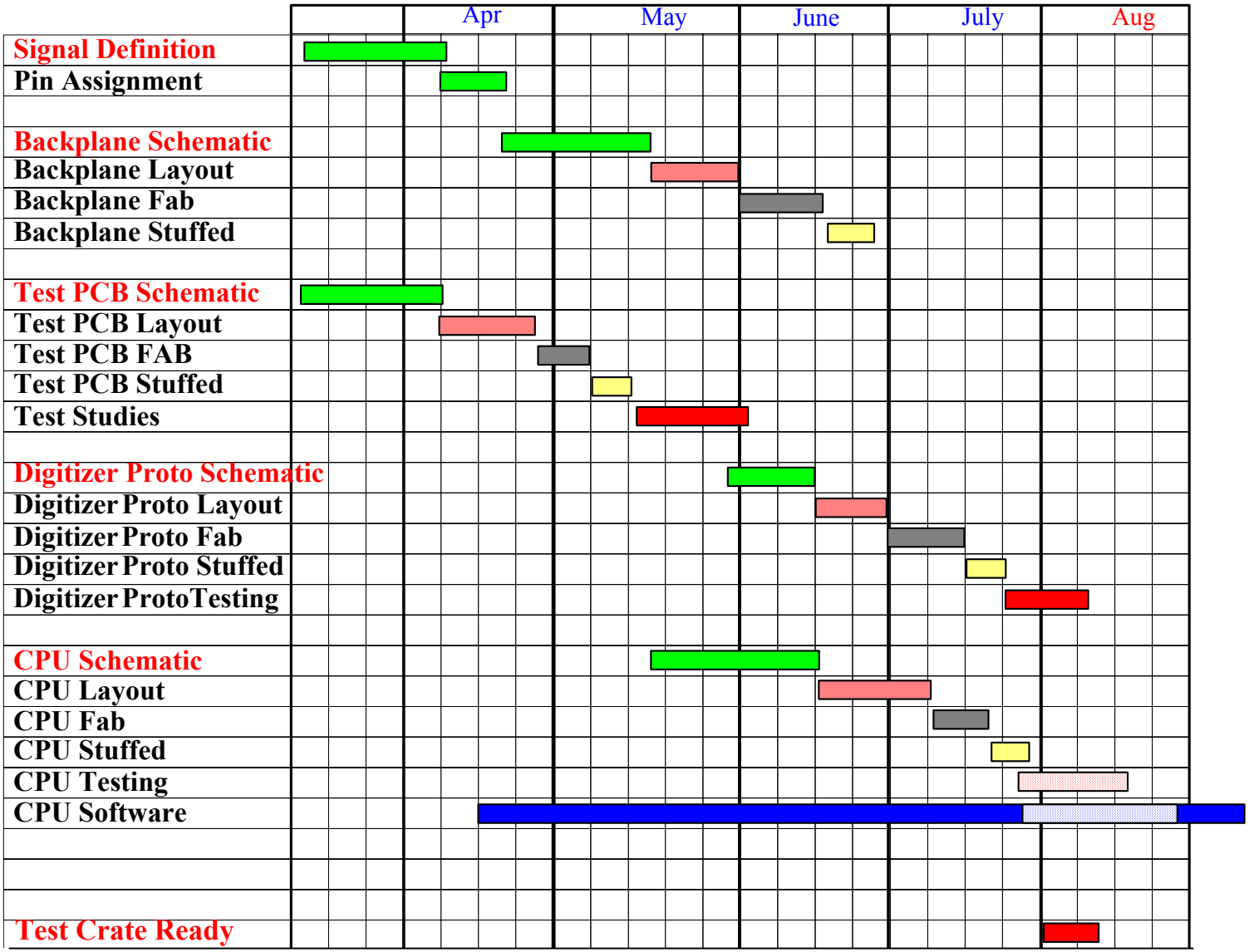
- BLM Replacement Prototype schedule:
- Provide prototype digitizer cards, crate, readout path by ~ Aug 2
- In order to test the key components of the system with real beam, in real beam environment we will need:
  - 1) >2 Digitizer Cards
  - 2) Crate, Backplane
  - 3) Timing Controller Card

- Readout using existing test stand CPU and EDB interface

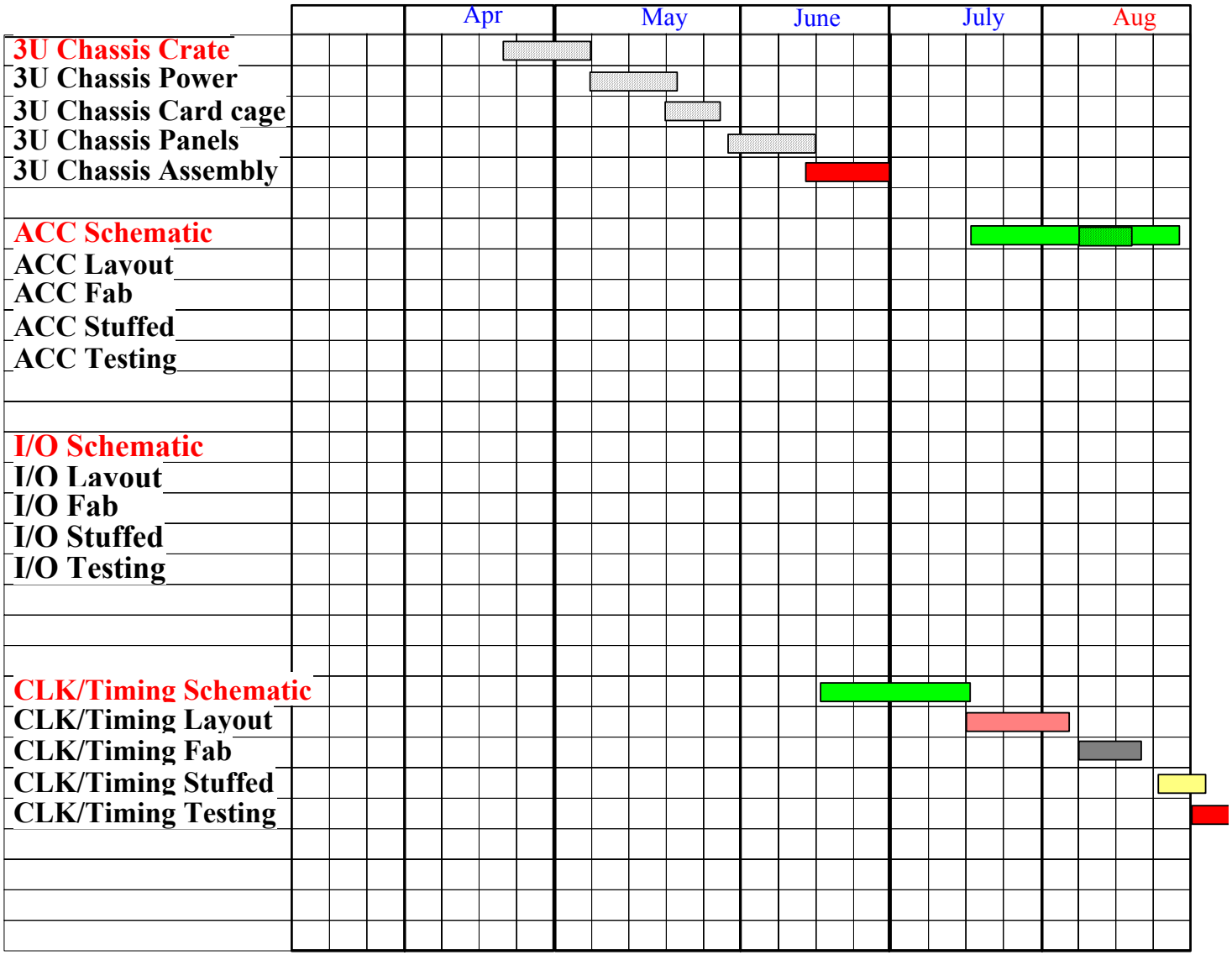
BLM Review

- BLM Replacement Production schedule:
- If digitizer tests are successful, in August we will order production quantities of parts.
- The remainder of the schedule is paced by the engineering effort required to design the other cards, and the system testing which involves the BLM project and machine people.
- If all goes well, we could have a full crate of pre-production cards to test by Feb 2005, this assumes 3 versions of digitizer card and 2 versions of all other cards.
- Single crate testing and modifications -- 3 months (Tevatron Only).
- This system is left in place to gain operational experience.
- Production, testing and installation of the full set of BLM Crates and systems -- 2 months + 2 months
- Sept 2005 system available

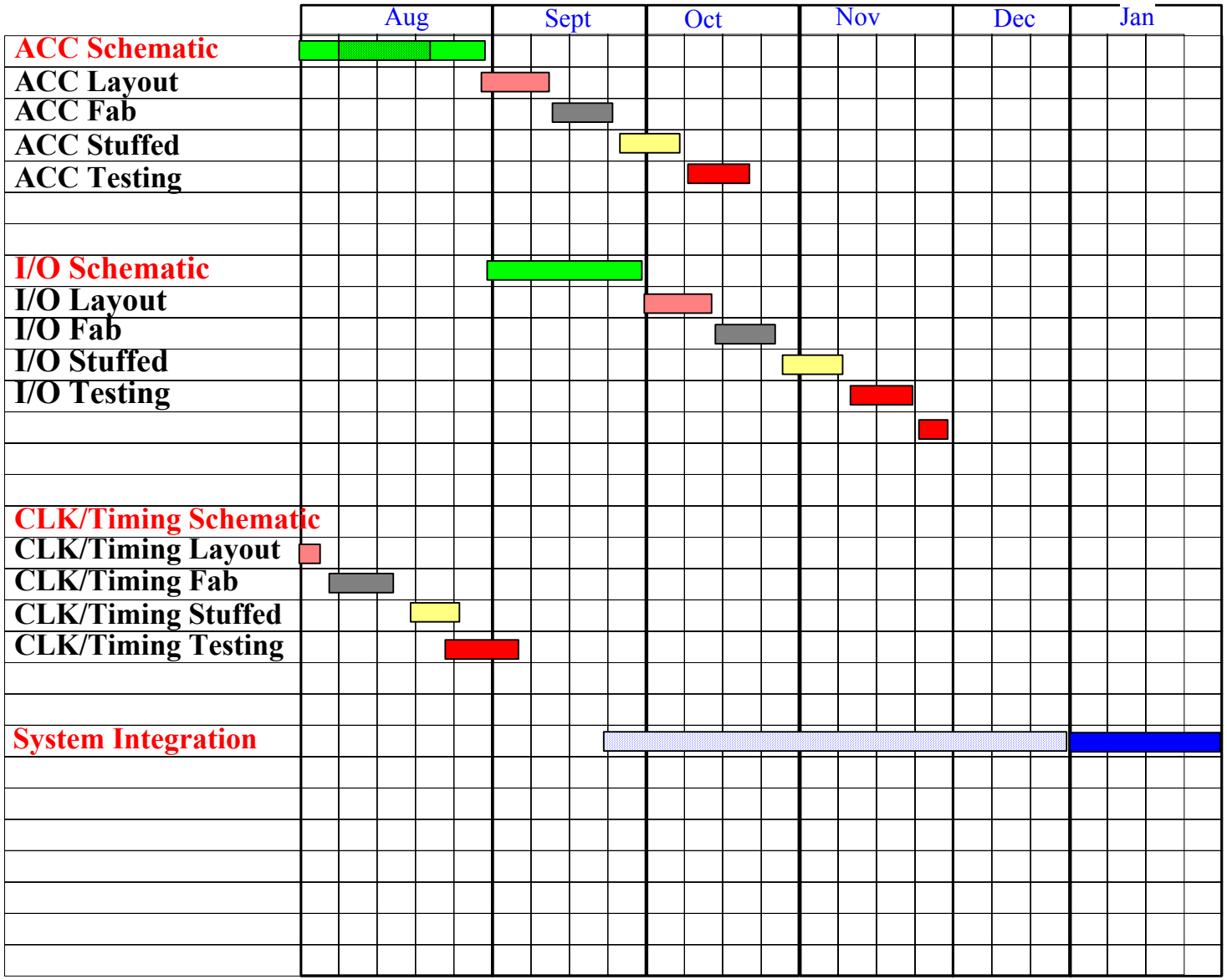
BLM Review


Apr
May
June
July
Aug
Signal Definition
Pin Assignment
Backplane Schematic
Backplane Layout
Backplane Fab
Backplane Stuffed
Test PCB Schematic
Test PCB Layout
Test PCB FAB
Test PCB Stuffed
Test Studies
Digitizer Proto Schematic
Digitizer Proto Layout
Digitizer Proto Fab
Digitizer Proto Stuffed
Digitizer ProtoTesting
CPU Schematic
CPU Layout
CPU Fab
CPU Stuffed
CPU Testing
CPU Software
Test Crate Ready

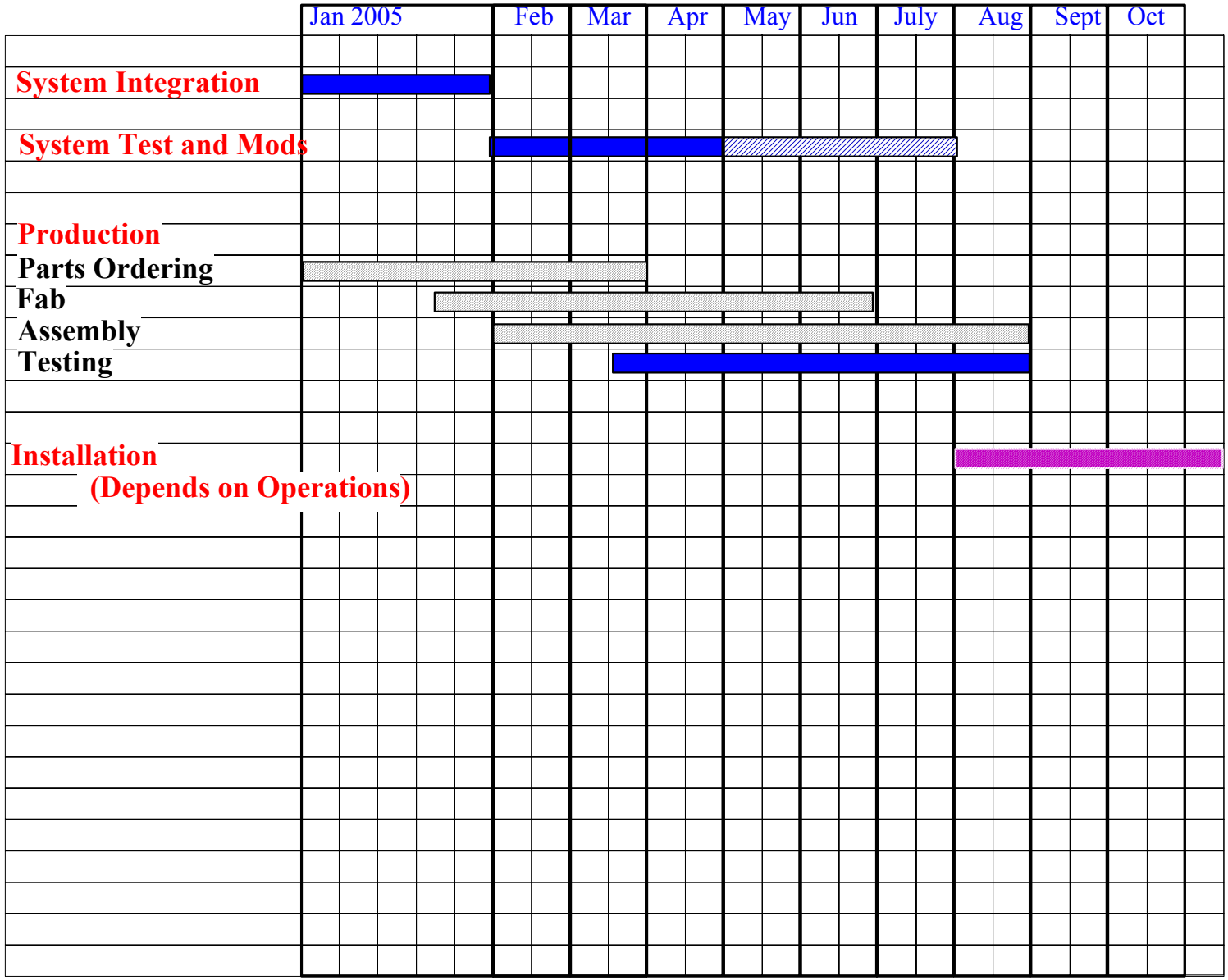
BLM Review


Apr
May
June
July
Aug
3U Chassis Crate
3U Chassis Power
3U Chassis Card cage
3U Chassis Panels
3U Chassis Assembly
ACC Schematic
ACC Layout
ACC Fab
ACC Stuffed
ACC Testing
I/O Schematic
I/O Layout
I/O Fab
I/O Stuffed
I/O Testing
CLK/Timing Schematic
CLK/Timing Layout
CLK/Timing Fab
CLK/Timing Stuffed
CLK/Timing Testing

BLM Review


Aug
Sept
Oct
Nov
Dec
Jan
ACC Schematic
ACC Layout
ACC Fab
ACC Stuffed
ACC Testing
I/O Schematic
I/O Layout
I/O Fab
I/O Stuffed
I/O Testing
CLK/Timing Schematic
CLK/Timing Layout
CLK/Timing Fab
CLK/Timing Stuffed
CLK/Timing Testing
System Integration

BLM Review


Jan 2005
Feb
Mar
Apr
May
Jun
July
Aug
Sept
Oct
System Integration
System Test and Mods
Production
Parts Ordering
Fab
Assembly
Testing
Installation
(Depends on Operations)

BLM Review

- BLM Replacement Current Status:

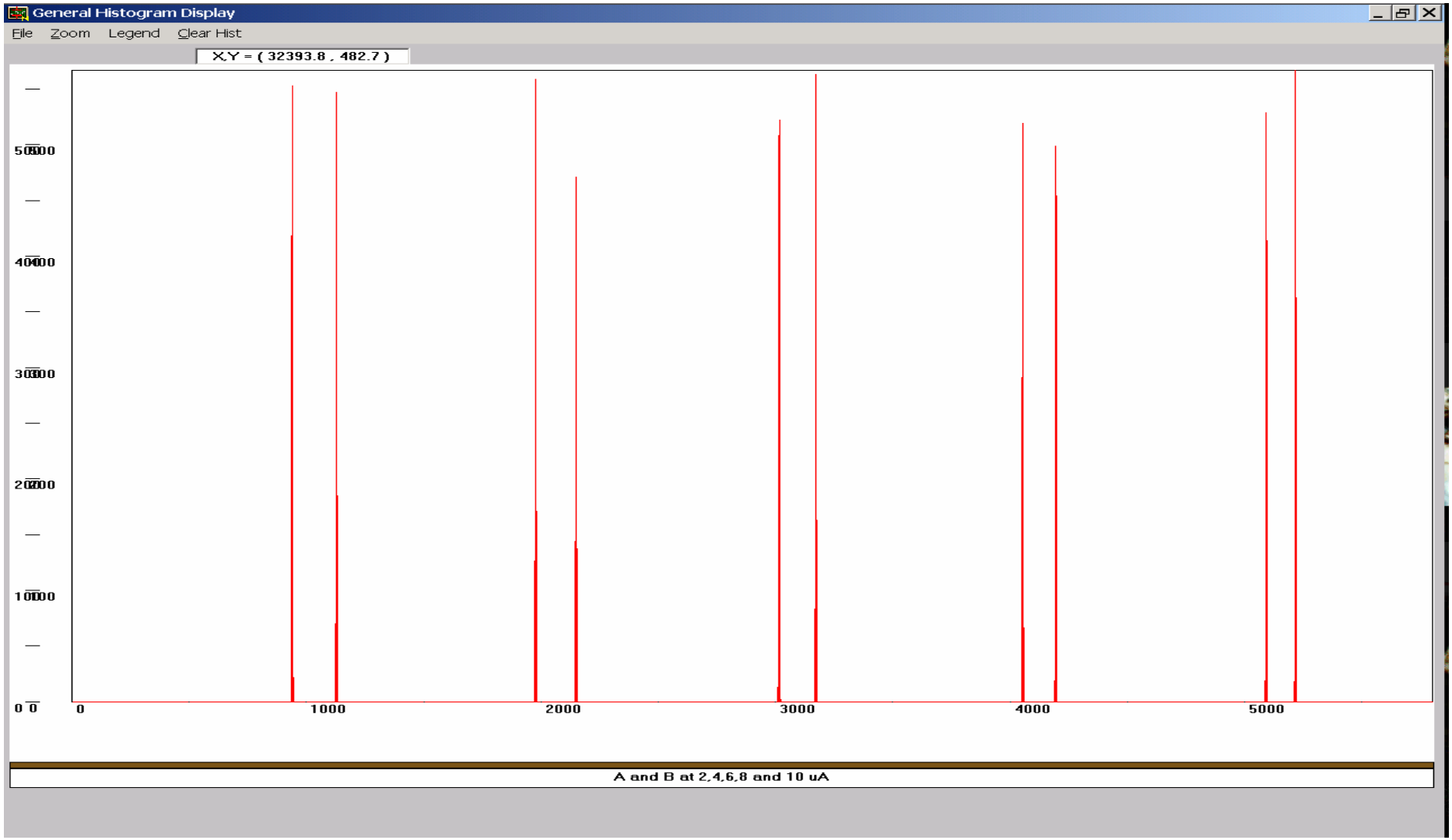
- Pre-Prototype Digitizer Card is in layout
- Analog Front end Testing nearly complete
- Backplane Schematic is nearly complete
- We are finalizing the specs in conjunction with Tevatron, Booster, and Main Injector personnel
- Work has started on Software for new CPU
- We are in the process of getting a sample 3U Crate from Rittal
- Architecture of the New CPU, Abort Controller Card, Timing Card, and EDB Interface Card are complete. Schematic work has not yet begun.

Tevatron BLM Review

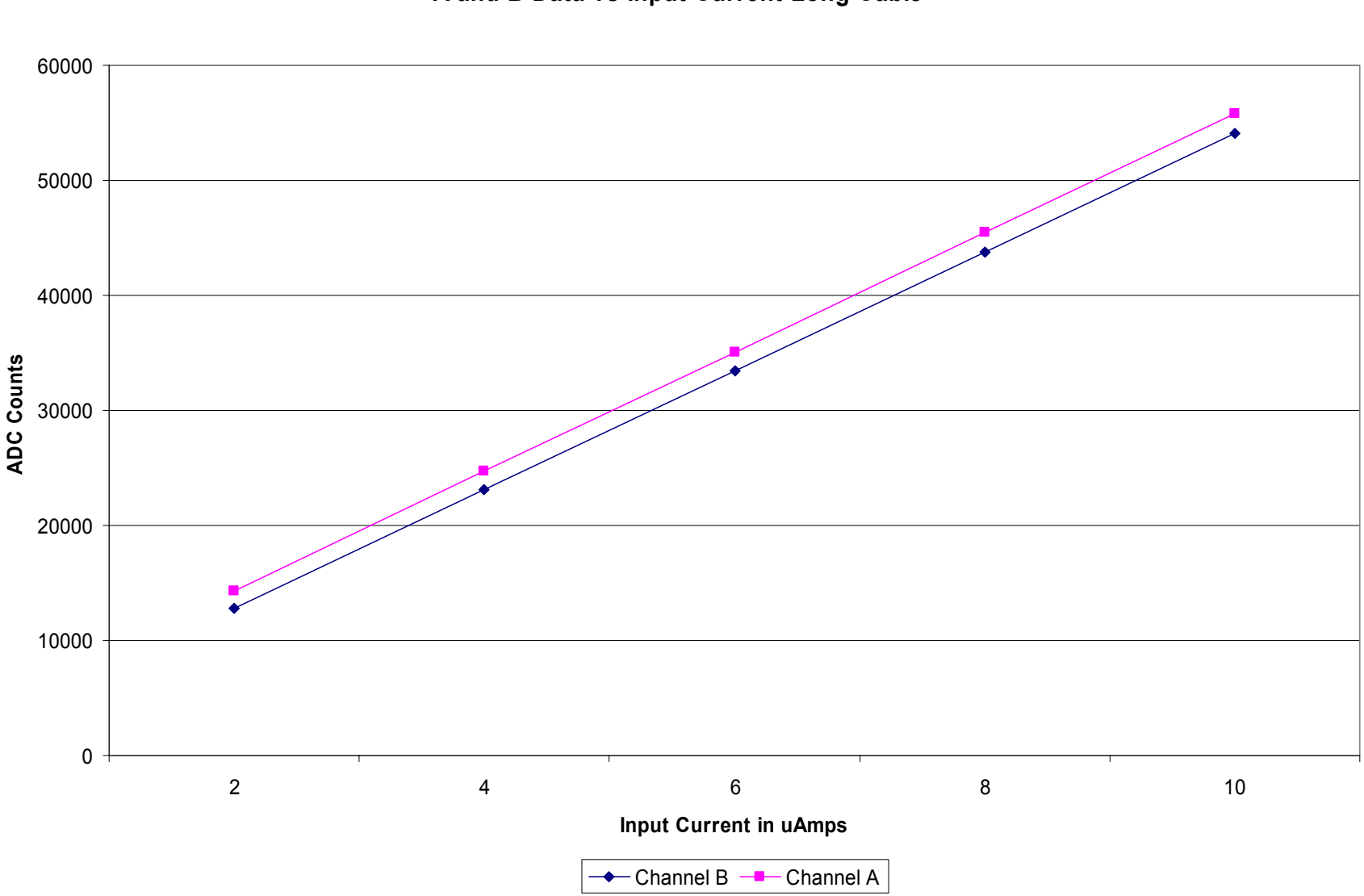
- Note: The full functionality of these systems will have to wait for ACNET front end software and application software to deal with the new BLM data structures. At installation the new BLMs will "look" like the old BLMs, which do not have the many buffers and abort modes of the new system.
- Initially we will most likely read out the new BLMs through the old BPM system.

- Software development will continue in both Host and front ends for some time.

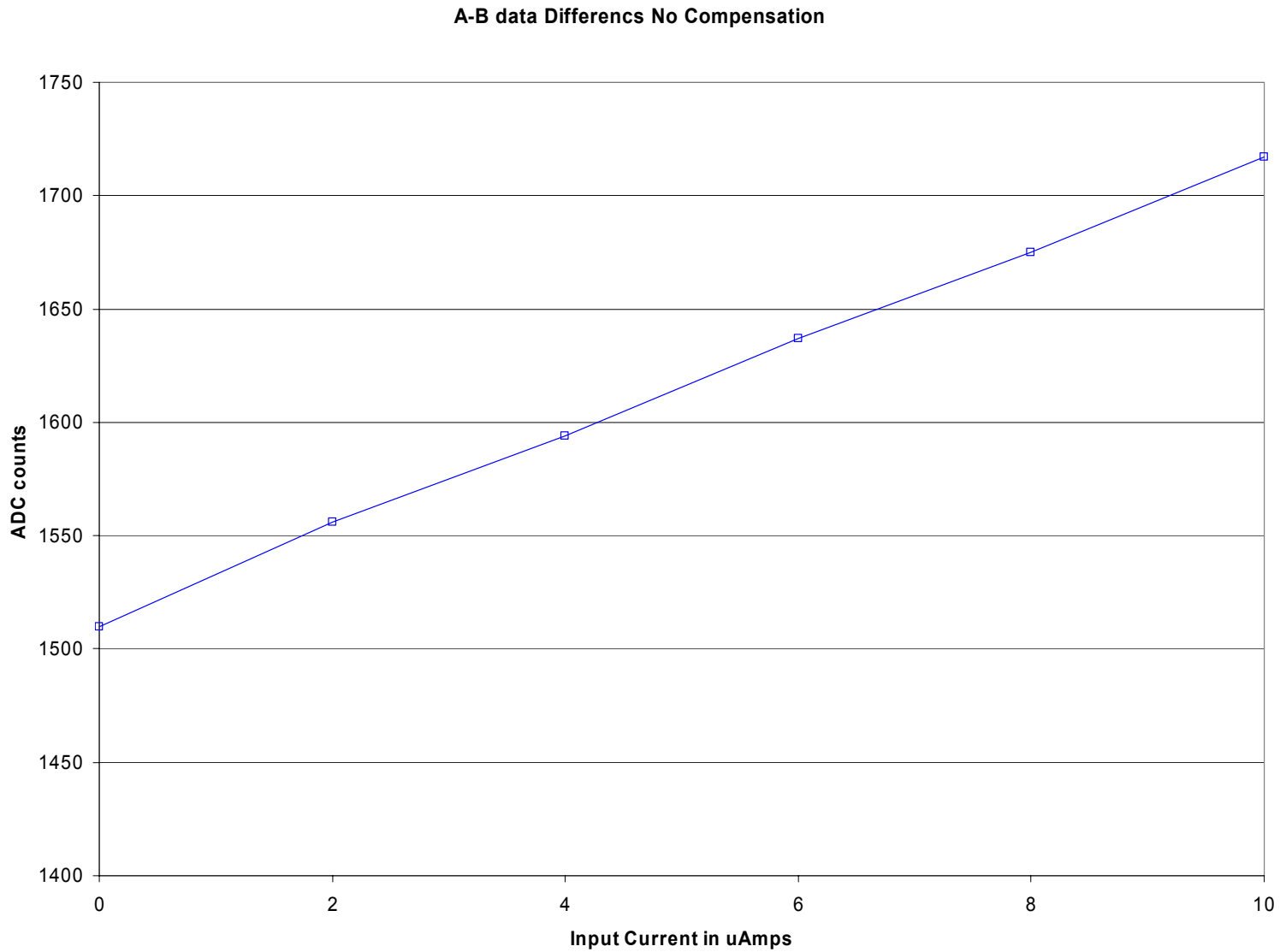
BLM Review


General Histogram Display
File
Zoom
Legend
Clear Hist
XY = (32393.8 , 482.7)
0
1000
2000
3000
4000
5000
A and B at 2,4,6,8 and 10 uA

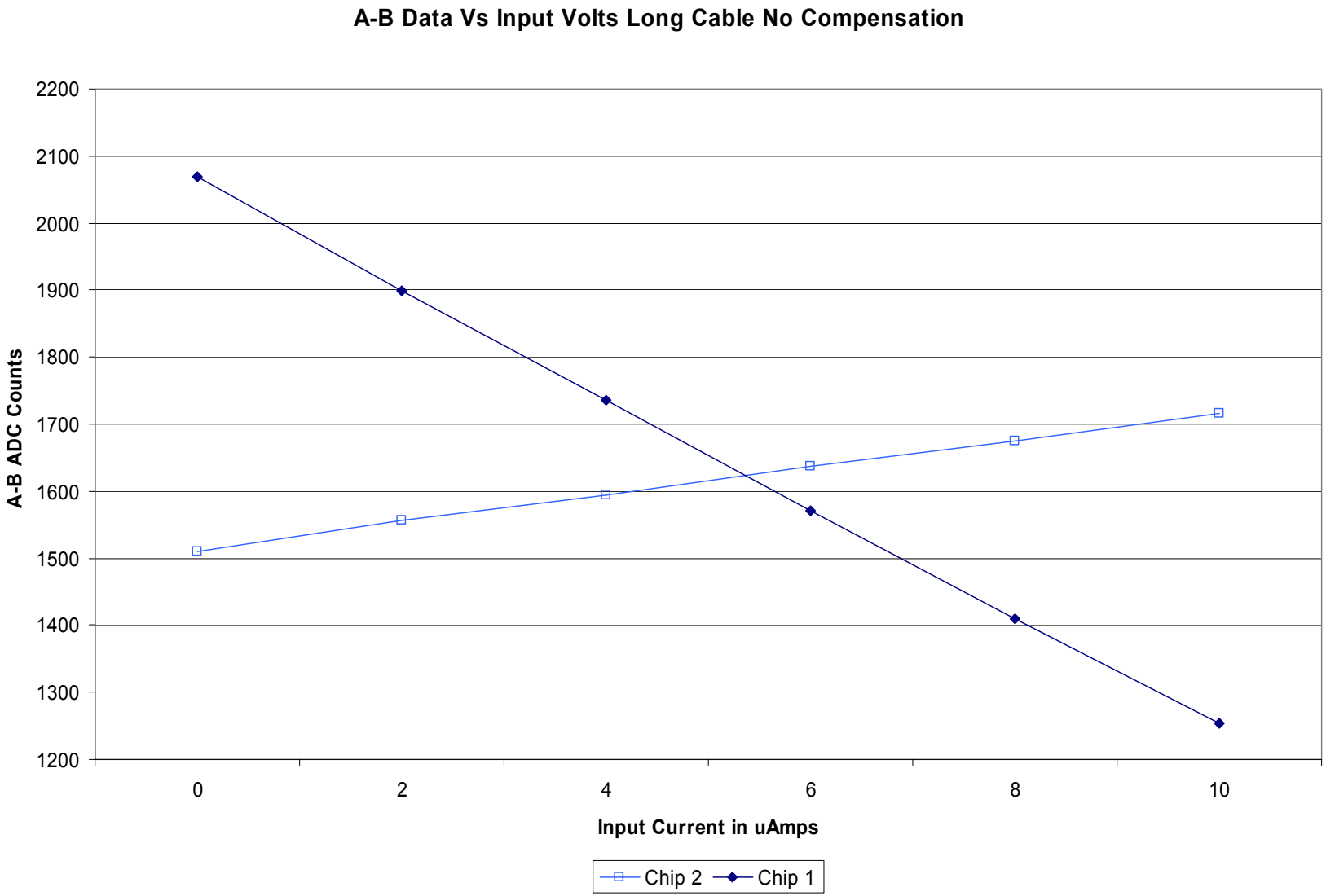
BLM Review


A and B Data vs Input Current Long Cable
60000
50000
40000
30000
20000
10000
0
ADC Counts
2
4
6
8
10
Input Current in uAmps
Channel B
Channel A

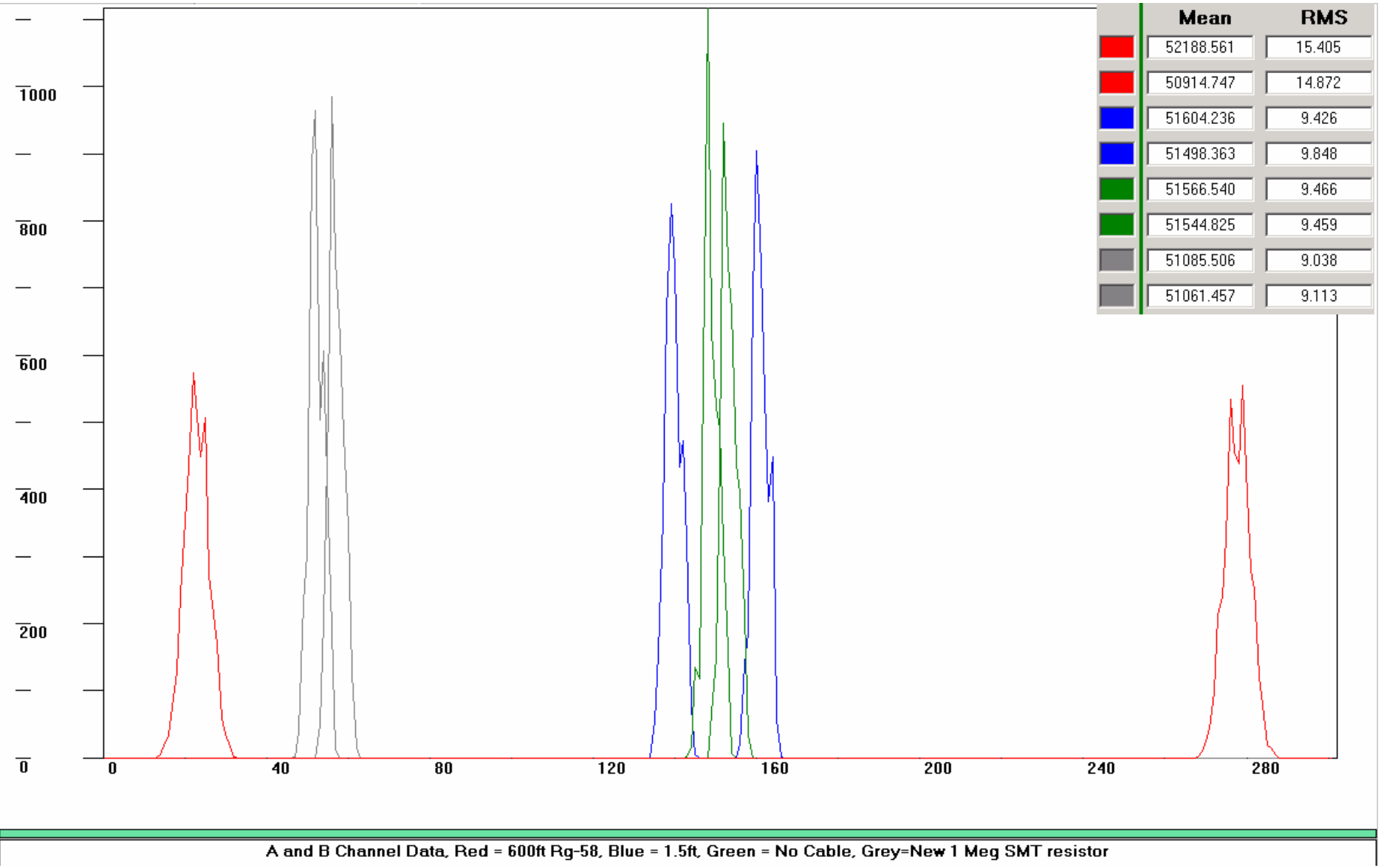
BLM Review


A-B data Differencs No Compensation
ADC counts
1750
1700
1650
1600
1550
1500
1450
1400
0
2
4
6
8
10
Input Current in uAmps

BLM Review


A-B Data Vs Input Volts Long Cable No Compensation
A-B ADC Counts
2200
2100
2000
1900
1800
1700
1600
1500
1400
1300
1200
0
2
4
6
8
10
Input Current in uAmps
Chip 2
Chip 1

BLM Review

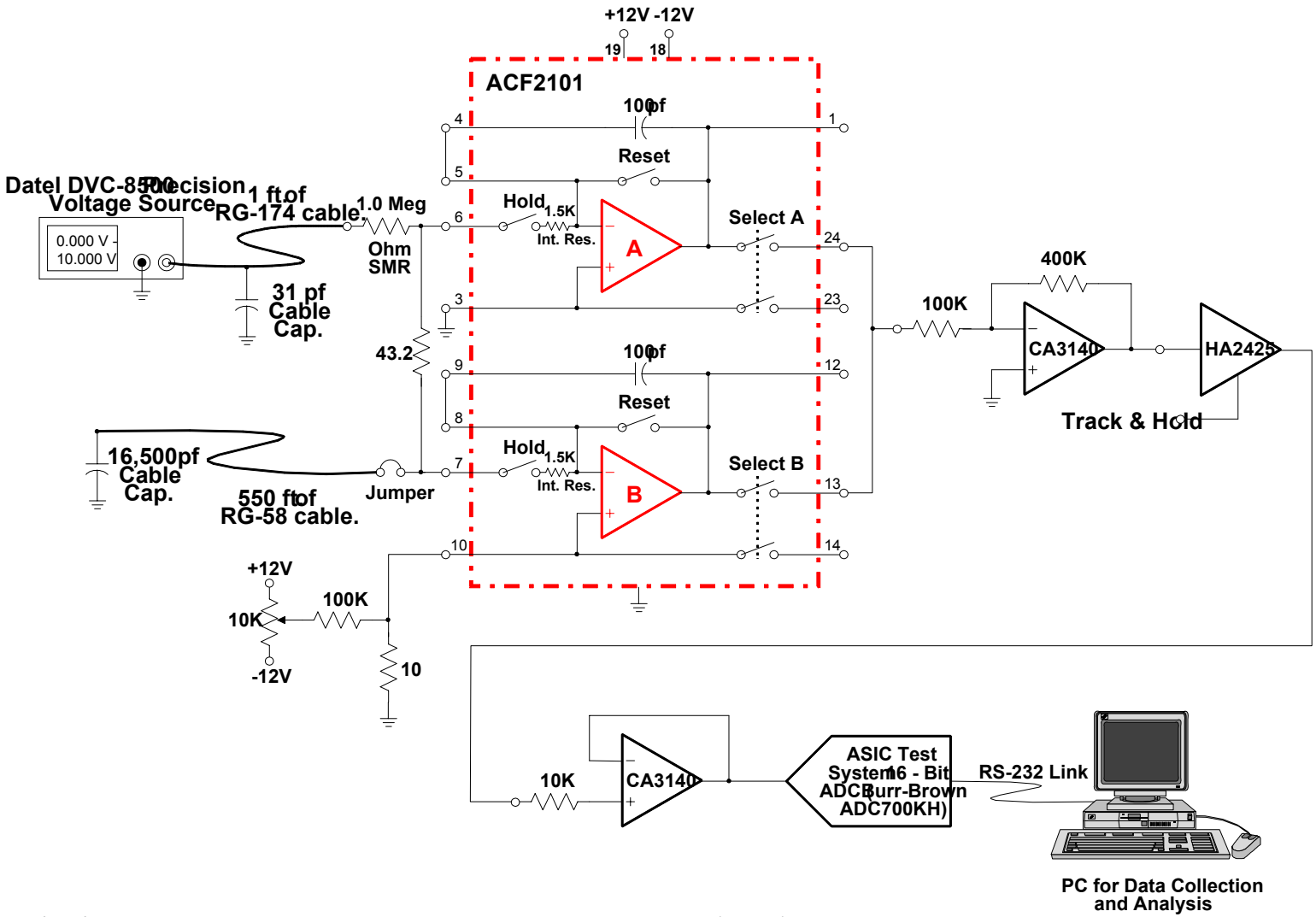

Mean
RMS
52188.561
15.405
50914.747
14.872
51604.236
9.426
51498.363
9.848
51566.540
9.466
51544.825
9.459
51085.506
9.038
51061.457
9.113
1000
800
600
400
200
0
0
40
80
120
160
200
240
280
A and B Channel Data, Red = 600ft Rg-58, Blue = 1.5ft, Green = No Cable, Grey=New 1 Meg SMT resistor

BLM Review

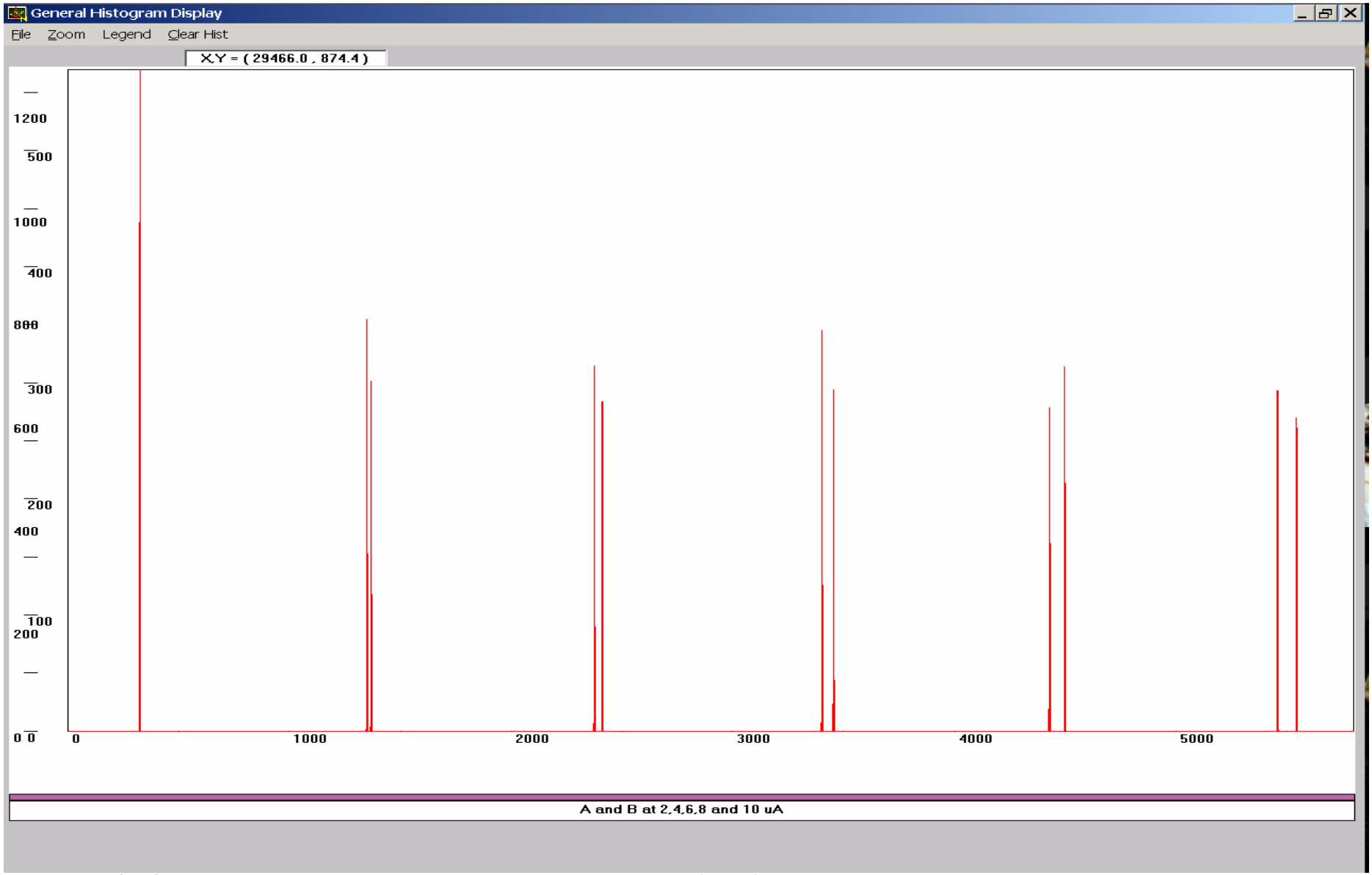
ACF2101 Test Setup Schematic

(Offset Null and Offset Adj. Configuration)

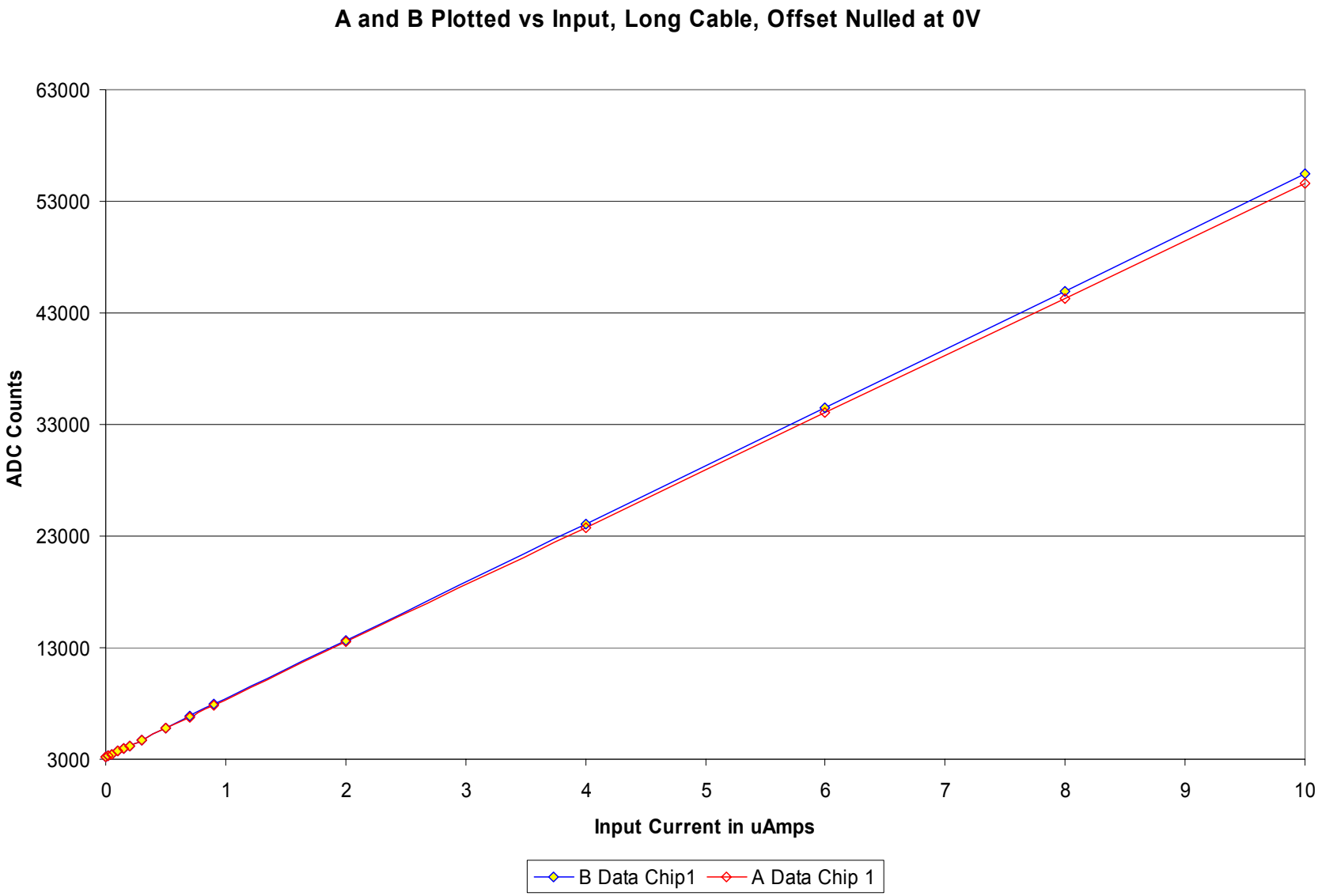
03/23/20



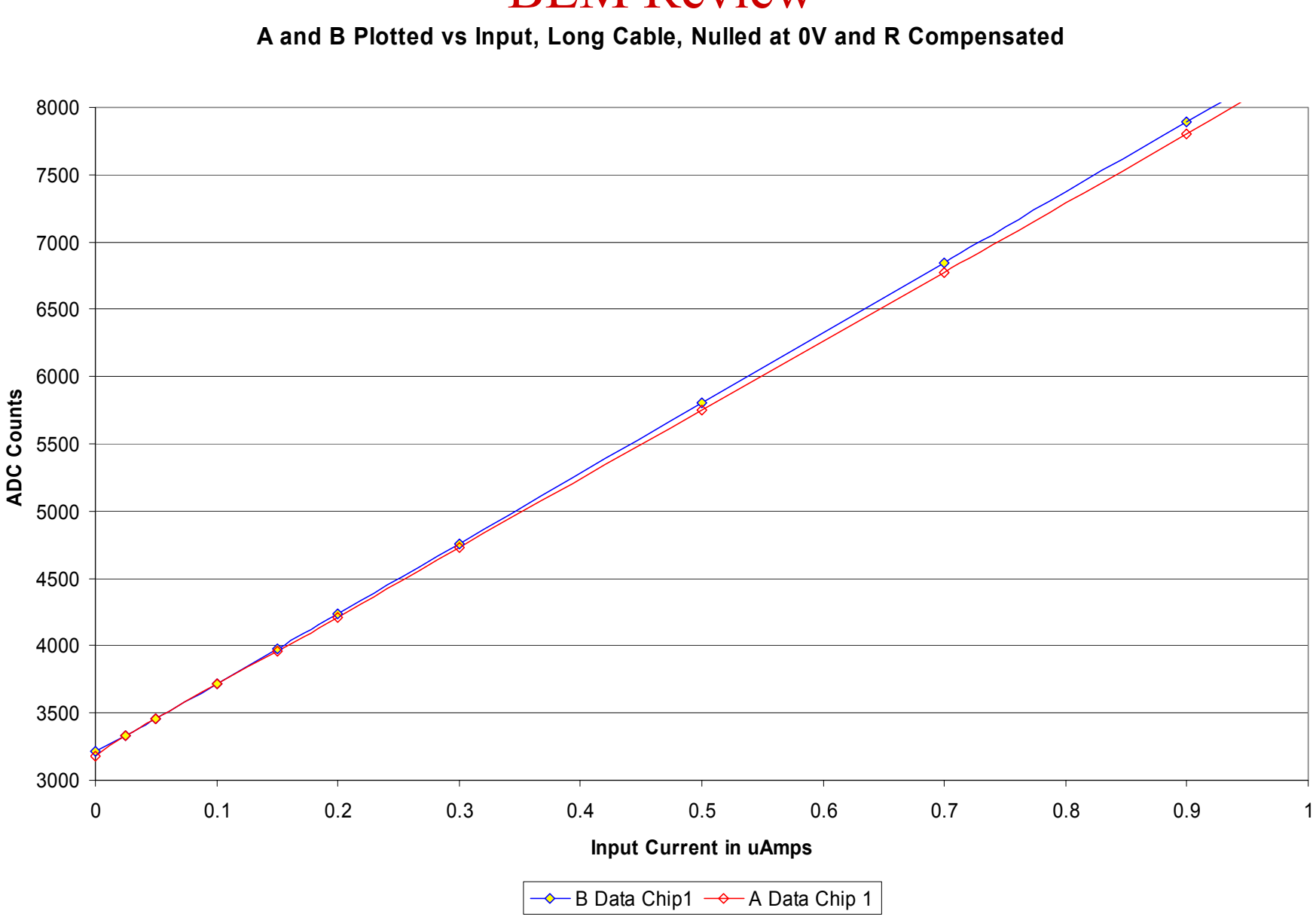
BLM Review


General Histogram Display
File Zoom Legend Clear Hist
X,Y = (29466.0 , 874.4)
1200
500
1000
400
800
300
600
200
400
100
200
0 0
0
1000
2000
3000
4000
5000
A and B at 2,4,6,8 and 10 uA

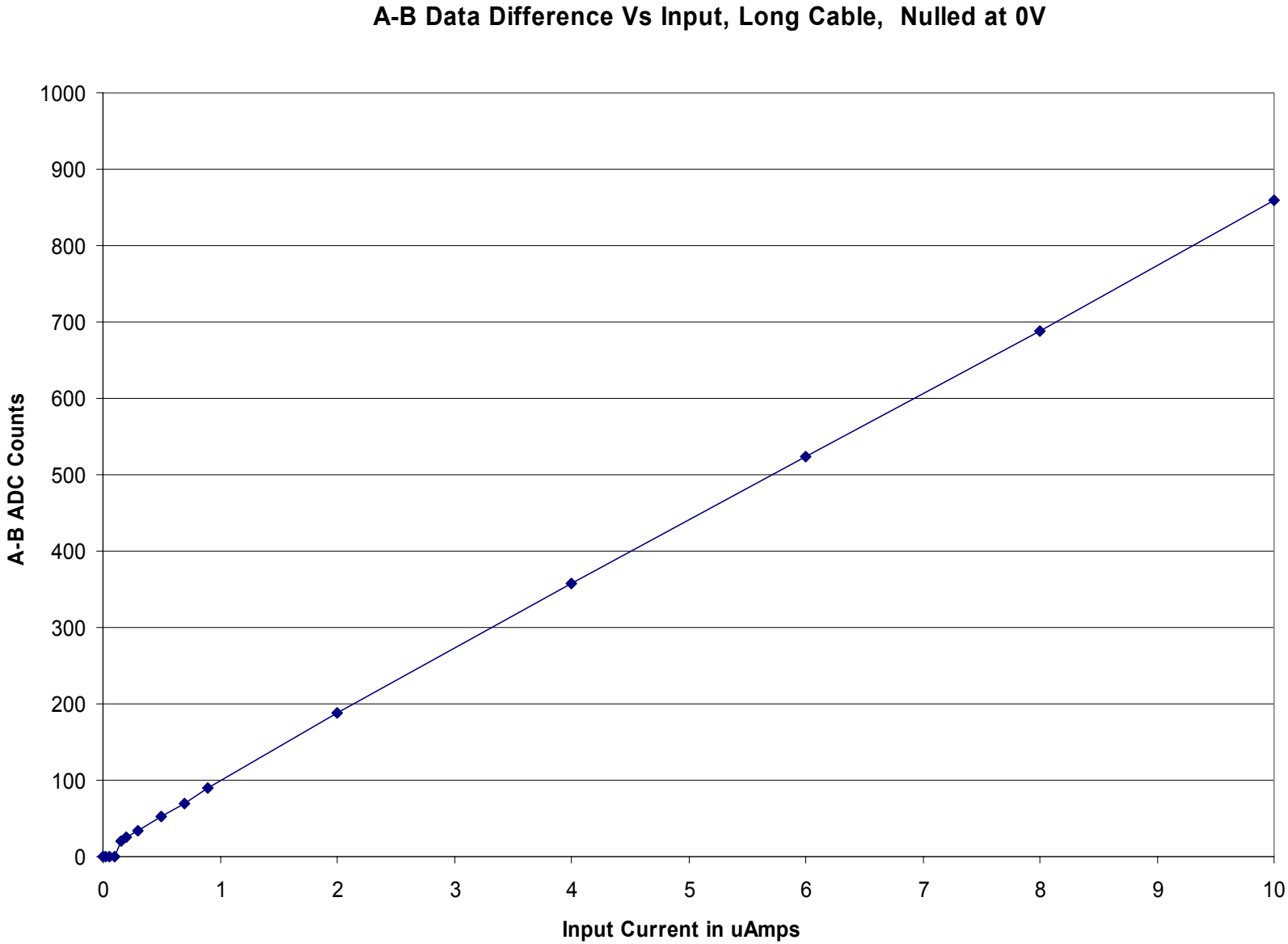
BLM Review


A and B Plotted vs Input, Long Cable, Offset Nulled at 0V
63000
53000
43000
33000
23000
13000
3000
ADC Counts
0
1
2
3
4
5
6
7
8
9
10
Input Current in uAmps
B Data Chip1
A Data Chip 1

BLM Review


A and B Plotted vs Input, Long Cable, Nulled at 0V and R Compensated
ADC Counts
8000
7500
7000
6500
6000
5500
5000
4500
4000
3500
3000
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Input Current in uAmps
B Data Chip1
A Data Chip 1

BLM Review

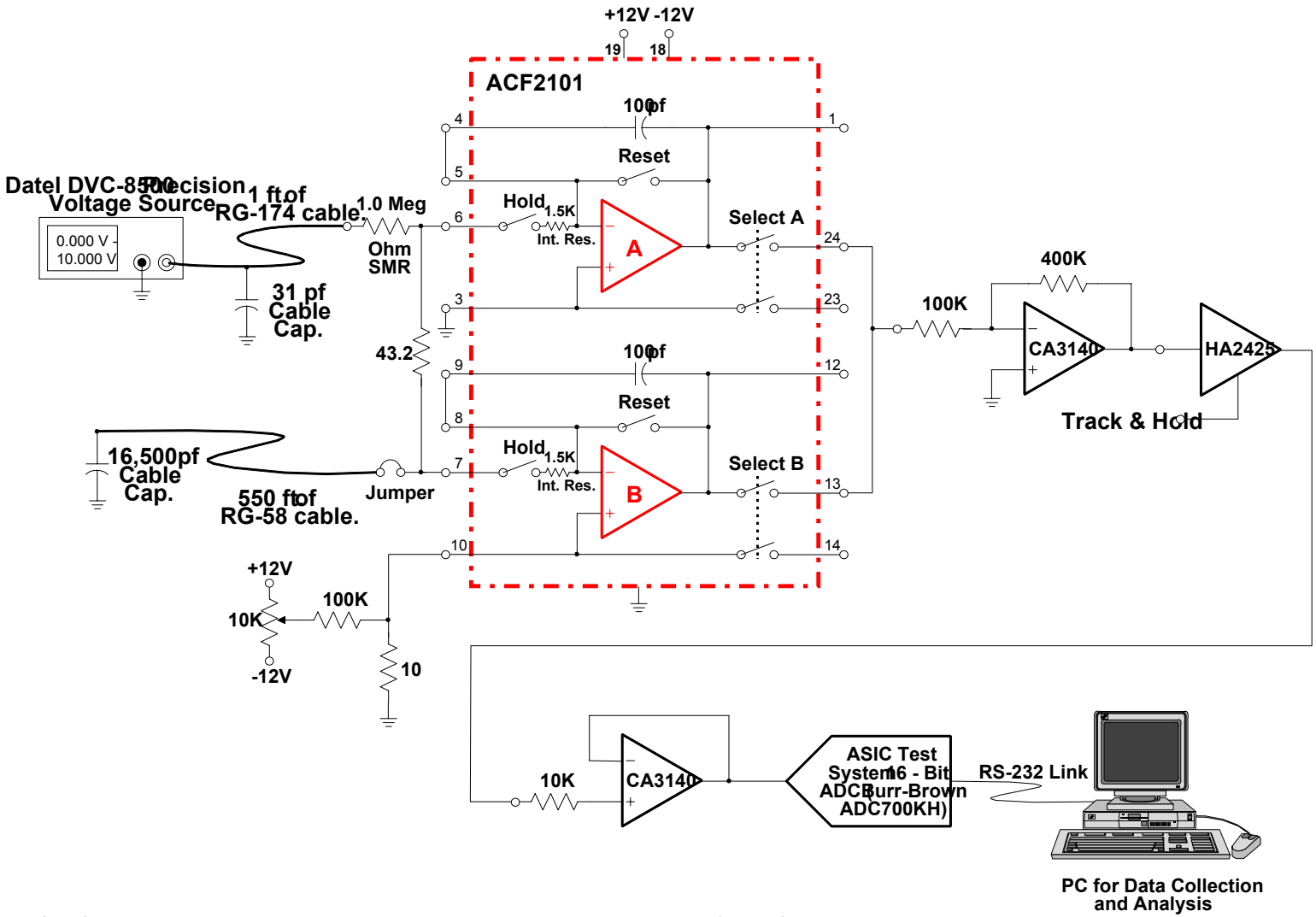

A-B Data Difference Vs Input, Long Cable, Nulled at 0V
A-B ADC Counts
1000
900
800
700
600
500
400
300
200
100
0
0
1
2
3
4
5
6
7
8
9
10
Input Current in uAmps

BLM Review

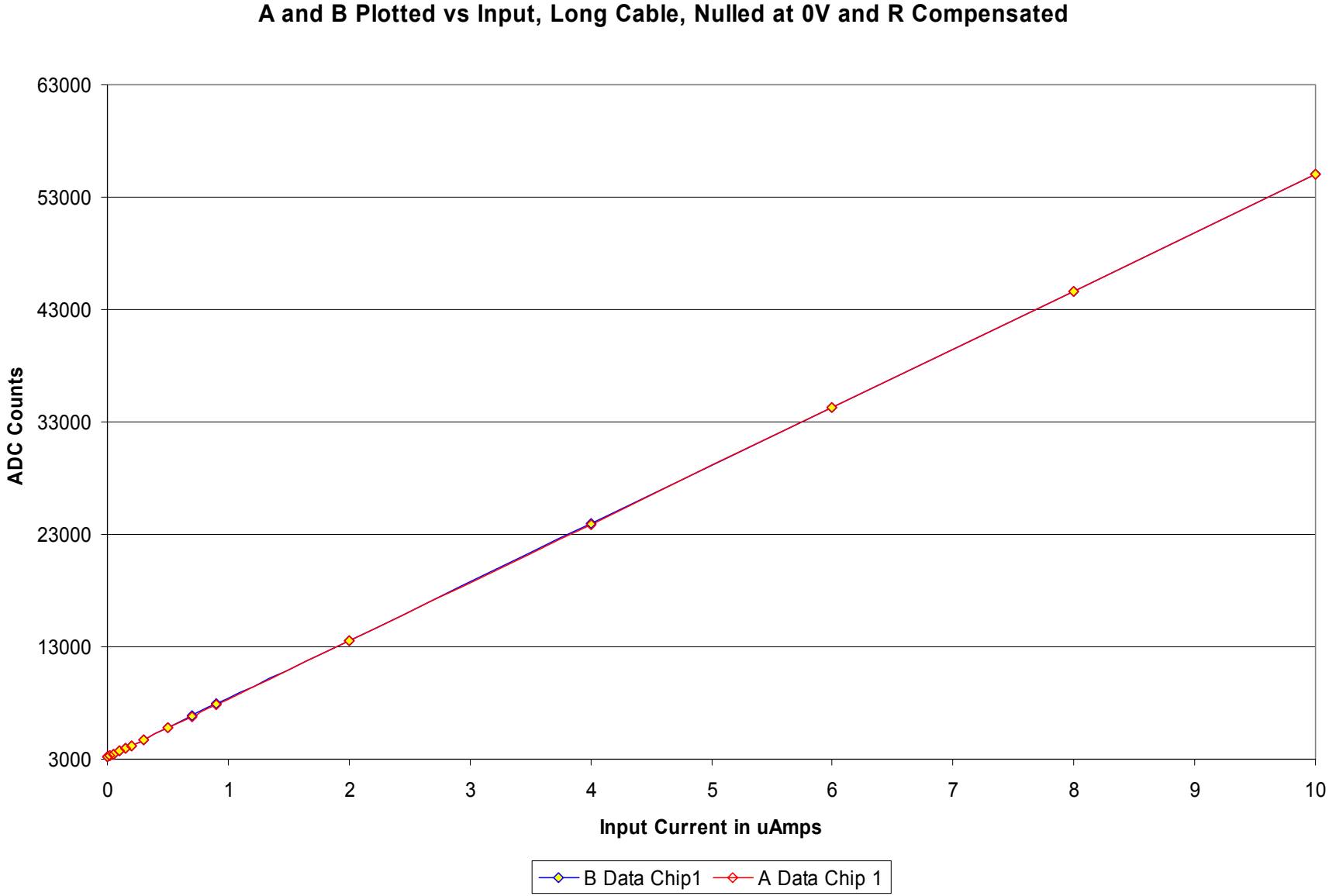
ACF2101 Test Setup Schematic

(Offset Null and Offset Adj. Configuration)

03/23/20



BLM Review


A and B Plotted vs Input, Long Cable, Nulled at 0V and R Compensated
63000
53000
43000
33000
23000
13000
3000
ADC Counts
0
1
2
3
4
5
6
7
8
9
10
Input Current in uAmps
B Data Chip1
A Data Chip 1