



Fermilab/BD/TEV  
Beams-doc-1202-v2  
June 15, 2004

## **Tevatron Beam Loss Monitor (BLM) Upgrade Hardware Prototype Testing**

**DRAFT**

Bill Haynes, Vince Pavlicek  
Fermilab, Computing Division, CEPA

### ***Abstract***

This document contains the results of the testing of a hardware prototype for the Beam Loss Monitor circuitry that is part of the Beam Position Monitor (BPM) upgrade data acquisition hardware. The External Device Bus (EDB) that connects the BLM sub rack to the BPM DA was prototyped and data transfer tests conducted.

## Overview

This note documents a prototype circuit that was used to understand the operation of the Beam Loss Monitor (BLM) interface to the Beam Position Monitor (BPM) system and to exercise that interface. The BLM circuitry is contained in a sub rack separate from the rest of the BPM hardware in a service building. The connection between the two is the External Device Bus (EDB), a simple byte address and byte data parallel interface with minimal control signals. The BPM data acquisition hardware will control and readout the BLM circuitry by reading and writing over the EDB. Figure 1 shows the functional block diagram of the prototype interface. The EDB is to the right. The prototype interface was implemented with a general purpose Programmable Mezzanine Connector (PMC) card made by BVM and containing a medium sized Field Programmable Gate Array (FPGA) device and several I/O connectors. The PMC card was plugged into a PMC carrier made by Valley Technologies and that was in a PCI slot in a desktop workstation. Simple FPGA firmware instantiated the interface lines as registers in the FPGA and diagnostic software was written to manipulate the register bits to perform the bus operations necessary to read and write across the EDB. The software could perform multiple operations sequentially allowing a measurement of the transfer speed of the prototype system. A spare BLM interface sub rack without BLM sensors was connected to the other end of the EDB. A standard 40 conductor ribbon cable, approximately 3 feet long was used for the EDB connection. This cable type is the same as in the current accelerator complex BLM EDB connection. The test setup is shown in Figure 2. Included are screen shots of the software display.

## Testing Results

Operation of the BLM circuitry was tested by writing into and reading back values in the accessible registers in the BLM electronics. The high voltage bias on the BLM sensors is controlled by the BLM electronics so the ability to adjust that voltage also confirmed correct EDB operation. Multiple transfers of data from the BLM sub rack to the prototype interface showed a transfer rate of over 150 Kbytes per second. Given a required update rate of several seconds and a data packet size of less than 50 bytes, the prototype interface would easily meet the BLM readout requirements. A more sophisticated firmware design in the FPGA could pipeline transfers to the BPM Data Acquisition hardware if required in the final upgrade implementation.

## Beam Loss Monitor Interface

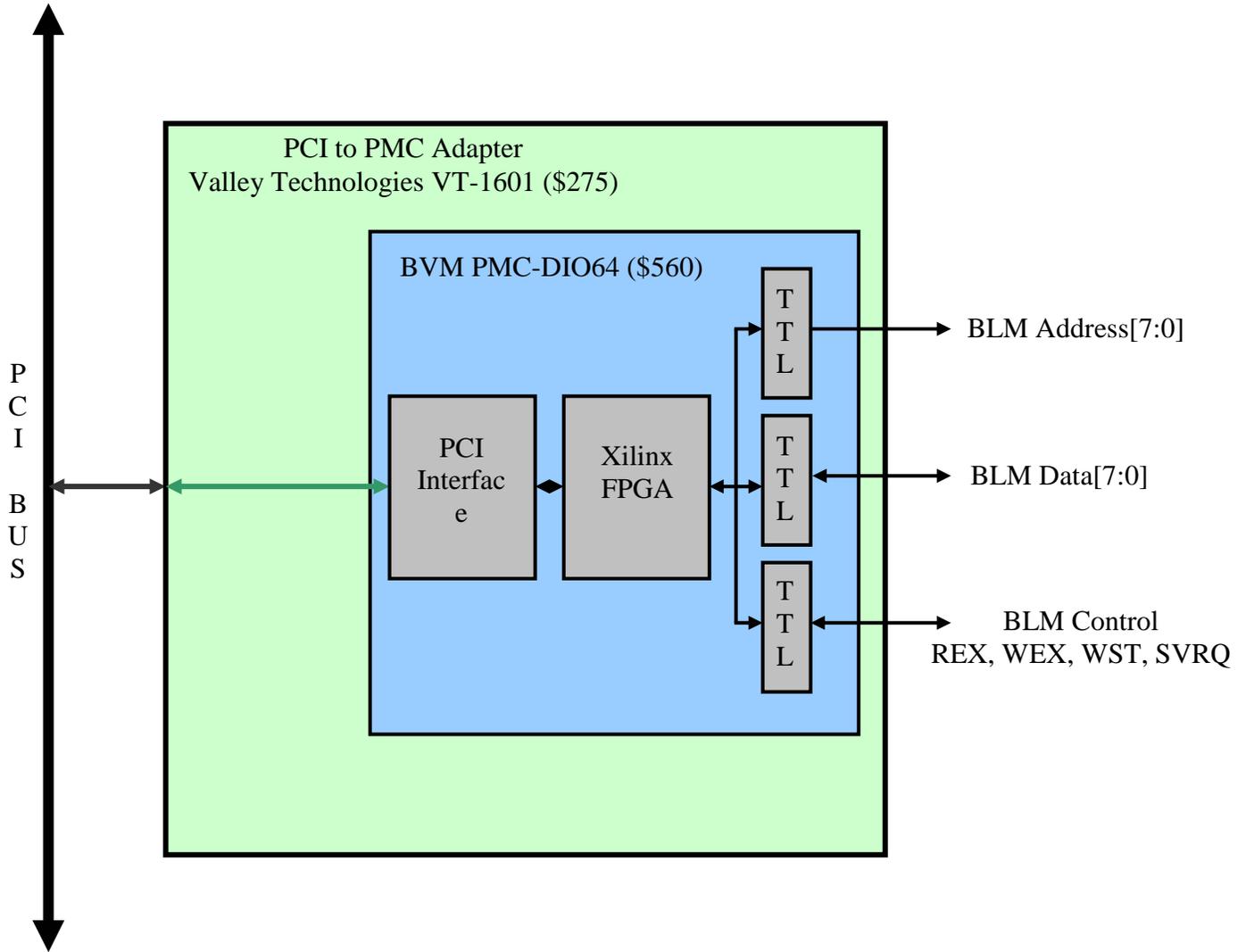


Figure 1 Prototype Interface

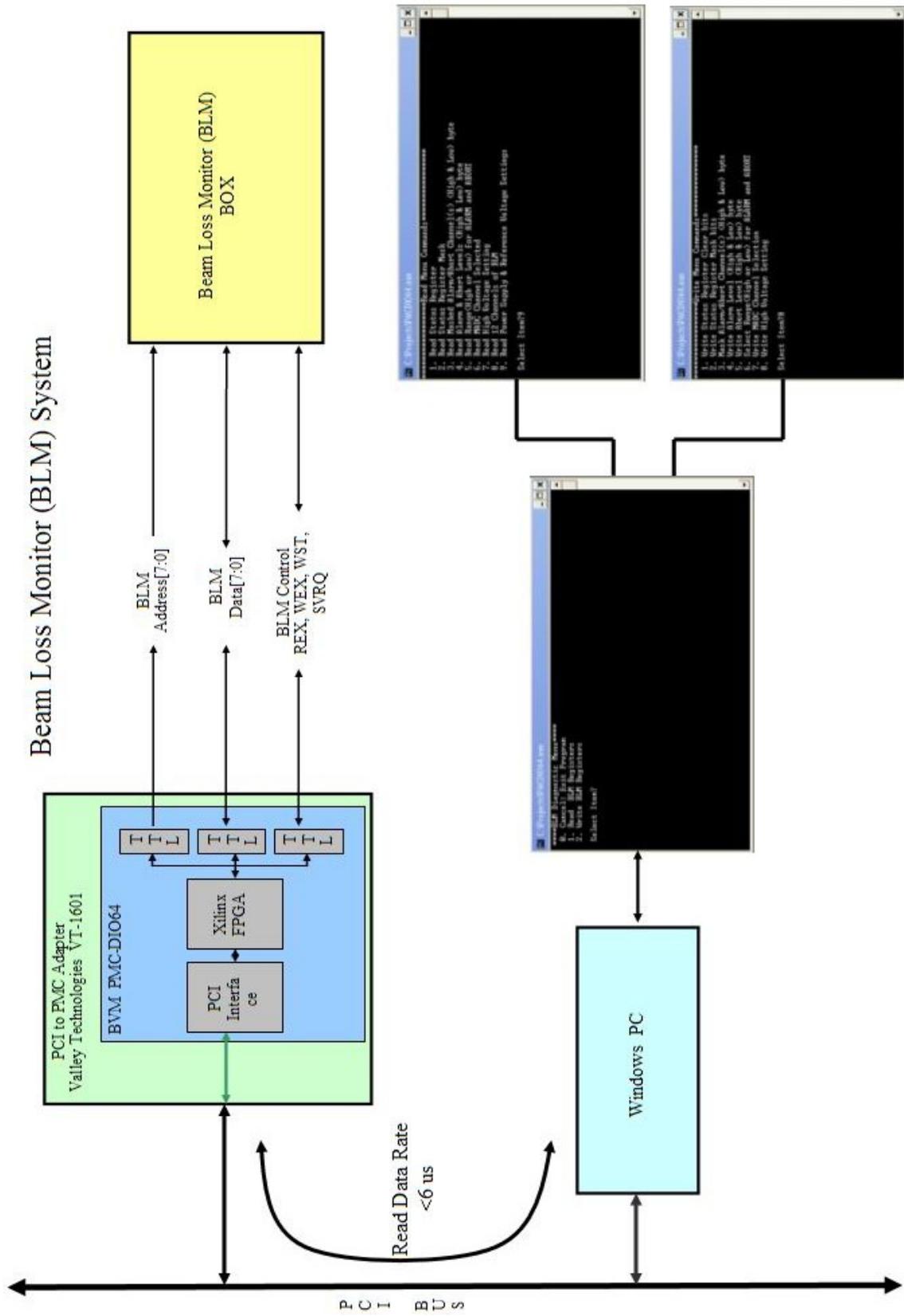


Figure 2 Test Set-up

