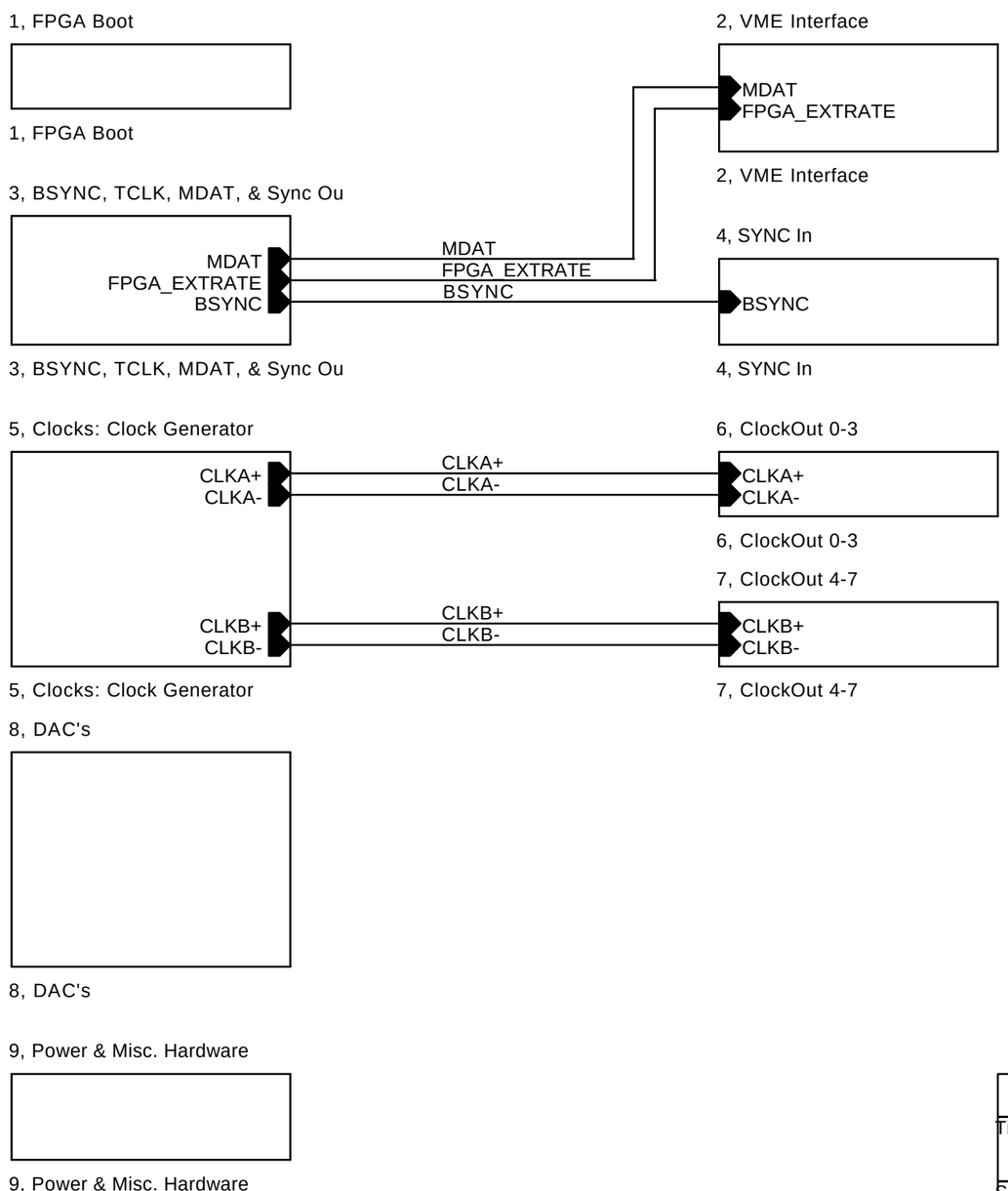
Timing Fanout Card



Title: TFC Block Diagram		
Size: A	Document Number: <Doc>	Rev: 0.2
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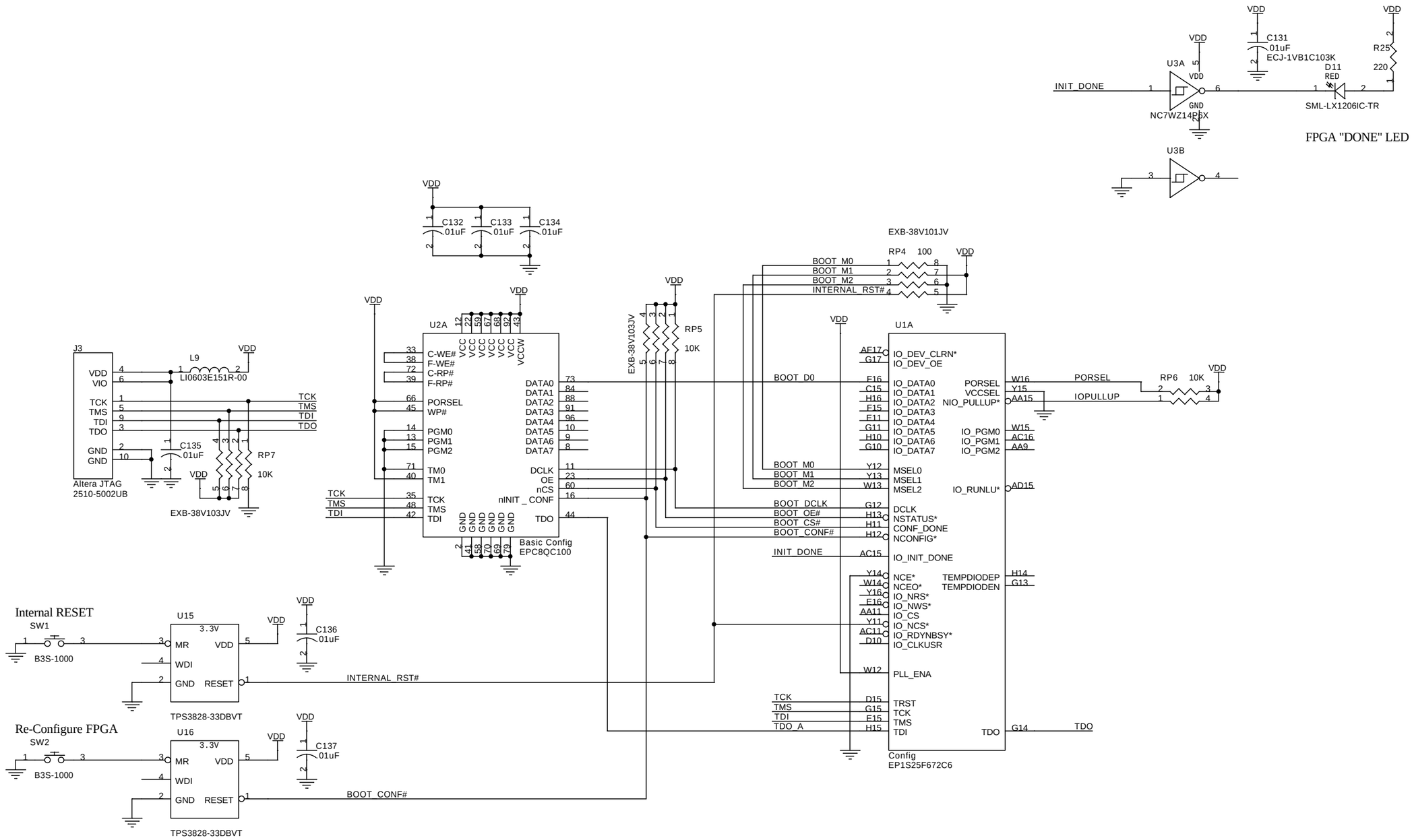

Title
Stratix FPGA Boot

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	<Doc>	0.2

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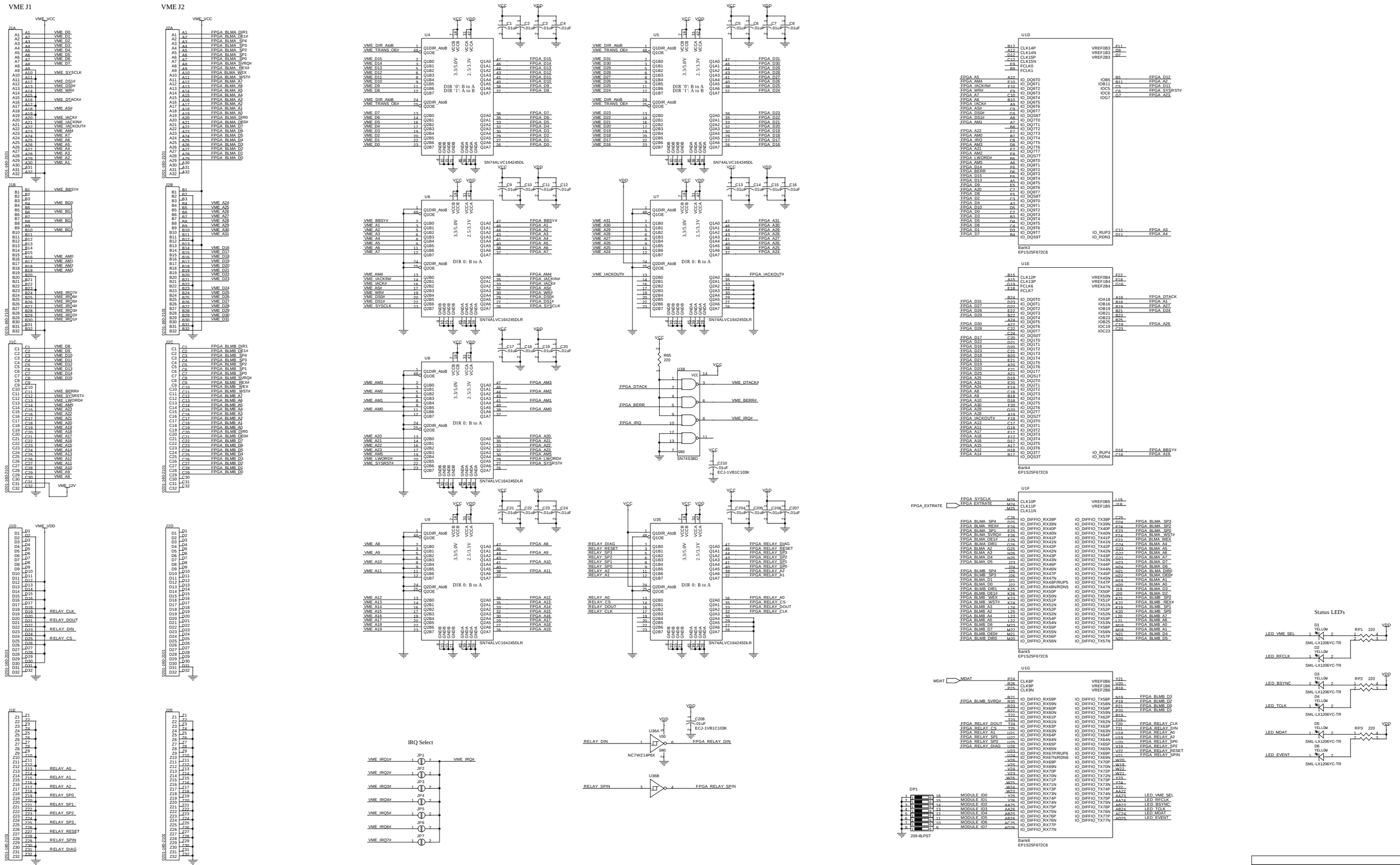

Title
VME Interface

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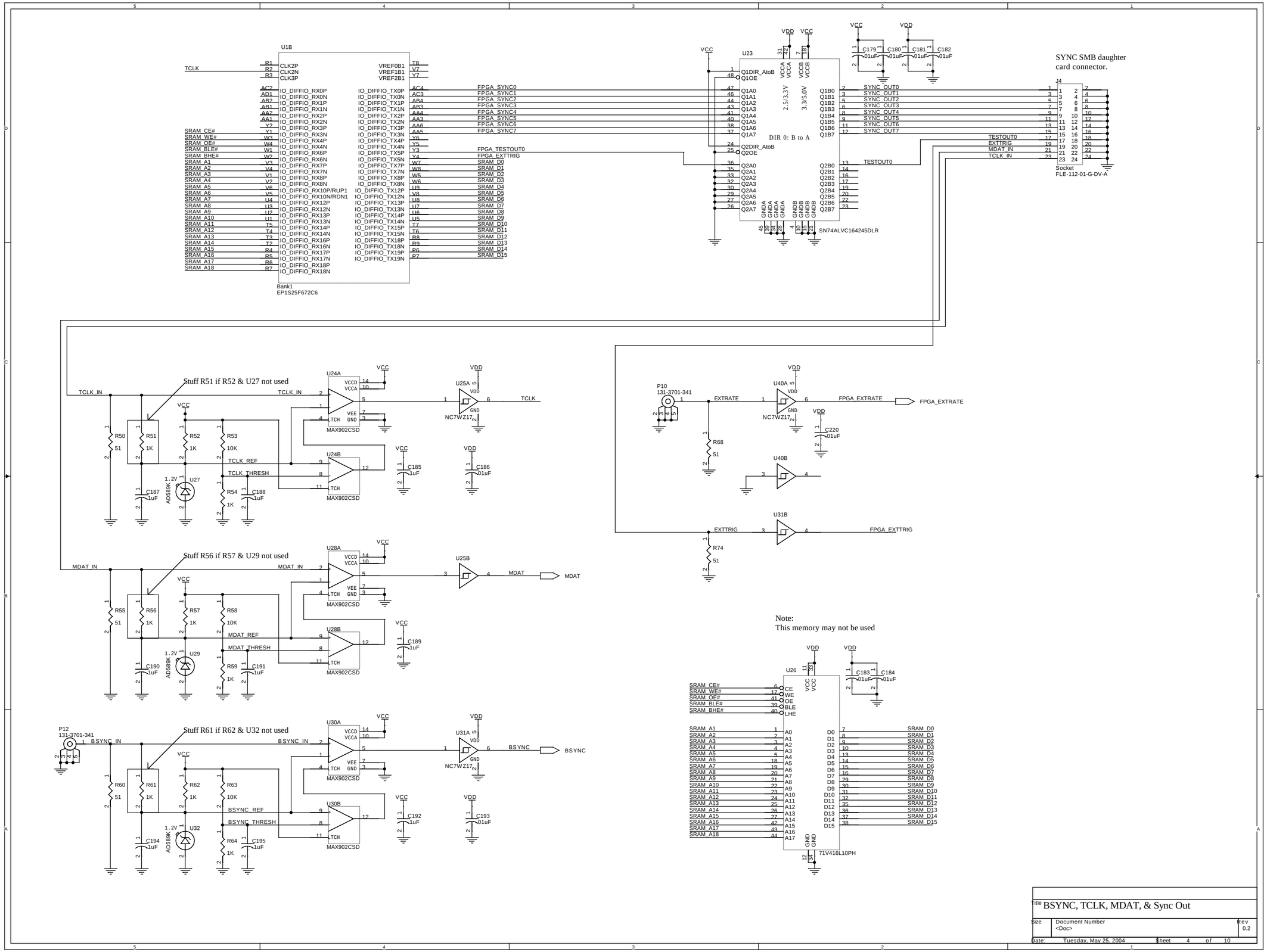
U1B
Bank1
EP1S25F672C6
U23
SN74ALVC164245DLR
DIR 0: B to A
2.5/3.3V
3.3/5.0V
SYNC SMB daughter card connector.
J4
Socket
FLE-112-01-G-DV-A
Stuff R51 if R52 & U27 not used
Stuff R56 if R57 & U29 not used
Stuff R61 if R62 & U32 not used
MAX902CSD
NC7WZ17
AD589K
P10
131-3701-341
P12
131-3701-341
U40A
U40B
U31B
U26
71V416L10PH
Note:
This memory may not be used
Title BSYNC, TCLK, MDAT, & Sync Out
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<Doc>
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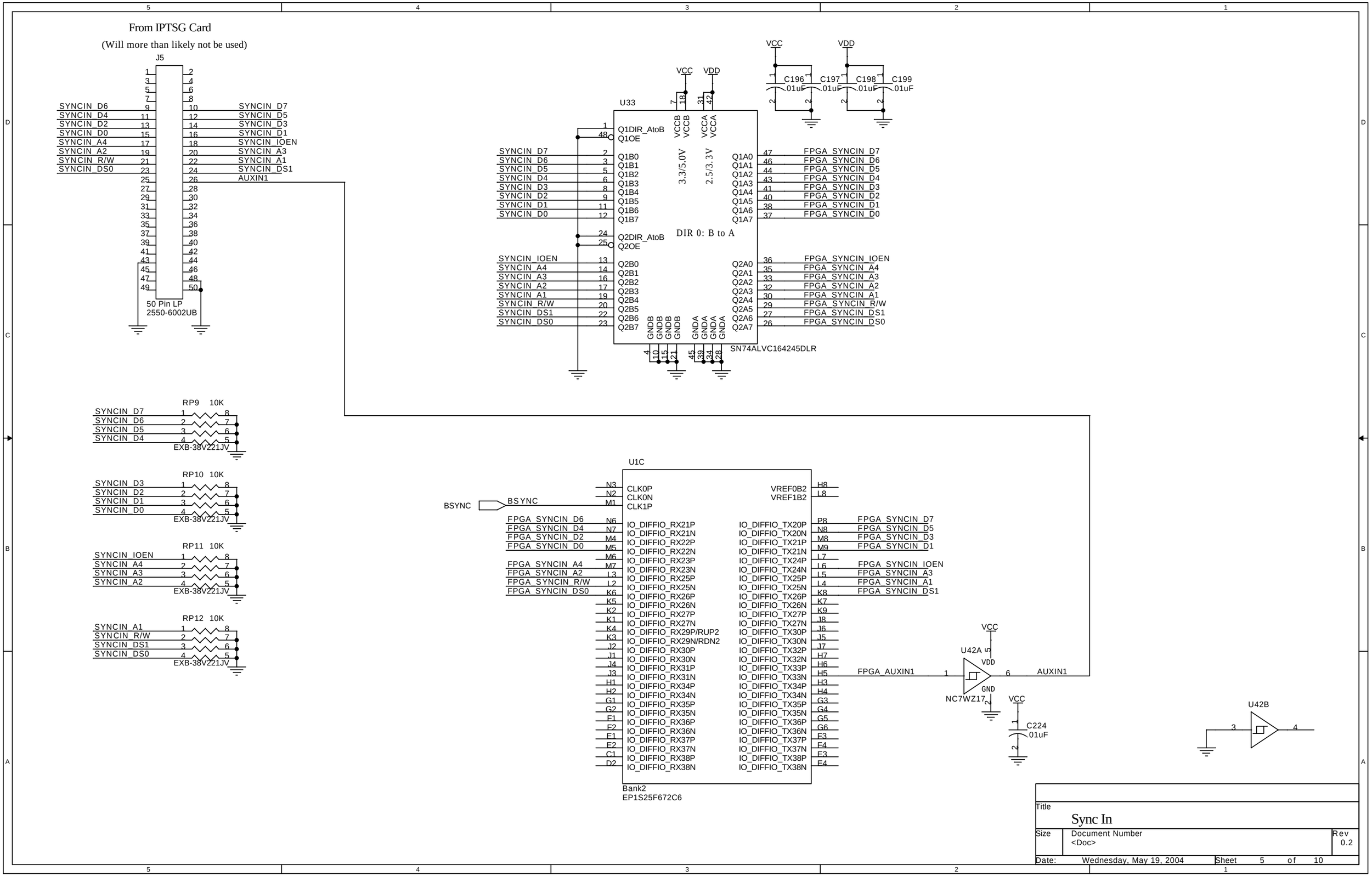
From IPTSG Card
(Will more than likely not be used)
J5
50 Pin LP
2550-6002UB
SYNCIN_D6
SYNCIN_D4
SYNCIN_D2
SYNCIN_D0
SYNCIN_A4
SYNCIN_A2
SYNCIN_R/W
SYNCIN_DS0
SYNCIN_D7
SYNCIN_D5
SYNCIN_D3
SYNCIN_D1
SYNCIN_IOEN
SYNCIN_A3
SYNCIN_A1
SYNCIN_DS1
AUXIN1
U33
VCC
VDD
C196 .01uF
C197 .01uF
C198 .01uF
C199 .01uF
Q1DIR_AtoB
Q1OE
Q2DIR_AtoB
Q2OE
VCCB
VCCA
3.3/5.0V
2.5/3.3V
DIR 0: B to A
GNDB
GNDA
SN74ALVC164245DLR
FPGA_SYNCIN_D7
FPGA_SYNCIN_D6
FPGA_SYNCIN_D5
FPGA_SYNCIN_D4
FPGA_SYNCIN_D3
FPGA_SYNCIN_D2
FPGA_SYNCIN_D1
FPGA_SYNCIN_D0
FPGA_SYNCIN_IOEN
FPGA_SYNCIN_A4
FPGA_SYNCIN_A3
FPGA_SYNCIN_A2
FPGA_SYNCIN_A1
FPGA_SYNCIN_R/W
FPGA_SYNCIN_DS1
FPGA_SYNCIN_DS0
RP9 10K
RP10 10K
RP11 10K
RP12 10K
EXB-38V221JV
U1C
BSYNC
CLK0P
CLK0N
CLK1P
VREF0B2
VREF1B2
FPGA_SYNCIN_D6
FPGA_SYNCIN_D4
FPGA_SYNCIN_D2
FPGA_SYNCIN_D0
FPGA_SYNCIN_A4
FPGA_SYNCIN_A2
FPGA_SYNCIN_R/W
FPGA_SYNCIN_DS0
IO_DIFFIO_RX21P
IO_DIFFIO_RX21N
IO_DIFFIO_RX22P
IO_DIFFIO_RX22N
IO_DIFFIO_RX23P
IO_DIFFIO_RX23N
IO_DIFFIO_RX25P
IO_DIFFIO_RX25N
IO_DIFFIO_RX26P
IO_DIFFIO_RX26N
IO_DIFFIO_RX27P
IO_DIFFIO_RX27N
IO_DIFFIO_RX29P/RUP2
IO_DIFFIO_RX29N/RDN2
IO_DIFFIO_RX30P
IO_DIFFIO_RX30N
IO_DIFFIO_RX31P
IO_DIFFIO_RX31N
IO_DIFFIO_RX34P
IO_DIFFIO_RX34N
IO_DIFFIO_RX35P
IO_DIFFIO_RX35N
IO_DIFFIO_RX36P
IO_DIFFIO_RX36N
IO_DIFFIO_RX37P
IO_DIFFIO_RX37N
IO_DIFFIO_RX38P
IO_DIFFIO_RX38N
IO_DIFFIO_TX20P
IO_DIFFIO_TX20N
IO_DIFFIO_TX21P
IO_DIFFIO_TX21N
IO_DIFFIO_TX24P
IO_DIFFIO_TX24N
IO_DIFFIO_TX25P
IO_DIFFIO_TX25N
IO_DIFFIO_TX26P
IO_DIFFIO_TX26N
IO_DIFFIO_TX27P
IO_DIFFIO_TX27N
IO_DIFFIO_TX30P
IO_DIFFIO_TX30N
IO_DIFFIO_TX32P
IO_DIFFIO_TX32N
IO_DIFFIO_TX33P
IO_DIFFIO_TX33N
IO_DIFFIO_TX34P
IO_DIFFIO_TX34N
IO_DIFFIO_TX35P
IO_DIFFIO_TX35N
IO_DIFFIO_TX36P
IO_DIFFIO_TX36N
IO_DIFFIO_TX37P
IO_DIFFIO_TX37N
IO_DIFFIO_TX38P
IO_DIFFIO_TX38N
FPGA_SYNCIN_D7
FPGA_SYNCIN_D5
FPGA_SYNCIN_D3
FPGA_SYNCIN_D1
FPGA_SYNCIN_IOEN
FPGA_SYNCIN_A3
FPGA_SYNCIN_A1
FPGA_SYNCIN_DS1
Bank2
EP1S25F672C6
FPGA_AUXIN1
U42A
NC7WZ17
VDD
GND
AUXIN1
C224 .01uF
U42B
Title
Sync In
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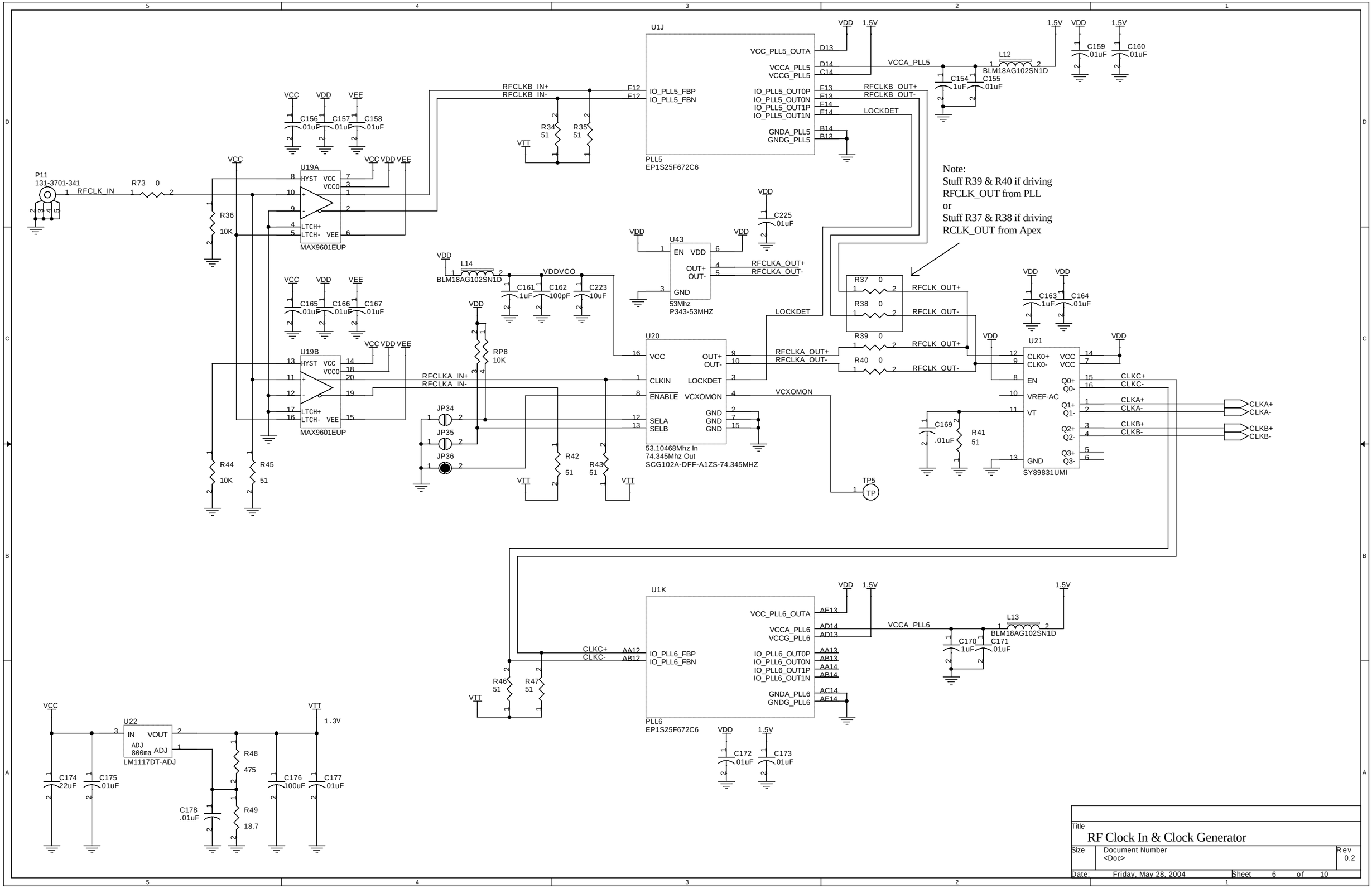

Title
RF Clock In & Clock Generator

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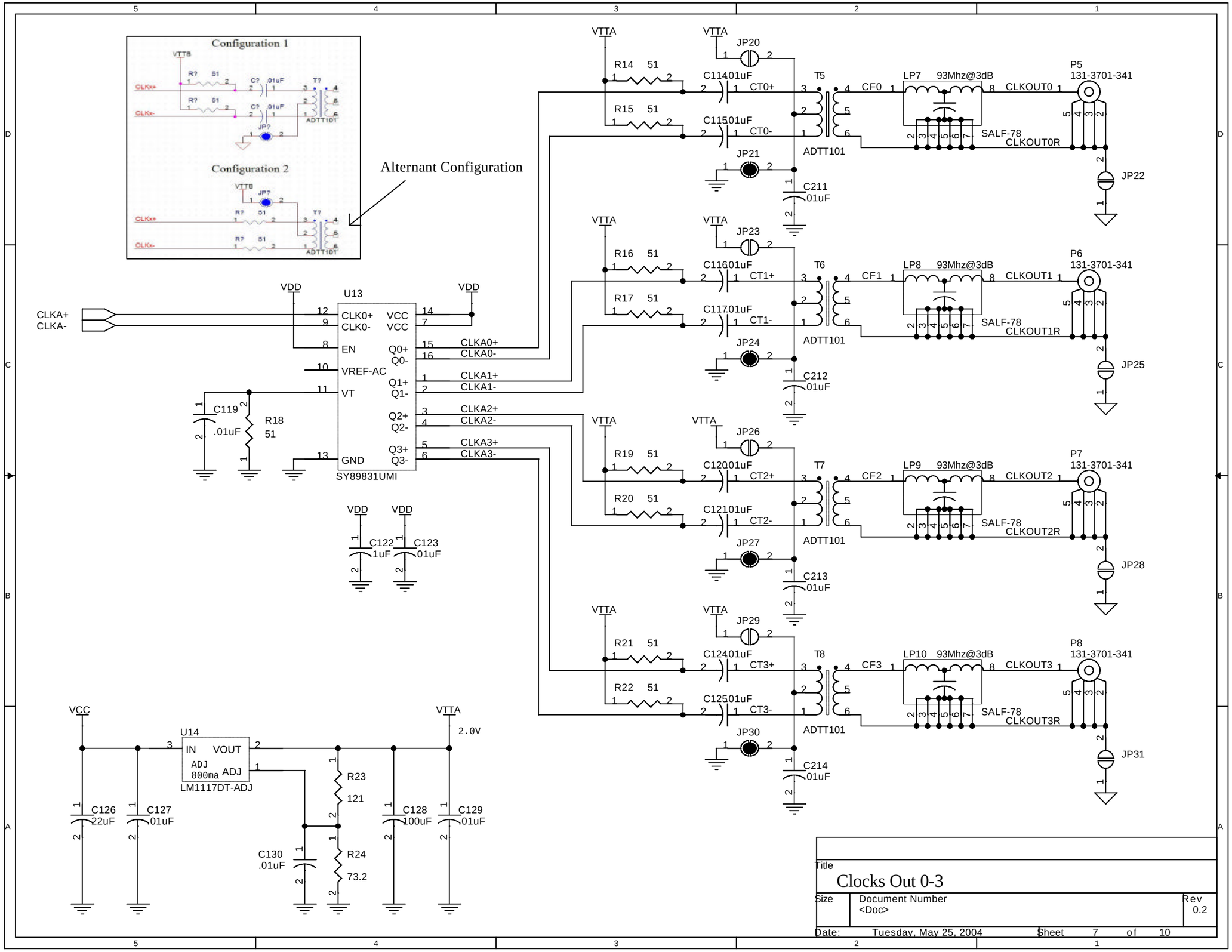
Configuration 1
Configuration 2
Alternant Configuration
U13
SY89831UMI
CLKA+
CLKA-
VDD
VTTA
VCC
U14
LM1117DT-ADJ
2.0V
T5
T6
T7
T8
ADTT101
LP7 93Mhz@3dB
LP8 93Mhz@3dB
LP9 93Mhz@3dB
LP10 93Mhz@3dB
SALF-78
P5 131-3701-341
P6 131-3701-341
P7 131-3701-341
P8 131-3701-341
CLKOUT0
CLKOUT0R
CLKOUT1
CLKOUT1R
CLKOUT2
CLKOUT2R
CLKOUT3
CLKOUT3R
Title
Clocks Out 0-3
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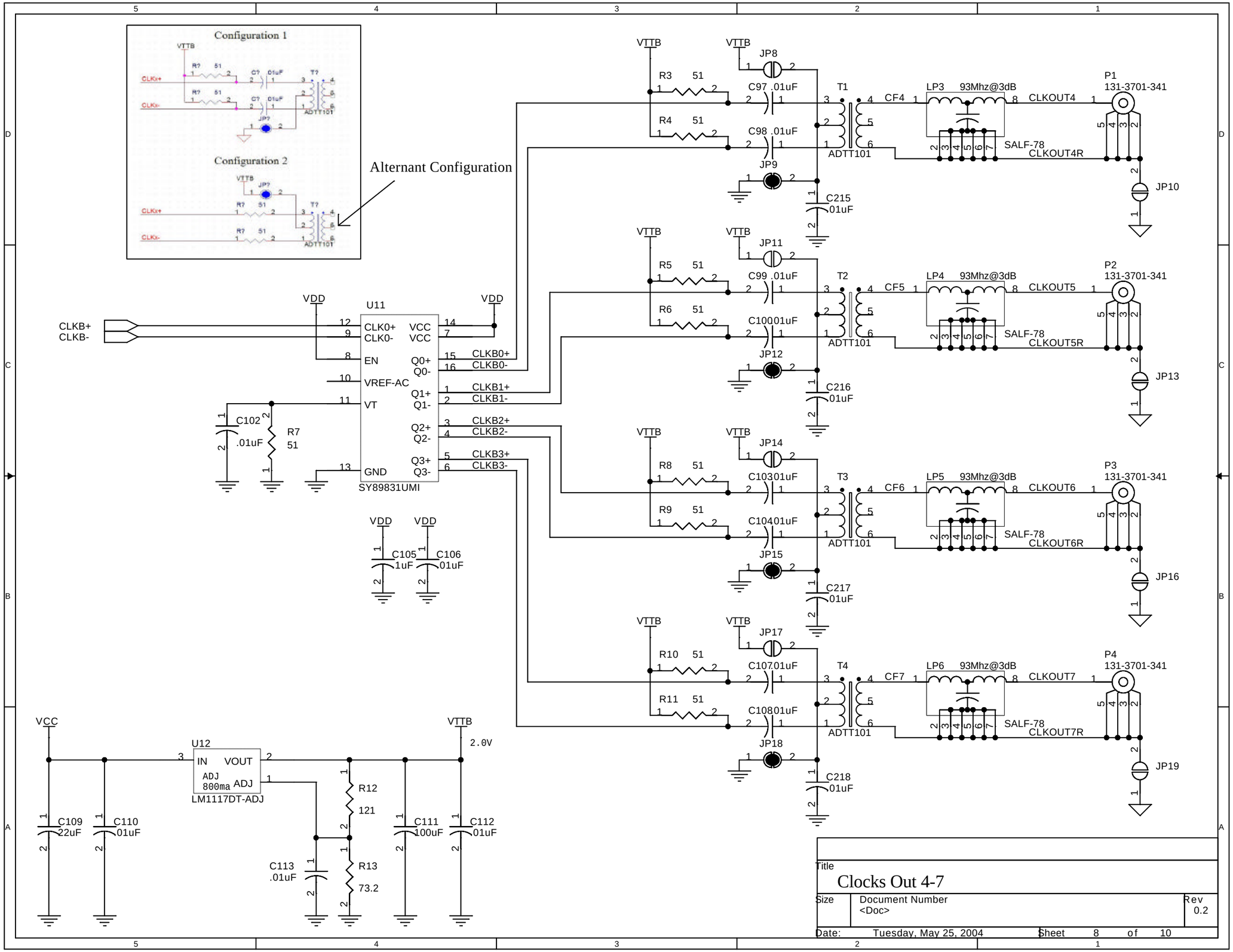
Configuration 1
Configuration 2
Alternant Configuration
U11
SY89831UMI
CLKB+
CLKB-
CLK0+
CLK0-
EN
VREF-AC
VT
GND
VCC
Q0+
Q0-
Q1+
Q1-
Q2+
Q2-
Q3+
Q3-
CLKB0+
CLKB0-
CLKB1+
CLKB1-
CLKB2+
CLKB2-
CLKB3+
CLKB3-
C102 .01uF
R7 51
C105 1uF
C106 01uF
U12
LM1117DT-ADJ
IN
VOUT
ADJ
800ma
2.0V
R12 121
R13 73.2
C113 .01uF
C109 22uF
C110 01uF
C111 100uF
C112 01uF
T1
T2
T3
T4
ADTT101
CF4
CF5
CF6
CF7
LP3 93Mhz@3dB
LP4 93Mhz@3dB
LP5 93Mhz@3dB
LP6 93Mhz@3dB
SALF-78
CLKOUT4
CLKOUT4R
CLKOUT5
CLKOUT5R
CLKOUT6
CLKOUT6R
CLKOUT7
CLKOUT7R
P1 131-3701-341
P2 131-3701-341
P3 131-3701-341
P4 131-3701-341
JP10
JP13
JP16
JP19
C215 01uF
C216 01uF
C217 01uF
C218 01uF
Title
Clocks Out 4-7
Size
Document Number
<Doc>
Rev
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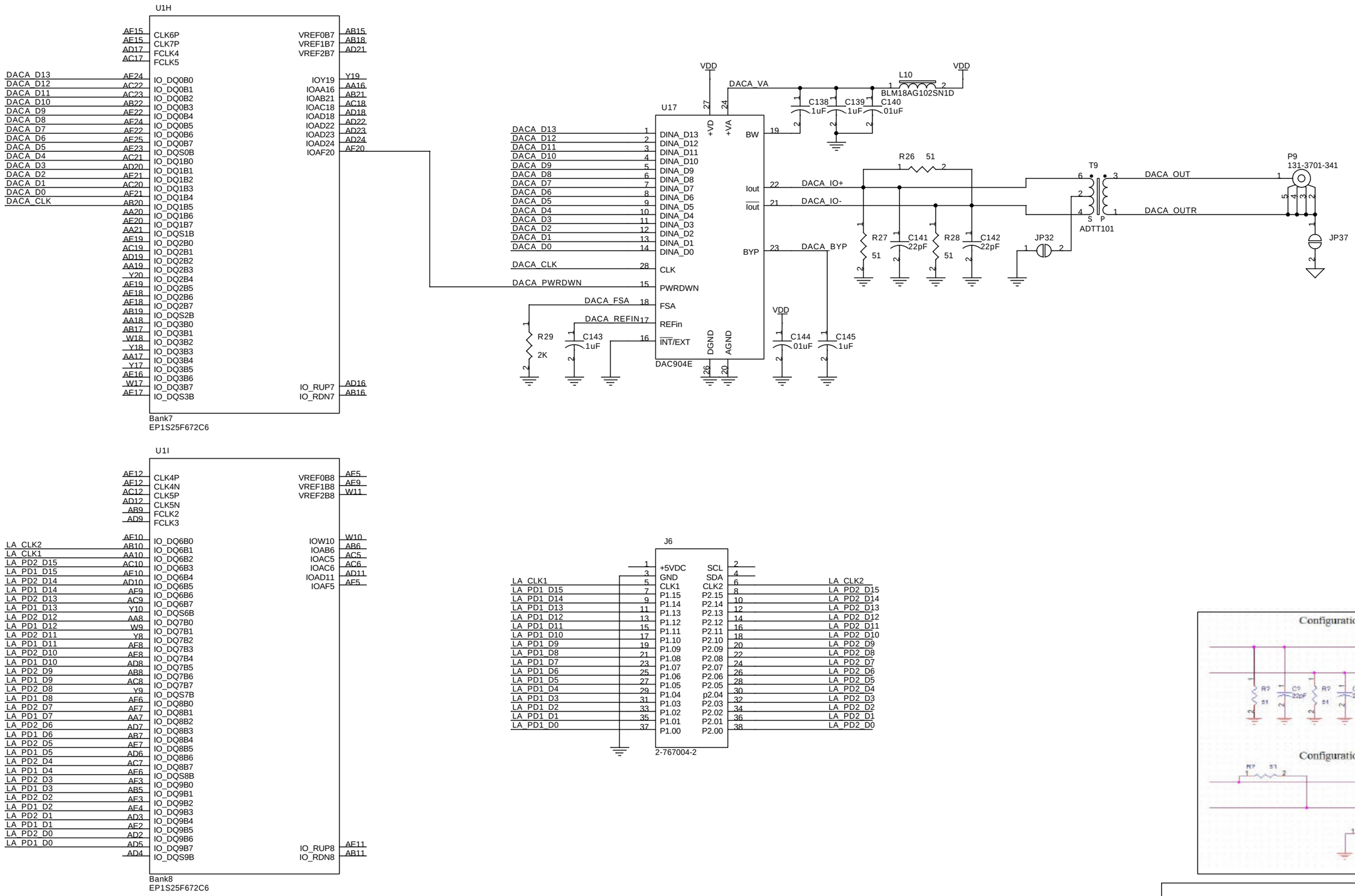

Title
Digital to Analog Outputs

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	<Doc>	0.2

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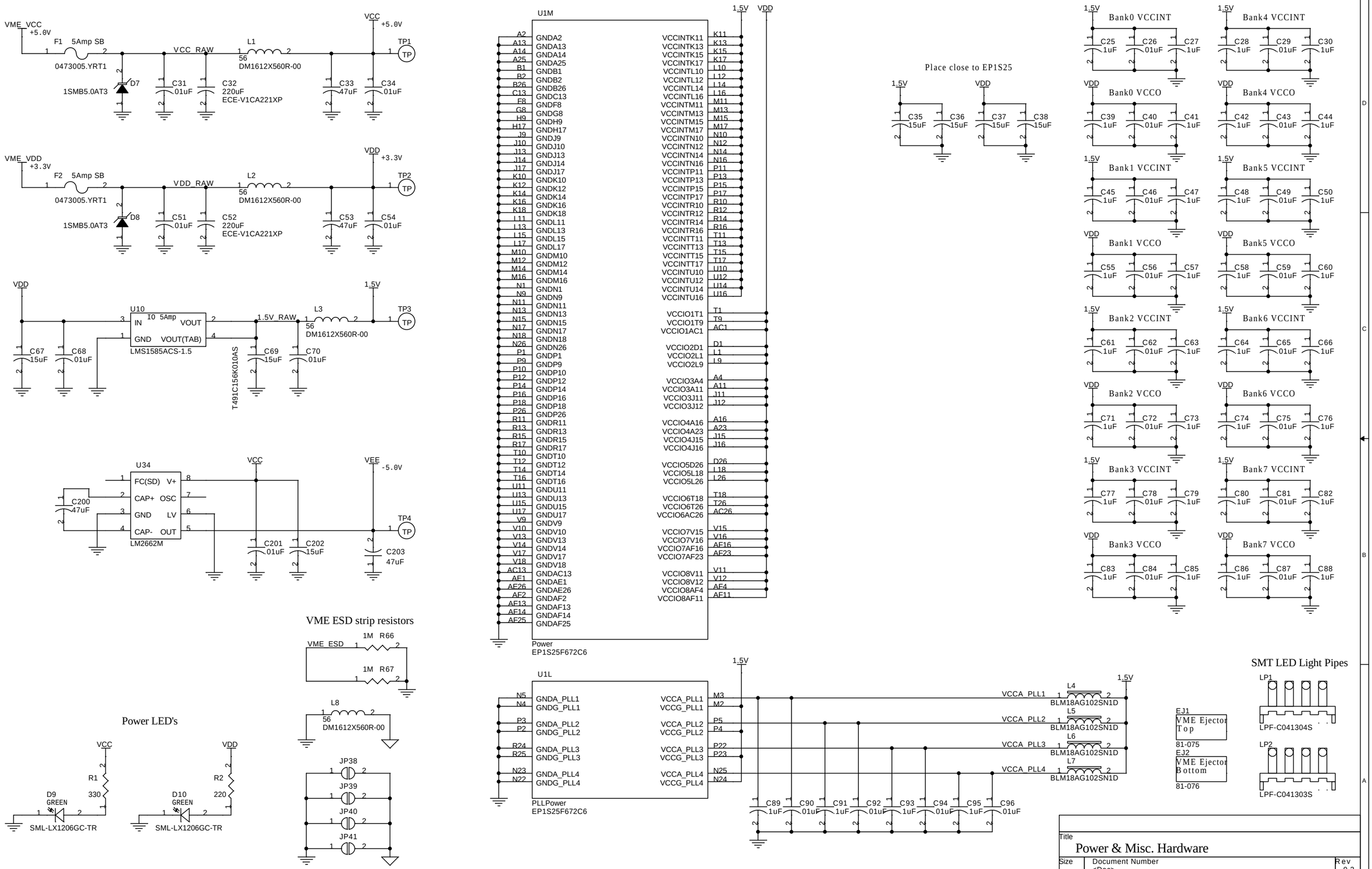

Title
Power & Misc. Hardware

Size	Document Number	Rev
	<Doc>	0.2

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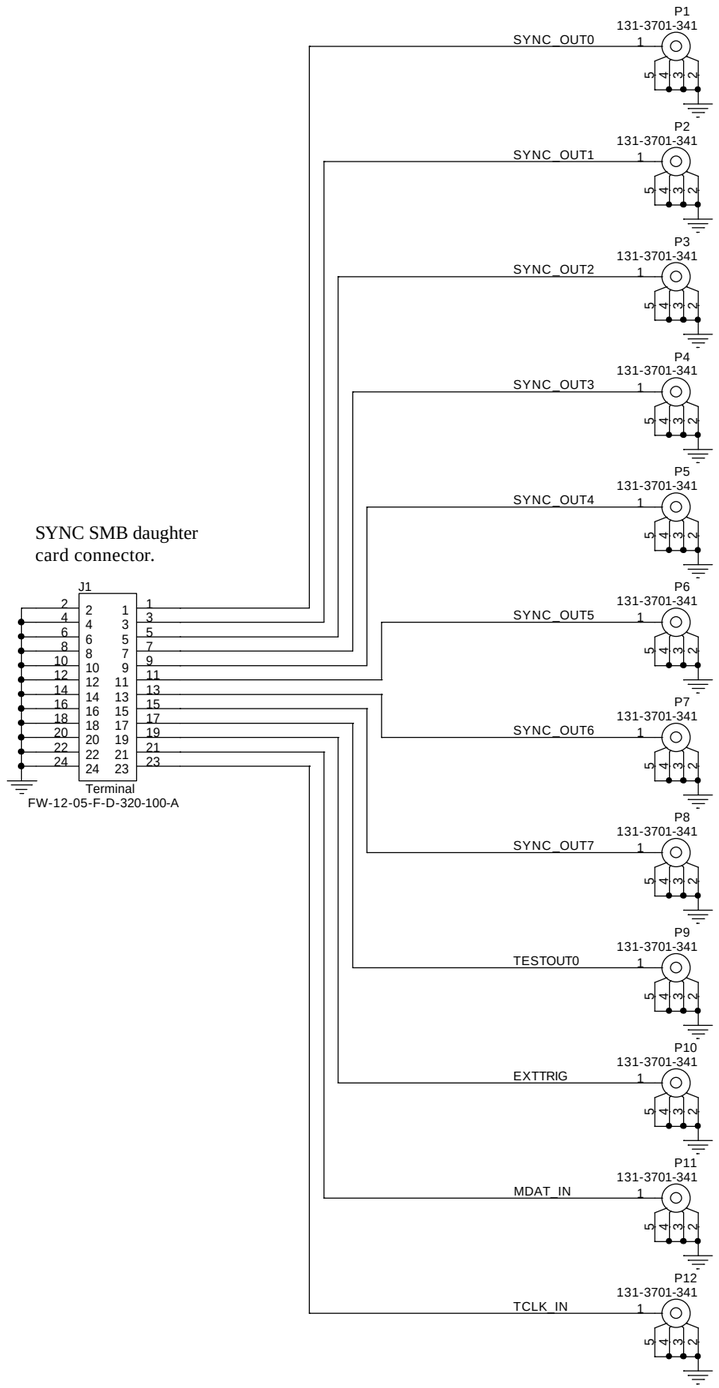
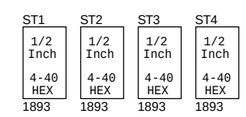
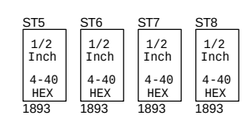
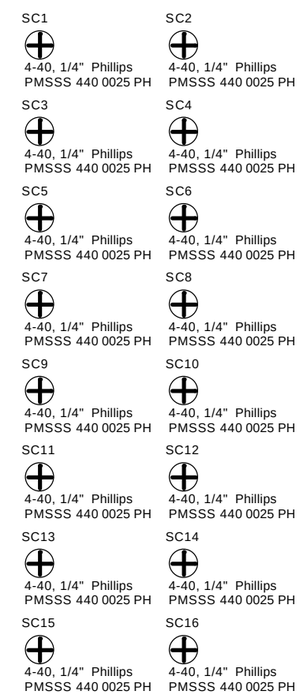
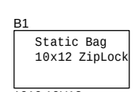
BPM Timing Fanout Daughter Card











Title	BPM Timing Fanout Daughter Card	
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